V93XX
Datasheet

Specifications are subject to change without notice.

Revision

Date	Version	Description
2019.07.19	2.0	Initial release
2020.11.25	2.1	Modify the description of SYS_STS register.
2020.02.18	3.1	Modify ANA_CTRL0 BIT13 and BIT14 function Modify ANA_CTRL1 BIT7 and BIT23 function Add pull-up resistance to TX, RX and RSTN pin When the RSTN pin remains low for a certain period of time, the chip will be reset. The time was changed from 1 ms to 2 ms Open the input short circuit function of voltage channel and current channel On-chip reference voltage changed to 1.21 V The power supply voltage range is changed to 2.6 ~ 3.6 V The power down threshold voltage is changed to 2.6 ~ 3.1 V
2022.01.20	3.2	Delete relevant contents of Roche coil
2022.03.01	3.3	Modify SYS_INTSTS and SYS_INTEN registers，increase the overflow interrupt of high-speed energy accumulator Modify the description of DMA_MODE bit in DSP_CTRL5 register (added description: at least one channel of waveform buffer and upload must be opened before enabling DMA transmission). Modify the description of bit3 and bit4 in DSP_CTRL5 registers, description of DMA channel manual switch for waveform upload. Delete the frequency function in DSP_CTRL0 register. Modify the function description of UPERIOD and IPERIOD from half cycle

		unit to cycle unit Modify SHORT_I of ANA_CTRL0, Change to current IA channel ADC input short circuit Modify the description of RCL clock intervals as determined time, and the algorithm is the longest time interval x 1.5 Modify the description of forced shutdown energy accumulator and CF output function in SYS_MISC register The power down threshold voltage is changed to 2.6 ~ 3.05 V
2022.03.25	3.4	Modify the description of CLK1 in Chapter 5
2022.05.19	3.5	Add Energy accumulator counter description Delete temperature measurement function ADD V9340/V9343 type
2022.08.13	3.6	Modify the table of parameter Modify UART baud rate range Table 5-1 in the field register, ANA_CTRL1 instead of DSP_CTRL1.
2022.10.11	3.7	Modify the description of voltage dip in Section 11.2
2023.03.01	3.8	Change V9343 to V9340T

Content

Figure List

Table List

1. General Description

The V93XX is a single-phase metering chip which supports the total-wave and fundamental-wave of various modes and supports various power grids to monitor events. Furthermore, the waveform data can be transmitted via DMA by SPI protocol, or storage locally through the waveform buffer.

- Main Power: 3.3 V power supply, voltage input range 2.6 V to 3.6 V.
- Reference voltage: 1.21 (typical T.C. 10 ppm/°C)
- Low-power design: the typical consumption in normal operation is about 2.6 mA.
- Metering Features:
  - 3 independent oversampling ∑/Δ ADCs: one of the ADC (channel A) can measure voltage, the other ADC with multifunction measure current.
  - Highly Metering Accurate:
    - Supports the requirements of IEC 62053-21:2020/ IEC 62053-22:2020 and IEC 62053-23:2020.
    - Less than 0.1% error in active energy metering over a dynamic range of 5000:1
    - Less than 0.2% error in reactive energy metering over a dynamic range of 5000:1
    - Less than 0.5% error in current/voltage RMS over a dynamic range of 5000:1.
  - Supports various measurements:
    - DC components of voltage and current signal
    - Total /fundamental instantaneous/average current/voltage RMS
    - Total instantaneous/average active /reactive/apparent power
    - 10 or 12 cycles of total RMS
    - Fundamental instantaneous/average active /reactive/apparent power
    - active/reactive energy, active/reactive/apparent power, Irms, constant value, and fundamental wave are selectable
    - Line frequency and phase
  - DC signals measurement

- Software calibration
- Accelerating calibration when weak current is applied.

- Supports detection for over-current, over-voltage, under-current, under-voltage, voltage dip, and voltage swell
- Supports waveform buffer and waveform transmitted by DMA
- Supports active upload for energy accumulation
- Current input: current shunt resistor, CT, Hall cell, and TMR supportive
- CTI input clock frequency: 6.5536 MHz
- Supports UART communication interface
- Supports SPI communication interface
- Operating Temperature:

  -40~+85 °C (V9381/ V9360/ V9340)

  -40~+105 °C (V9340T)
- Storage Temperature: -55~+150 °C
- Package: SSOP(M)24, SOP(M)16, SOP8

1.1. Functional Block Diagram

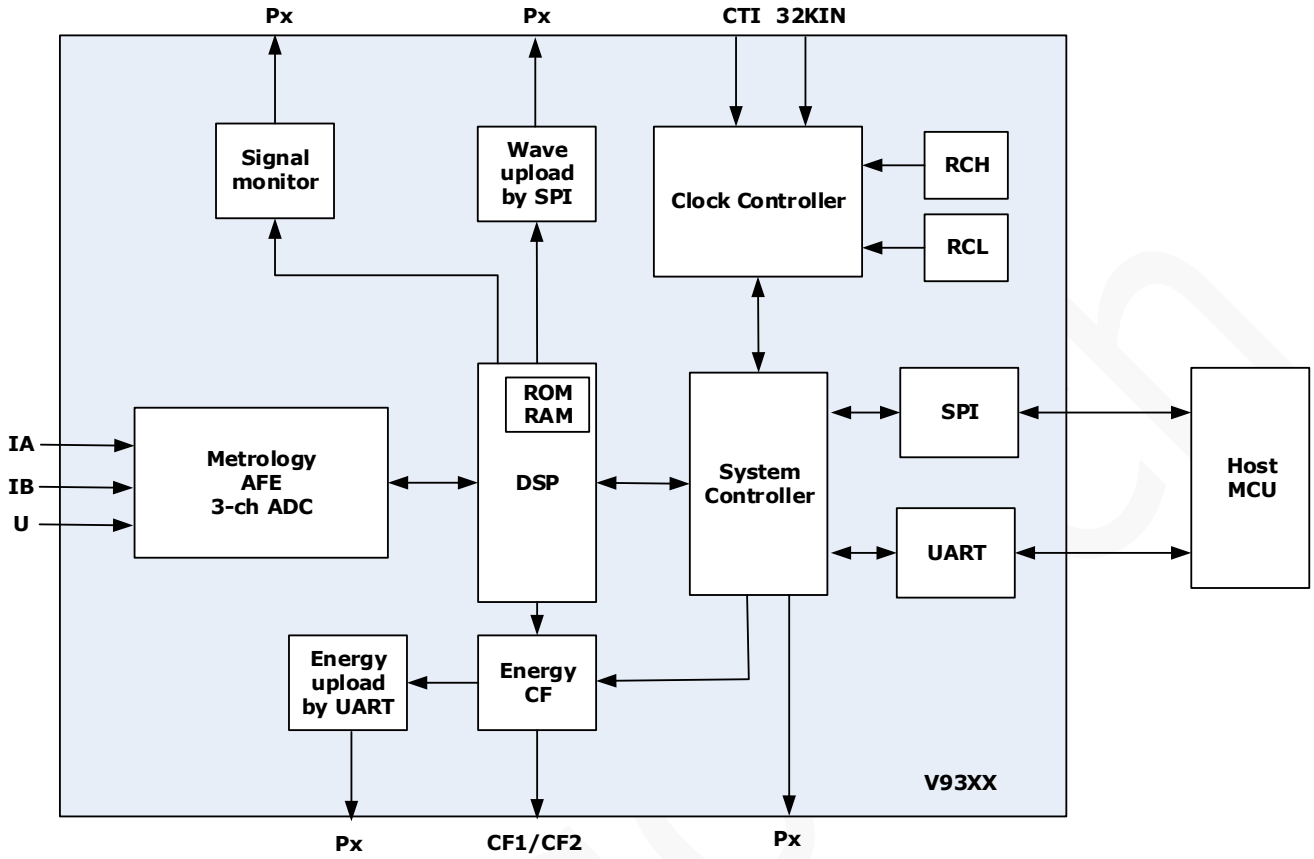


Figure 1-1 Functional block diagram

1.2. Pin Description

1.2.1. V9381 Pin Description

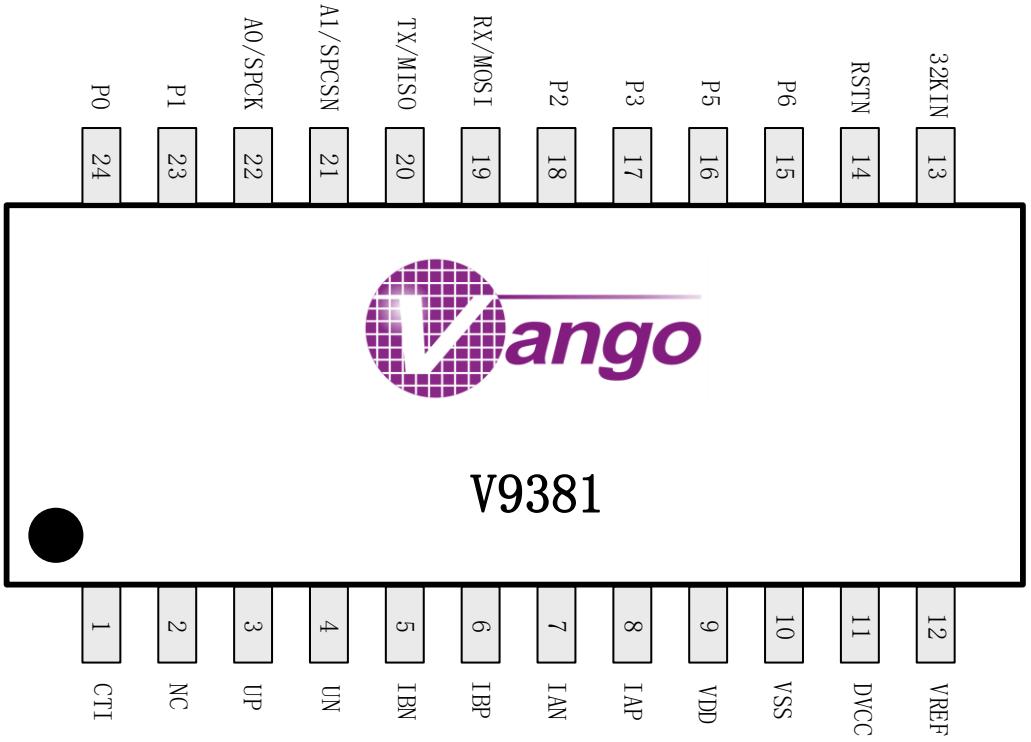


Figure 1-2 V9381 Pin Description

1.2.2. V9360 Pin Description

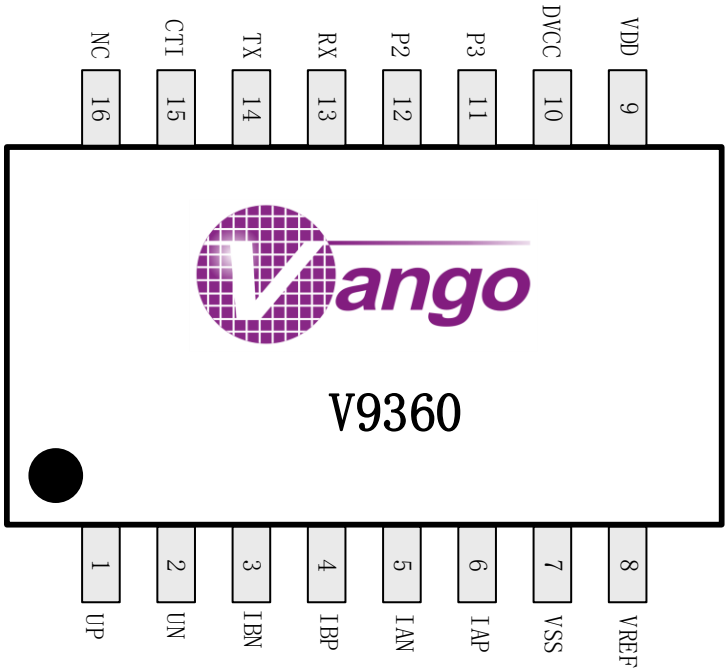


Figure 1-3 V9360 Pin Description

1.2.3. V9340 Pin Description

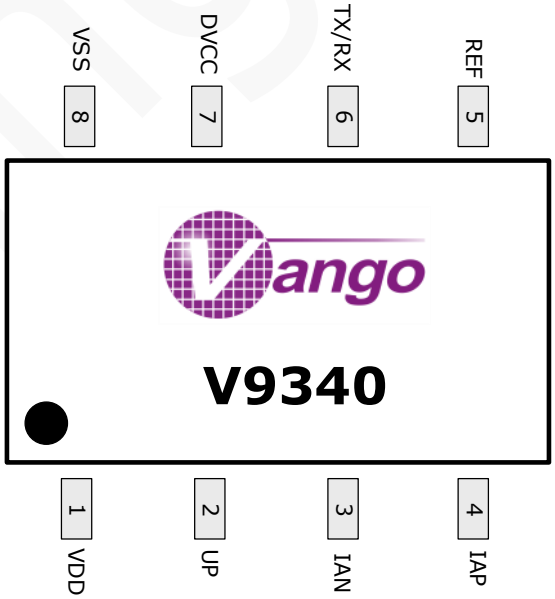


Figure 1-4 V9340 Pin Description

1.2.4. V9340T Pin Description

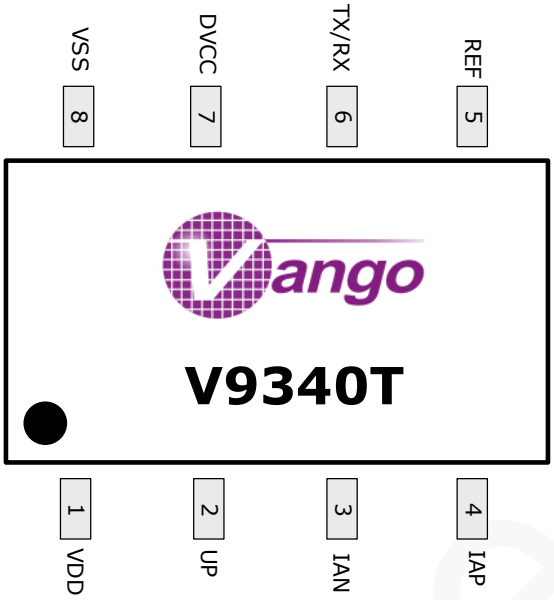


Figure 1-5 V9340T Pin Description

1.2.5. Pin Description

Table 1-1 Pin description

Pin No.			Mnemonic	Type	Description
V9381	V9360	V9340/V9340T			
1	15		CTI	Input	Input pin for 6.5536 MHz clock.
2	16		NC		Floating
3	1	2	UP	Input	Positive input pin for Voltage Channel Sampling.
4	2		UN	Input	Negative input pin for Voltage Channel Sampling.
5	3		IBN	Input	Negative input pin for current channel B sampling.
6	4		IBP	Input	Positive input pin for current channel B

					sampling.
7	5	3	IAN	Input	Negative input pin for current channel A sampling.
8	6	4	IAP	Input	Positive input pin for current channel A sampling.
9	9	1	VDD	Power	3.3 V power supply. This pin must be decoupled to a ⩾0.1 μF capacitor.
10	7	8	VSS	Ground	Ground
11	10	7	DVCC	Power	Digital power output. This pin must be connected to a parallel circuit combined by a ⩾4.7 μF capacitor and 0.1 μF capacitor, and then grounded.
12	8	5	VREF	Input/ Output	On-chip reference voltage. This pin must be connected to a 1 μF capacitor, and then grounded.
13	-		X32KIN	Input	32 KHz CLK input pin (Digital IO interface).
14	-		RSTN	Input	Reset input, active low. After power on, the "RSTN" could be driven low for at least 2 ms by MCU to force the chip into the reset state. There is a pull-up resistor inside the chip, which is about 50K ohm.
15	-		P6	Output	CF1/ CF2/ single interruption/ all interruption/ automatic data uploads
16	-		P5	Output	CF1/ CF2/ single interruption/ all interruption/ automatic data uploads
17	11		P3	Output	CF1/ CF2/ single interruption/ all interruption/ automatic data uploads

18	12		P2	Output	CF1/ CF2/ single interruption/ all interruption/ automatic data uploads
19	13	6	RX/MOSI	Input	UART communicates with RX pin. / SPI interface in slave mode. It's used for data input. There is a pull-up resistor inside the chip, which is about 50 Kohm.
20	14	6	TX/MISO	Output	UART communicates with TX pin. / SPI interface in slave mode. It's used for data output. There is a pull-up resistor inside the chip, which is about 50 Kohm.
21	-		A1/SPCSN	Input	Address select pin 1 for UART. / Chip select pin for SPI
22	-		A0/SPCK	Input	Address select pin 0 for UART. / SPI interface in slave mode. It's used for clock input.
23	-		P1	Output	CF1/ CF2/ single interruption/ all interruption/ automatic data uploads
24	-		P0	Output	CF1/ CF2/ single interruption/ all interruption/ automatic data uploads

1.3. Parameters

Table 1-2 Parameters

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Parameter	Min.	Typ.	Max.	Unit	Remark
Phase Error Between Channels					
PF=0.8 Capacitive		±0.05		Degree	
PF=0.5 Inductive		±0.05		Degree	

Parameter	Min.	Typ.	Max.	Unit	Remark
Active Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Active Energy Metering Bandwidth		1.6		kHz	
Reactive Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Reactive Energy Metering Bandwidth		1.6		kHz	
VRMS Metering Error		1		%	Dynamic Range 2000:1 @ 25°C Fundamental frequency deviation within ± 25%
VRMS Metering Bandwidth		1.6		kHz	
IRMS Metering Error		1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
IRMS Metering Bandwidth		1.6		kHz	
Frequency Measurement					
Range	40		70	Hz	
Error		0.01		Hz	
Analog Input					
Maximum Signal Level			±200	mV	Peak value
ADC					
DC Offset			10	mV	
Resolution		23		Bit	Sign bit is included.
Bandwidth (-3dB)	0.4	3.2	6.4	kHz	
On-chip Reference					
Reference Error	-18		18	mV	@ 25°C
Power Supply Rejection Ratio		92		dB	
Temperature Coefficient		10	30	ppm/°C	

Parameter	Min.	Typ.	Max.	Unit	Remark
Output Voltage		1.210		V	
Power Supply					
VDD33	2.6	3.3	3.6	V	
POR Detection Threshold	1.22	1.3	1.34	V	Error: ±10%
Power-Down Detection Threshold	2.6	2.8	3.05	V	
Digital Power Supply (DVCC)					
Voltage		1.5		V	Programmable. Error: ±10%
Current			35	mA	
CTI					
RCL frequency	-50%	32.768	+50%	KHz	
RCH frequency	-20%	6.5536	+20%	MHz	
Logic Input	RX				
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}	0		0.4	V	
Input Current, I_{IN}			1	μA	
Input Capacitance, C_{IN}			10	pF	
Baud Rate	1200		19200	bps	Automatic baud rate adaption
SPI Data Rate			800	KHz	Related to system CLK, the highest speed is one sixteenth of system CLK.

1.4. Absolute Maximum Ratings

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V. Operating circumstance exceeding Absolute Maximum Ratings may cause permanent damage to the device.

Table 1-3 Absolute maximum ratings

Parameter	Mnemonic	Min.	Max.	Unit	Description
Analog Power Supply	VDD	-0.3	+3.63	V	To ground.
Digital Power Supply	DVCC	-0.3	+1.98	V	To ground.
Analog Input Voltage	IAP/IAN/IBP/IBN	-0.3	3.3	V	To ground.
Analog Input Voltage	UP/UN	-0.3	3.3	V	To ground.
Operating Temperature		-40	+85	°C	V9381/V9360/V9340
		-40	+105	°C	V9340T
Storage Temperature		-55	+150	°C	

2. Registers

All register will be reset to default value which are hexadecimal when V93XX is in the reset state. There are four kinds of reset conditions, including power on reset (POR) external pin reset, global software reset, and RX reset.

2.1. Registers List

Table 2-1 Register list

Register	Type	Address	Description	Default
DSP_CTRL0	R/W	0x00	Analog Control Register 0.	0x00000000
DSP_CTRL1	R/W	0X01	Analog Control Register 1.	0x00000000
DSP_CTRL0	R/W	0x02	Metering Control Register 0.	0x00000000
DSP_CTRL1	R/W	0x03	Metering Control Register 1.	0x00000000
DSP_CTRL2	R/W	0x04	Metering Control Register 2.	0x00000000
DSP_CTRL3	R/W	0x05	Metering Control Register 3.	0x00000000
DSP_CTRL4	R/W	0x06	Metering Control Register 4.	0x00000000
DSP_CTRL5	R/W	0x07	Metering Control Register 5.	0x00000000
DSP_DAT_PA	R	0x08	Instantaneous Active Power of channel A.	--
DSP_DAT_QA	R	0x09	Instantaneous Reactive Power of channel A.	--
DSP_DAT_SA	R	0x0A	Instantaneous Apparent Power of channel A.	--
DSP_DAT_PB	R	0x0B	Instantaneous Active Power of channel B.	--
DSP_DAT_QB	R	0x0C	Instantaneous Reactive Power of channel B.	--
DSP_DAT_SB	R	0x0D	Instantaneous Apparent Power of channel B.	--
DSP_DAT_RMS0UA	R	0x0E	Instantaneous RMS of Voltage.	--
DSP_DAT_RMS0IA	R	0x0F	Instantaneous RMS of current A.	--
DSP_DAT_RMS0IB	R	0x10	Instantaneous RMS of Current B.	--
DSP_DAT_CH1	R	0x11	Instantaneous Value of Fundamental wave of Channel 1.	--
DSP_DAT_CH2	R	0x12	Instantaneous Value of Fundamental wave of	--

			Channel 2.	
DSP_DAT_PA1	R	0x13	Average Active Power of Channel A.	--
DSP_DAT_QA1	R	0x14	Average Reactive Power of Channel A.	--
DSP_DAT_SA1	R	0x15	Average Apparent Power of Channel A.	--
DSP_DAT_PB1	R	0x16	Average Active power of Channel B.	--
DSP_DAT_QB1	R	0x17	Average Reactive power of Channel B.	--
DSP_DAT_SB1	R	0x18	Average Apparent Power of Channel B.	--
DSP_DAT_RMS1U	R	0x19	Average RMS of Voltage.	--
DSP_DAT_RMS1IA	R	0x1A	Average RMS of Current A.	--
DSP_DAT_RMS1IB	R	0x1B	Average RMS of Current B.	--
DSP_DAT_CH1_AVG	R	0x1C	Average value of Fundamental wave of Channel 1.	--
DSP_DAT_CH2_AVG	R	0x1D	Average value of Fundamental wave of Channel 2.	--
DSP_DAT_RMSU_AVG	R	0x1E	Average RMS of Voltage for 10 or 12 cycles (chose by line frequency).	--
DSP_DAT_RMSIA_AVG	R	0x1F	Average RMS of Current IA for 10 or 12 cycles (chose by line frequency).	--
DSP_DAT_RMSIB_AVG	R	0x20	Average RMS of Current IB for 10 or 12 cycles (chose by line frequency).	--
DSP_DAT_FRQ	R	0x21	Line Frequency.	--
DSP_DAT_DCU	R	0x22	DC value of voltage channel.	--
DSP_DAT_DCIA	R	0x23	DC value of current channel A.	--
DSP_DAT_DCIB	R	0x24	DC value of Current channel B.	--
DSP_CFG_CALI_PA	R/W	0x25	To set gain calibration for the active power A.	0x00000000
DSP_CFG_DC_PA	R/W	0x26	To set offset calibration for the active power A.	0x00000000
DSP_CFG_CALI_QA	R/W	0x27	To set gain calibration for Reactive power A.	0x00000000
DSP_CFG_DC_QA	R/W	0x28	To set offset calibration for Reactive power A.	0x00000000
DSP_CFG_CALI_PB	R/W	0x29	To set gain calibration for Active power B.	0x00000000

DSP_CFG_DC_PB	R/W	0x2A	To set offset calibration for Active power B.	0x00000000
DSP_CFG_CALI_QB	R/W	0x2B	To set gain calibration for Reactive power B.	0x00000000
DSP_CFG_DC_QB	R/W	0x2C	To set offset calibration for Reactive power B.	0x00000000
DSP_CFG_CALI_RMSU	R/W	0x2D	To set gain calibration for Voltage RMS.	0x00000000
DSP_CFG_RMS_DCU	R/W	0x2E	To set offset calibration for Voltage RMS.	0x00000000
DSP_CFG_CALI_RMSIA	R/W	0x2F	To set gain calibration for Current RMS A.	0x00000000
DSP_CFG_RMS_DCIA	R/W	0x30	To set offset calibration for Current RMS A.	0x00000000
DSP_CFG_CALI_RMSIB	R/W	0x31	To set gain calibration for Current RMS B.	0x00000000
DSP_CFG_RMS_DCIB	R/W	0x32	To set offset calibration for Current RMS B.	0x00000000
DSP_CFG_PHC	R/W	0x33	Phase Error Calibration Register. [10:0]= phase error calibration value for channel A [26:16]= phase error calibration value for channel B, where the range is from -766~767.	0x00000000
DSP_CFG_DCU	R/W	0x34	To set the DC calibration for the voltage channel.	0x00000000
DSP_CFG_DCIA	R/W	0x35	To set the DC calibration for the current channel A.	0x00000000
DSP_CFG_DCIB	R/W	0x36	To set the DC calibration for the current channel B.	0x00000000
DSP_CFG_BPF	R/W	0x37	Band-pass filter coefficient. Related to setting the DSP_MODE by Bit[7:4] of metering control register 0 (0x02,DSP_CTRL0). Setting 0x806764B6 at DSP_MODE=0, 1, 2; Setting 0x80DD7A8C at DSP_MODE=6, 7; Setting 0x82B465F0 at DSP_MODE=8. The frequency of other modes would be not	0x00000000

			supported to measure, so setting to 0x0.	
DSP_CFG_CKSUM	R/W	0x38	Configuration register for checksum.	0x00000000
EGY_PROCTH	R/W	0x39	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.	0x00000000
EGY_PWRTH	R/W	0x3A	Accumulation threshold for energy accumulator. Because the energy accumulator was 46Bit, the accumulated value of the high-speed energy accumulator equals to this threshold*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.	0x00000000
EGY_CONST1	R/W	0x3B	Energy accumulator 1 accumulating constant.	0x00000000
EGY_OUT1L	R/W	0x3C	Energy accumulator 1 accumulating lower bit.	0x00000000
EGY_OUT1H	R/W	0x3D	Energy accumulator 1 accumulating higher bit. Effective for lower 14 bit.	0x00000000
EGY_CFCNT1	R	0x3E	Energy accumulator 1 pulse counter.	0x00000000
EGY_CONST2	R/W	0x3F	Energy accumulator 2 accumulating constant.	0x00000000
EGY_OUT2L	R/W	0x40	Energy accumulator 2 accumulating lower bit.	0x00000000
EGY_OUT2H	R/W	0x41	Energy accumulator 2 accumulating higher bit. Effective for lower 14 bit.	0x00000000
EGY_CFCNT2	R	0x42	Energy accumulator 2 pulse counter.	0x00000000
EGY_CONST3	R/W	0x43	Energy accumulator 3 accumulating constant.	0x00000000
EGY_OUT3	R/W	0x44	Energy accumulator 3 accumulating value.	0x00000000
EGY_CFCNT3	R	0x45	Energy accumulator 3 pulse counter.	0x00000000
EGY_CONST4	R/W	0x46	Energy accumulator 4 accumulating constant.	0x00000000
EGY_OUT4	R/W	0x47	Energy accumulator 4 accumulating value.	0x00000000

EGY_CFCNT4	R	0x48	Energy accumulator 4 pulse counter.	0x00000000
EGY_CONST5	R/W	0x49	Energy accumulator 5 accumulating constant.	0x00000000
EGY_OUT5	R/W	0x4A	Energy accumulator 5 accumulating value.	0x00000000
EGY_CFCNT5	R	0x4B	Energy accumulator 5 pulse counter.	0x00000000
EGY_CONST6	R/W	0x4C	Energy accumulator 6 accumulating constant.	0x00000000
EGY_OUT6	R/W	0x4D	Energy accumulator 6 accumulating value.	0x00000000
EGY_CFCNT6	R	0x4E	Energy accumulator 6 pulse counter.	0x00000000
EGY_CONST7	R/W	0x4F	Energy accumulator 7 accumulating constant.	0x00000000
EGY_OUT7	R/W	0x50	Energy accumulator 7 accumulating value.	0x00000000
EGY_CFCNT7	R	0x51	Energy accumulator 7 pulse counter.	0x00000000
EGY_CONST8	R/W	0x52	Energy accumulator 8 accumulating constant.	0x00000000
EGY_OUT8	R/W	0x53	Energy accumulator 8 accumulating value.	0x00000000
EGY_CFCNT8	R	0x54	Energy accumulator 8 pulse counter.	0x00000000
DSP_OV_THL	R/W	0x55	To set the lower threshold for the power-creep detection.	0x00000000
DSP_OV_THH	R/W	0x56	To set the upper threshold for the power-creep detection.	0x00000000
DSP_SWELL_THL	R/W	0x57	To set the lower threshold for the voltage swell.	0x00000000
DSP_SWELL_THH	R/W	0x58	To set the upper threshold for the voltage dip.	0x00000000
DSP_DIP_THL	R/W	0x59	To set the lower threshold for the voltage dip.	0x00000000
DSP_DIP_THH	R/W	0x5A	To set the upper threshold for the voltage dip.	0x00000000
FD_OVTH	R/W	0x5B	To set over-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
FD_LVTH	R/W	0x5C	To set under-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
FD_IA_OCTH	R/W	0x5D	To set over-current threshold in current channel A for fast detection. Bit width is 30bit.	0x00000000
FD_IA_LCTH	R/W	0x5E	To set under-current threshold in current channel A for fast detection. Bit width is 30bit.	0x00000000

FD_IB_OCTH	R/W	0x5F	To set over-current threshold in current channel B for fast detection. Bit width is 30bit.	0x00000000
FD_IB_LCTH	R/W	0x60	To set under-current threshold in current channel B for fast detection. Bit width is 30bit.	0x00000000
DSP_PHS_STT	R/W	0x61	To control the phase measurement. Enable phase measurement once for writing operation.	--
DSP_PHS_U	R	0x62	Voltage phase.	1
DSP_PHS_UN	R	0x63	Voltage waveform data which before zero-crossing.	0
DSP_PHS_UP	R	0x64	Voltage waveform data which after zero-crossing.	0x80000000
DSP_PHS_I	R	0x65	Current phase.	1
DSP_PHS_IN	R	0x66	Current waveform data which before zero-crossing.	0
DSP_PHS_IP	R	0x67	Current waveform data which after zero-crossing.	0x80000000
DAT_WAVE	R	0x69	Waveform data reading. It can repeatable reading the address and obtain the overall waveform data. If there is no need to read all data, it would be reset the bit 31 of DSP_CTRL5 to read address.	0
DAT_SWELL_CNT	R/C	0x6A	Voltage swell time records, half-wave as unit. Effective as 24bit. Writing any value into this address would be clear this counter to zero.	0
DAT_DIP_CNT	R/C	0x6B	Voltage dip time records, half wave as unit. Effective as 24bit. Writing any value into this address would be clear this counter to zero.	0
SYS_SFTRST	W	0x6C	Software reset register. Writing 0x4572beaf into this address would be happen software reset once.	--
SYS_BAUDCNT1	R	0x70	This register stores the system clock count value of the first bit of the UART frame header sent by	--

			V93XX.	
SYS_BAUDCNT8	R	0x71	This register stores the system clock count value of the 8 bits of the UART frame header received by V93XX.	--
SYS_INTSTS	R/C	0x72	Interrupt status register.	--
SYS_INTEN	R/W	0x73	Interrupt enable register.	0x00000000
SYS_STS	R	0x74	System status register.	--
SYS_MISC	R/W	0x75	System control register.	--
SYS_BLK0_ADDR	R/W	0x79	Register for block reading address 0.	0
SYS_BLK1_ADDR	R/W	0x7A	Register for block reading address 1.	0
SYS_BLK2_ADDR	R/W	0x7B	Register for block reading address 2.	0
SYS_BLK3_ADDR	R/W	0x7C	Register for block reading address 3.	0
SYS_IOCFGX0	R/W	0x7D	Output configuration register for P0, P1, P2 and P3.	0
SYS_IOCFGX1	R/W	0x7E	Output configuration register for P4, P5 and P6.	0
SYS_VERSION	R	0x7F	Present hardware version.	--

2.2. Analog Control Registers

When power-on reset (POR), RSTN pin reset, RX reset, or global software reset occurs, all analog control registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

The address range of Analog Control Register is 0x00~0x01 which all is readable and writable. Also, all the metering control registers need to be configuration verification and self-checking.

2.2.1. ANA_CTRL0 Register

Table 2-2 Analog Control Register 0 (0x00, ANA_CTRL0)

0x00, R/W, Analog Control Register 0, ANA_CTRL0			
Bit		Default Value	Description
31:18	Reserved	0	These bits must hold its default value for proper operation.
17:14	Reserved	0	These bits must hold its default value for proper operation.
13	MEA	0	To select the analog input for Channel IB. 0: differential IB input 1: Reserved
12	Reserved	0	The bit must hold its default value for proper operation.
11	SHORT_I	0	Current IA channel ADC input short circuit. 0: short circuit 1: Normal
10	SHORT_V	0	Voltage U channel ADC input short circuit. 0: short circuit 1: Normal
9:0	Reserved	0	These bits must hold its default value for proper operation.

2.2.2. ANA_CTRL1 Register

Table 2-3 Analog Control Register 1 (0x01, ANA_CTRL1)

0x01, R/W, Analog Control Register 1, ANA_CTRL1			
Bit		Default Value	Description
31:30	ADCKSEL[1:0]	0	The options of clock frequency divider rate for the ADC

0x01, R/W, Analog Control Register 1, ANA_CTRL1			
Bit		Default Value	Description
			00 corresponds to 819.2 KHz. 00: ×1 01: ×2 10: ×1/4 11: ×1/2
29:24	RCHTRIM[5:0]	0	To adjust the 6.5M RC frequency. 000000~011111: step-up the frequency by 1.25% 100000~111111: step-down the frequency by 1.25%
23	Reserved	0	The bit must hold its default value for proper operation.
22	RCCLK_PD	0	To enable the 6.5M RC oscillator. 0: enable 1: disable This bit must be set to 0 for proper operation.
21:15	Reserved	0	These bits must hold its default value for proper operation.
14:12	GIB[2:0]	0	To adjust the gain of current ADC in the channel B. 000: 4 001: 1 010: 32 011: 16 100/101/110/111: prohibited GIB[2:0] is recommended set to 000 for proper operation.
11	GU	0	To adjust the gain of voltage ADC.

0x01, R/W, Analog Control Register 1, ANA_CTRL1			
Bit		Default Value	Description
			0: 8 1: 4 This bit must be set to 0 for proper operation.
10:8	GIA[2:0]	0	To adjust the gain of current ADC in the channel A. 000: 32 001: 16 010: 4 011: 1 100~111: prohibited GIA[2:0] is recommended set to 000 for proper operation.
7	XRST_PD	0	The external input CTI clock enable. 0: enable 1: disable
6:5	Reserved	0	These bits must hold its default value for proper operation.
4:3	RESTL[1:0]	0	To roughly adjust the temperature coefficient of the Bandgap circuit. 00: 0 ppm 01: -58 ppm 10: +111 ppm 11: +56 ppm
2:0	REST[2:0]	0	To finely adjust the temperature coefficient of the Bandgap circuit.

0x01, R/W, Analog Control Register 1, ANA_CTRL1			
Bit		Default Value	Description
			000: 0 ppm 001: +7 ppm 010: +14 ppm 011: +28 ppm 100: -32 ppm 101: -21 ppm 110: -14 ppm 111: -7 ppm

2.3. System Control & Status Register

When power-on reset (POR), RSTN pin reset, RX reset, or global software reset occurs, all system control registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

In the V93XX, the mainly functions of System Control Register is controlling interface, interrupt, RAM, and IO output. SYS_INTEN (0x73) controls enable interruption, SYS_INTSYS (0x72) is interrupted status register. Bit[4: 0] of SYS_MISC (0x75) are used for configuring the interface operation, interrupting pin output whether reverse, whether turn off the energy accumulator when power down and whether turn off the energy accumulator when in wrong calibration. SYS_RAMADDR (0x77) is controlling internal RAM address. SYS_RAMDATA is internal RAM data registers. SYS_BLK0_ADDR~SYS_BLK3_ADDR are blocked reading address. SYS_IOCFGX0~SYS_IOCFGX1 are the control register of IO output

2.3.1. SYS_BAUDCNT1 Register

Table 2-4 UART transmitting data 1bit count value (0x70, SYS_BAUDCNT1)

0x70, UART transmitting data 1bit count value, SYS_BAUDCNT1				
bit		R/W	Default Value	Description
31:14	-	-	-	Reserved.
13:0	BAUDCNT1	R		This register stores the system clock count value of the first bit of the UART frame header sent by V93XX.

2.3.2. SYS_BAUDCNT8 Register

Table 2-5 UART receiving data 8bit count value (0x71, SYS_BAUDCNT8)

0x71, UART receiving data 8bit count value, SYS_BAUDCNT8				
Bit		R/W	Default Value	Description
31:17	-	-	-	Reserved.
16:0	BAUDCNT8	R		This register stores the system clock count value of the 8 bits of the UART frame header received by V93XX.

2.3.3. SYS_INTSTS Register

Table 2-6 System Interrupt Register (0x72, SYS_INTSTS)

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
31:30	-	-	-	Reserved.
29	EGY2OV	R/C	0	Flag bit for high-speed energy accumulator 2 overflow interrupt Read 0: high-speed energy accumulator overflow did not happen Read 1: high-speed energy accumulator overflow happened

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
				Write 0: no effects Write 1: clear the bit
28	EGY1OV	R/C	0	Flag bit for high-speed energy accumulator 1 overflow interrupt Read 0: high-speed energy accumulator overflow did not happen Read 1: high-speed energy accumulator overflow happened Write 0: no effects Write 1: clear the bit
27	UDIP	R/C	0	Flag bit for the voltage dip. Read 0: the voltage dip did not happen Read 1: the voltage dip happened Write 0: no effects Write 1: clear the bit
26	USWELL	R/C	0	Flag bit for the voltage swell. Read 0: the voltage swell did not happen Read 1: the voltage swell happened Write 0: no effects Write 1: clear the bit
25	IBLC	R/C	0	Flag bit for the IB under-current. Read 0: IB under-current did not happen Read 1: IB under-current happen Write 0: no effects Write 1: clear the bit
24	IBOC	R/C	0	Flag bit for the IB over-current. Read 0: IB over-current did not happen Read 1: IB over-current happened

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
				Write 0: no effects Write 1: clear the bit
23	IALC	R/C	0	Flag bit for the IA under-current. Read 0: IA under-current did not happen Read 1: IA under-current happened Write 0: no effects Write 1: clear the bit
22	IAOC	R/C	0	Flag bit for the IA over-current. Read 0: IA over-current did not happen Read 1: IA over-current happened Write 0: no effects Write 1: clear the bit
21	ULV	R/C	0	Flag bit for the channel U under-voltage. Read 0: channel U under-voltage did not happen Read 1: channel U under-voltage happened Write 0: no effects Write 1: clear the bit
20	UOV	R/C	0	Flag bit for the channel U over-voltage. Read 0: channel U over-voltage did not happen Read 1: channel U over-voltage happened Write 0: no effects Write 1: clear the bit
19	SPI_ERR	R/C	0	Flag bit for the SPI communication error. When any one of condition below happens, the bit will set to "1". A, SPI overtime (rising edge of each 2 SPCK needs to shorter than 20 ms) B, SPI CLK counter error (the number of clocks not equals to 48 at 4-wire SPI)

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
				Read 0: SPI error did not happen Read 1: SPI error happened write 0: no effects write 1: clear the bit
18:17	Reserved	-	-	-
16	UART_ERR	R/C	0	Flag bit for the UART communication error. When any one of condition as below happens, the bit will set to "1". A: UART overtime (each 2 Bytes needs to shorter than 20 ms) B: UART checksum bit error C: UART checksum byte error Read 0: UART error did not happen Read 1: UART happened write 0: no effects write 1: clear the bit
15	DMA_FINISH	R/C	0	Flag bit for active waveform uploading finished. Read 0: active waveform uploading did not finish Read 1: active waveform uploading finished Write 0: no effects Write 1: clear the bit
14	CKERR	R/C		Flag bit for checksum error. Checksum from correct to error, it would be interrupted. Read 0: checksum error did not happen Read 1: checksum error happened Write 0: no effects Write 1: clear the bit
13	HSE_FAIL	R/C		Flat bit for CTI external input clock status. Read 0: CTI external input clock error has

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
				occurred l did not happen Read 1: CTI external input clock error has happened Write 0: no effects Write 1: clear the bit
12	REF_ERR	R/C		Flag bit for reference error Read 0: reference error did not happen Read 1: reference error happened Write 0: no effects Write 1: clear the bit
11	BIST_ERR	R/C		Flag bit for BIST error Read 0: BIST error did not happen Read 1: BIST error happened Write 0: no effects Write 1: clear the bit
10	ISIGN	R/C		Flag bit for current zero-crossing, it could to select the channel IA or IB by bit20 of metering control register (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)), and to select the direction of zero-crossing by bit19~bit18 of metering control register (0x03,DSP_CTRL1). Read 0: current zero-crossing did not happen Read 1: current zero-crossing happened Write 0: no effects Write 1: clear the bit
9	USIGN	R/C		Flag bit for voltage zero-crossing, it could to select the direction of zero-crossing by bit19~bit18 of DSP_CTRL1 Read 0: voltage zero-crossing did not happen

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
				Read 1: voltage zero-crossing happened Write 0: no effects Write 1: clear the bit
8	WAVE_OVERFLOW	R/C	0	Flag bit for waveform storage overflow. Read 0: waveform storage did not overflow Read 1: waveform storage already overflowed Write 0: no effects Write 1: clear the bit
7	WAVE_STORE	R/C	0	Flag bit for waveform storage status. Read 0: waveform storage did not finish Read 1: waveform storage already finished Write 0: no effects Write 1: clear the bit
6	WAVE_UPD	R/C	0	Flag bit for waveform updating. Read 0: waveform data did not update Read 1: waveform data updated Write 0: no effects Write 1: clear the bit
5	CURRMS_UPD	R/C	0	Flag bit for instantaneous RMS data updating. Read 0: instantaneous RMS data did not update Read 1: instantaneous RMS data updated Write 0: no effects Write 1: clear the bit
4	AVGRMS_UPD	R/C	0	Flag bit for average RMS data updating. Read 0: average RMS data did not update Read 1: average RMS data updated Write 0: no effects Write 1: clear the bit
3	CURPOWER_UPD	R/C	0	Flag bit for instantaneous power data updating.

0x72, System Interrupt Register, SYS_INTSTS				
Bit		R/W	Default value	Description
				Read 0: instantaneous power data did not update Read 1: instantaneous power data updated Write 0: no effects Write 1: clear the bit
2	AVGPOWER_UPD	R/C	0	Flag bit for average power data updating. Read 0: average power data did not update Read 1: average power data updated Write 0: no effects Write 1: clear the bit
1	INTPDN	R/C	0	Flag bit for power down event. When the power input (VDD) is lower than 2.8V (±7%), it would be triggered. Read 0: power down did not happen Read 1: power down happened Write 0: no effects Write 1: clear the bit
0	INTUPHSDONE	R/C	0	Flag bit for Phase measurement finished. This bit will clear automatically when starts to phase measurement. Read 0: phase measurement did not finish Read 1: phase measurement already finished Write 0: no effects Write 1: clear the bit

2.3.4. SYS_INTEN Register

Table 2-7 System Interrupt Enable Register (0x73, SYS_INTEN)

0x73, System Interrupt Enable Register, SYS_INTEN				
Bit		R/W	Default Value	Description
31:30	Reserved		0	These bits must hold its default value for proper operation.
29	EGY2OV	R/W	0	Interrupt for high-speed energy accumulator 2 overflow 0: disable interrupt 1: enable interrupt
28	EGY1OV	R/W	0	Interrupt for high-speed energy accumulator 1 overflow 0: disable interrupt 1: enable interrupt
27	UDIP	R/W	0	Interrupt for the voltage dip. 0: disable interrupt 1: enable interrupt
26	USWELL	R/W	0	Interrupt for voltage swell. 0: disable interrupt 1: enable interrupt
25	IBLC	R/W	0	Interrupt for IB under-current. 0: disable interrupt 1: enable interrupt
24	IBOC	R/W	0	Interrupt for IB over-current. 0: disable interrupt 1: enable interrupt
23	IALC	R/W	0	Interrupt for IA under-current. 0: disable interrupt 1: enable interrupt

0x73, System Interrupt Enable Register, SYS_INTEN				
Bit		R/W	Default Value	Description
22	IAOC	R/W	0	Interrupt for IA over-current. 0: disable interrupt 1: enable interrupt
21	ULV	R/W	0	Interrupt for channel U under-voltage. 0: disable interrupt 1: enable interrupt
20	UOV	R/W	0	Interrupt for channel U over-voltage. 0: disable interrupt 1: enable interrupt
19	SPI_ERR	R/W	0	Interrupt for SPI transmission error. 0: disable interrupt 1: enable interrupt
18:17	Reserved			These bits must hold its default value for proper operation.
16	UART_ERR	R/W	0	Interrupt for UART transmission error. 0: disable interrupt 1: enable interrupt
15	DMA_FINISH	R/W	0	Waveform uploading finished. 0: disable interrupt 1: enable interrupt
14	CKERR	R/W	0	Interrupt for checksum error. 0: disable interrupt 1: enable interrupt
13	HSE_FAIL	R/W	0	Interrupt for CTI external input clock error. 0: disable interrupt

0x73, System Interrupt Enable Register, SYS_INTEN				
Bit		R/W	Default Value	Description
				1: enable interrupt
12	REF_ERR	R/W	0	Interrupt for reference error. 0: disable interrupt 1: enable interrupt
11	BOST_ERR	R/W	0	Interrupt for BIST error. 0: disable interrupt 1: enable interrupt
10	ISIGN	R/W	0	Interrupt for the current zero-crossing. 0: disable interrupt 1: enable interrupt
9	USIGN	R/W	0	Interrupt for the voltage zero-crossing. 0: disable interrupt 1: enable interrupt
8	WAVE_OVERFLOW	R/W	0	Interrupt for the Waveform storage overflow. 0: disable interrupt 1: enable interrupt
7	WAVE_STORE	R/W	0	Interrupt for the Waveform storage status. 0: disable interrupt 1: enable interrupt
6	WAVE_UPD	R/W	0	Interrupt for the Waveform data updating. 0: disable interrupt 1: enable interrupt
5	CURRMS_UPD	R/W	0	Interrupt for the Instantaneous RMS data updating. 0: disable interrupt

0x73, System Interrupt Enable Register, SYS_INTEN				
Bit		R/W	Default Value	Description
				1: enable interrupt
4	AVGRMS_UPD	R/W	0	Interrupt for the average RMS data updating. 0: disable interrupt 1: enable interrupt
3	CURPOWER_UPD	R/W	0	Interrupt for the Instantaneous power data updating. 0: disable interrupt 1: enable interrupt
2	AVGPOWER_UPD	R/W	0	Interrupt for the Average power data updating. 0: disable interrupt 1: enable interrupt
1	INTPDN	R/W	0	Interrupt for the Power down. 0: disable interrupt 1: enable interrupt
0	INTUPHSDONE	R/W	0	Interrupt for the Phase measurement finished. 0: disable interrupt 1: enable interrupt

2.3.5. SYS_STS Register

Table 2-8 System Status Register (0x74, SYS_STS)

0x74, System Status Register, SYS_STS				
Bit		R/W	Default Value	Description
31	-	-	-	Reserved

0x74, System Status Register, SYS_STS				
Bit		R/W	Default Value	Description
30	UDIP	R	0	Status bit for the voltage dip. 0: not happened 1: happened
29	USWELL	R	0	Status bit for voltage swell. 0: not happened 1: happened
28	IBLC	R	0	Status bit for IB under-current. 0: not happened 1: happened
27	IBOC	R	0	Status bit for IB over-current. 0: not happened 1: happened
26	IALC	R	0	Status bit for IA under-current. 0: not happened 1: happened
25	IAOC	R	0	Status bit for IA over-current. 0: not happened 1: happened
24	ULV	R	0	Status bit for channel U under-voltage. 0: not happened 1: happened
23	UOV	R	0	Status bit for channel U over-voltage. 0: not happened 1: happened

0x74, System Status Register, SYS_STS				
Bit		R/W	Default Value	Description
22:20	RST_SOURCE	R	-	Status bit for reset. 1: power on reset 2: external reset 3: RX low-level voltage reset 4: software reset Others are reserved.
19	CRP_OUT2	R	0	Status bit for power-creep detection for energy accumulator 2. 0: start 1: power-creep
18	CRP_OUT1	R	0	Status bit for power-creep detection for energy accumulator 1. 0: start 1: power-creep
17	SBCREEP	R	-	Status bit for no-load detection for apparent power Channel B. 0: start 1: power-creep
16	QBCREEP	R	-	Status bit for power-creep detection for reactive power Channel B. 0: start 1: power-creep

0x74, System Status Register, SYS_STS				
Bit		R/W	Default Value	Description
15	PBCREEP	R	-	Status bit for power-creep detection for active power Channel B. 0: start 1: power-creep
14	SACREEP	R	-	Status bit for power-creep detection for apparent power Channel A. 0: start 1: power-creep
13	QACREEP	R	-	Status bit for power-creep detection for reactive power Channel A. 0: start 1: power-creep
12	PACREEP	R	-	Status bit for power-creep detection for active power Channel A. 0: start 1: power-creep
11	QBSIGN	R	0	Sign bit for reactive power Channel B. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
10	PBSIGN	R	0	Sign bit for active power Channel B. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative

0x74, System Status Register, SYS_STS				
Bit		R/W	Default Value	Description
9	QASIGN	R	0	Sign bit for reactive power Channel A. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
8	PASIGN	R	0	Sign bit for active power Channel A. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
7	-	-	-	Reserved
6	HSEFAIL	R	0	Status bit for CTI external input clock status. 0: normal 1: abnormal
5	BISTERR	R	0	Status bit for SRAM BIST. 0: SRAM BIST normal 1: SRAM BIST error
4	RAMINITIAL		0	Status bit for RAM initialization finished 0: failed 1: finished
3	PHSDONE		0	Status bit for Phase measurement finished 0: failed 1: finished

0x74, System Status Register, SYS_STS				
Bit		R/W	Default Value	Description
2	PD	R	0	Status bit for power down. When the power input (VDD) is lower than 2.8V (±7%), power down event happens. 0: VDD >= 2.8V (±7%) 1: VDD < 2.8V (±7%)
1	REFLK	R	0	Status bit for the reference of ADC whether electric leaking. 0: ADC reference circuit normal 1: ADC reference circuit decrease is greater than 2.5%.
0	CHECKSUM	R	1	Status bit for Checksum. Checksum calculation address range: 0x0 ~ 0x7, 0x25 ~ 0x3A, 0x55 ~ 0x60 0: checksum correct 1: checksum incorrect

2.3.6. SYS_MISC Register

Table 2-9 System Control Register (0x75, SYS_MISC)

0x75, system Control Register, SYS_MISC				
Bit		R/W	Default Value	Description
31:25	Reserved	R	0	These bits must hold its default value for proper operation.
24:16	WAVE_STORE_CNT	R	0	Count value for Waveform storage.
15:6	Reserved		0	These bits must hold its default value for proper operation.
5	BIST_EGY_EN	R/W	0	When RAM self-test has error, force the energy

0x75, system Control Register, SYS_MISC				
Bit		R/W	Default Value	Description
				accumulator and CF output to disable. 0: enable 1: disable The control bits for the energy accumulator and CF counter (Bit[15] and Bit[7:6]) in DSP_CTRL1 register will not change. Although the DSP_CTRL1 register value has not changed, the energy accumulator and CF output functions will not be restored automatically and need to be opened manually by the user after the state returns to normal.
4	CK_EGY_EN	R/W	0	When checksum has error, force the energy accumulator and CF output to disable. 0: enable 1: disable The control bits for the energy accumulator and CF counter (Bit[15] and Bit[7:6]) in DSP_CTRL1 register will not change. Although the DSP_CTRL1 register value has not changed, the energy accumulator and CF output functions will not be restored automatically and need to be opened manually by the user after the state returns to normal.
3	PD_EGY_EN	R/W	0	When power-down, force the energy accumulator and CF output to disable. 0: enable

0x75, system Control Register, SYS_MISC				
Bit		R/W	Default Value	Description
				1: disable The control bits for the energy accumulator and CF counter (Bit[15] and Bit[7:6]) in DSP_CTRL1 register will not change. Although the DSP_CTRL1 register value has not changed, the energy accumulator and CF output functions will not be restored automatically and need to be opened manually by the user after the state returns to normal.
2	INTPOL	R/W	0	Reverse output on Interrupted pin. 0: interrupt pin triggered by high-level voltage, and default is low-level voltage. 1: interrupt pin triggered by low-level voltage, and default is high-level voltage.
1	UARTBURSTEN	R/W	0	To enable the UART continue writing mode. 0: enable 1: disable
0	UARTAUTOEN	R/W	0	To enable baud rate self-adapting for UART. It suggests enabling before changing system CLK. 0: disable Baud rate self-adapting function. Baud rate self-adapting only for first time communication. 1: enable Baud rate self-adapting function. Baud rate self-adapting for every time communication.

2.3.7. SYS_BLKX Register

Table 2-10 Block-reading Address Register 0 (0x79, SYS_BLK0_ADDR)

0x79, Block-reading Address Register 0, SYS_BLK0_ADDR				
Bit		R/W	Default Value	Description
31:24	ADDR3	R/W	0	Block-reading address 3.
23:16	ADDR2	R/W	0	Block-reading address 2.
15:8	ADDR1	R/W	0	Block-reading address 1.
7:0	ADDR0	R/W	0	Block-reading address 0.

Table 2-11 Block-reading Address Register 1 (0x7A, SYS_BLK1_ADDR)

0x7A, Block-reading Address Register 1, SYS_BLK1_ADDR				
Bit		R/W	Default Value	Description
31:24	ADDR7	R/W	0	Block-reading address 7.
23:16	ADDR6	R/W	0	Block-reading address 6.
15:8	ADDR5	R/W	0	Block-reading address 5.
7:0	ADDR4	R/W	0	Block-reading address 4.

Table 2-12 Block-reading Address Register 2 (0x7B, SYS_BLK2_ADDR)

0x7B, Block-reading Address Register 2, SYS_BLK2_ADDR				
Bit		R/W	Default Value	Description
31:24	ADDR11	R/W	0	Block-reading address 11.
23:16	ADDR10	R/W	0	Block-reading address 10.
15:8	ADDR9	R/W	0	Block-reading address 9.
7:0	ADDR8	R/W	0	Block-reading address 8.

Table 2-13 Block-reading Address Register 3 (0x7C, SYS_BLK3_ADDR)

0x7C, Block-reading Address Register 3, SYS_BLK3_ADDR				
Bit		R/W	Default Value	Description
31:24	ADDR15	R/W	0	Block-reading address 15.
23:16	ADDR14	R/W	0	Block-reading address 14.
15:8	ADDR13	R/W	0	Block-reading address 13.
7:0	ADDR12	R/W	0	Block-reading address 12.

2.3.8. SYS_IOCFGXX Register

Table 2-14 IO Configuration Register 0 (0x7D, SYS_IOCFGX0)

0x7D, IO Configuration Register 0, SYS_IOCFGX0				
Bit		R/W	Default Value	Description
31:24	P3CFG	R/W	0	Configuration as the same as P0CFG.
23:16	P2CFG	R/W	0	Configuration as the same as P0CFG.
15:8	P1CFG	R/W	0	Configuration as the same as P0CFG.
7:0	P0CFG	R/W	0	Bit[7:6]: 00: as shown in the Table 2-15, it can be configured the different combination interruption. 10: CF1 output. Bit[5:0] can be configured arbitrary value. 01: CF2 output. Bit[5:0] can be configured arbitrary value. 11: Actively energy accumulation data uploads. Bit[5:0] can be configured arbitrary value.

Table 2-15 P0CFG Bit[5:0] Description

Bit[5:3]	Bit[2:0]	
0	0	High impedance.

0	1	Current zero-crossing interruption.
0	2	Voltage zero-crossing interruption.
0	3	Current zero-crossing interruption.
0	4	Voltage zero-crossing interruption.
0	5	High speed energy accumulator 1 overflow interrupt
0	6	High speed energy accumulator 2 overflow interrupt
0	7	1st type interruption.
1	0	Waveform refresh interruption.
1	1	Instantaneous RMS refresh interruption.
1	2	Average RMS refresh interruption.
1	3	Instantaneous power refresh interruption.
1	4	Average power refresh interruption.
1	5	Waveform storage finish interruption.
1	6	Waveform storage address overflow interruption.
1	7	Waveform data upload finish interruption.
2	0	IB channel under-current interruption.
2	1	IB channel over-current interruption.
2	2	IA channel under-current interruption.
2	3	IA channel over-current interruption.
2	4	Voltage Channel under-voltage interruption.
2	5	Voltage Channel over-voltage interruption.
2	6	Voltage dip interruption.
2	7	Voltage swell interruption.

3	0	Reference error.
3	1	CTI external input clock error.
3	2	SPI communication error interruption.
3	3	UART communication error interruption.
3	4	Power-down interruption.
3	5	Parameter self-checking error interruption.
3	6	Phase test finish interruption.
3	7	RAM self-checking error.
4	0	1st type interruption.
4	1	2nd type interruption.
4	2	3rd type interruption.
4	others	4th type interruption.
5	0	3rd type interruption.
5	1	1st and 2nd type interruption.
5	2	1st and 3rd type interruption.
5	3	1st and 4th type interruption.
5	4	2nd and 3rd type interruption.
5	5	2nd and 4th type interruption.
5	6	3rd and 4th type interruption.
5	7	All interruption.
6	0	1st, 2nd and 3rd type interruption.
6	1	1st, 2nd and 4th type interruption.
6	2	1st, 3rd and 4th type interruption.

6	3	2nd, 3rd and 4th type interruption.
6	others	All interruption.
7	1	Active waveform updating for chip select of SPI, SPIMAS_SPCSN.
7	2	Active waveform updating for SPI clock, SPIMAS_SPCK.
7	4	Active waveform updating for SPI data, SPIMAS_SPDO.
7	others	Prohibited output.

While the IO interface is not configured (i.e. all zero), output is high impedance.

- 1st type interruption: current zero-crossing interruption, voltage zero-crossing interruption, high-speed energy accumulator 1/2 overflow interruption.
- 2nd type interruption: waveform refreshes interruption, instantaneous RMS refresh interruption, average RMS refreshes interruption, instantaneous power value refresh interruption, average power value refreshes interruption, waveform storage finish interruption, waveform storage overflow interruption and waveform data upload finished interruption.
- 3rd type interruption: IB channel under-current interruption, IB channel over-current interruption, IA channel under-current interruption, IA channel over-current interruption, voltage channel under-voltage interruption, voltage channel over-voltage interruption, voltage dip interruption and voltage swell interruption.
- 4th type interruption: SPI communicating error interruption, UART communicating error interruption, parameters self-checking error interruption, phase measurement finished interruption, power-down interruption, reference error interruption, CTI external input clock error interruption and RAM self-checking error interruption.

Table 2-16 IO Configuration Register 1 (0x7E, SYS_IOCFGX1)

0x7E, IO Configuration Register 1, SYS_IOCFGX1				
Bit		R/W	Default Value	Description
31:24	Reserved		0	These bits must hold its default value for proper operation.
23:16	P6CFG	R/W	0	Configuration as the same as P0CFG.

0x7E, IO Configuration Register 1, SYS_IOCFGX1				
Bit		R/W	Default Value	Description
15:8	P5CFG	R/W	0	Configuration as the same as P0CFG.
7:0	P4CFG	R/W	0	Configuration as the same as P0CFG.

2.3.9. SYS_VERSION Register

Table 2-17 Version Information Register (0x7F, SYS_VERSION)

0x7F, Version Information Register, SYS_VERSION				
Bit		R/W	Default Value	Description
31:0	VERSION	R	-	Present hardware version.

2.4. Metering Control Registers

When power-on reset (POR), RSTN pin reset, RX reset, or global software reset occurs, all metering control registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

All the metering control registers need to be configuration verification and self-checking.

2.4.1. DSP_CTRL0 Register

Table 2-18 Metering Control Register 0 (0x02, DSP_CTRL0)

0x02, R/W, Metering Control Register 0, DSP_CTRL0				
Bit		R/W	Default Value	Description
31	CURDAT_RATE	R/W	0	Double refresh time for Instantaneous power value and RMS value. 0: refresh time for instantaneous power value is 20 ms and instantaneous RMS value is 10 ms. 1: refresh time for instantaneous power value is 40

0x02, R/W, Metering Control Register 0, DSP_CTRL0				
Bit		R/W	Default Value	Description
				ms and instantaneous RMS value is 20 ms.
30	Reserved		0	The bit must hold its default value for proper operation.
29:28	FRQ_SEL	R/W	0	Source comes from the register value of DSP_DAT_FRQ. 00: accumulation value for line frequency test value of 16 cycles (the default update time is 320 ms) 01: line frequency test value of 1 cycle (the default update time is 20 ms) 10: line frequency test value of 64 cycles (the default update time is 1280 ms) 11: Reserved
27	DC_METER_MODE	R/W	0	To enable the DC metering mode. 0: disable 1: enable
26: 25	-	-	0	The bit must hold its default value for proper operation.
24	S_MODE	R/W	0	Source select for Apparent power calculation. 0: by RMS value 1: by power value
23:20	CFG_CHANNEL	R/W	0	Fundamental Channel selectable. 0: channel 1, fundamental active power A; channel 2, fundamental active power B 1: channel 1, fundamental active power A; channel

0x02, R/W, Metering Control Register 0, DSP_CTRL0				
Bit		R/W	Default Value	Description
				2, fundamental voltage RMS 2: channel 1, fundamental active power A; channel 2, fundamental current RMS A 3: channel 1, fundamental active power A; channel 2, fundamental current RMS B 4: channel 1, fundamental active power B, channel 2, fundamental voltage RMS 5: channel 1, fundamental active power B; channel 2, fundamental current RMS A 6: channel 1, fundamental active power B; channel 2, fundamental current RMS B 7: channel 1, fundamental voltage RMS; channel 2, fundamental current RMS A 8: channel 1, fundamental voltage RMS, channel 2, fundamental current RMS B 9: channel 1, fundamental current RMS A; channel 2, fundamental current RMS B 10~15: the same as configured 0
19	QB_MODE	R/W	0	To select mode for Reactive power B. 0: total wave, reactive power 1: fundamental wave, reactive power
18	QA_MODE	R/W	0	To select mode for Reactive power A. 0: total wave, reactive power 1: fundamental wave, reactive power

0x02, R/W, Metering Control Register 0, DSP_CTRL0				
Bit		R/W	Default Value	Description
17	PQ_HPFSEL	R/W	0	Calculate the total power whether pass high-pass filter. 0: pass 1: not pass
16	FUND_HPFSEL	R/W	0	Calculate the fundamental data whether pass high-pass filter: 0: pass 1: not pass
15	RMSU_HPFSEL	R/W	0	Calculate the total voltage RMS data whether pass high-pass filter: 0: pass 1: not pass
14	RMSIA_HPFSEL	R/W	0	Calculate the total current IA RMS data whether pass high-pass filter: 0: pass 1: not pass
13	RMSIB_HPFSEL	R/W	0	Calculate current IB RMS data whether pass high-pass filter: 0: pass 1: not pass
12	RESPONSE_TIME	R/W	0	Metering data response time. 0: normal 1: 2 times

0x02, R/W, Metering Control Register 0, DSP_CTRL0				
Bit		R/W	Default Value	Description
11:10	AVGRMS_RATE	R/W	0	Average RMS refresh time. 00: 40 ms 01: 80 ms 10: 320 ms 11: 640 ms
9:8	AVGPQ_RATE	R/W	0	Average power refresh time. 00: 40 ms 01: 80 ms 10: 320 ms 11: 640 ms
7:4	DSP_MODE	R/W	0	DSP Operating Mode. 0: 128 sampling points per cycle by DSP at 6.5536 MHz system clock 1: 64 sampling points per cycle by DSP at 6.5536 MHz system clock 2: 32 sampling points per cycle by DSP at 6.5536 MHz system clock. 3, 4, and 5: Reserved. 6: 64 sampling points per cycle by DSP at 3.2768 MHz system clock 7: 32 sampling points per cycle by DSP at 3.2768 MHz system clock 8: 32 sampling points per cycle by DSP at 819.2 KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) 9: 16 sampling points per cycle by DSP at 409.6

0x02, R/W, Metering Control Register 0, DSP_CTRL0				
Bit		R/W	Default Value	Description
				KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) Others: the same as mode 0
3	-	-	0	Reserved
2	ADCUEN	R/W	0	To enable the voltage channel (including ADC and DSP).
1	ADCIBEN	R/W	0	To enable the current channel B (including ADC and DSP).
0	ADCIAEN	R/W	0	To enable the current channel A (including ADC and DSP).

2.4.2. DSP_CTRL1 Register

Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)

0x03, R/W, Metering Control Register 2, DSP_CTRL1				
Bit		R/W	Default Value	Description
31	BW_COMP	R/W	0	Automatic gain compensation for filter. By default, this function was enabled. This bit does not influence DC metering. It will automatic turn off during the DC metering. 0: enable 1: disable
30:22	Reserved		0	The bit must hold its default value for proper operation.
23	EGY_CLK_SEL	R/W	0	To select the energy accumulator CLK. It needs the stable time around 107 μs when CLK switch over. Please disable CF before it is stable.

0x03, R/W, Metering Control Register 2, DSP_CTRL1				
Bit		R/W	Default Value	Description
				0: 204.8 KHz 1: 32.768 KHz
22	LCF_ACC	R/W	0	0: disable To write "0" into the bit31 of the DSP_CTRL0 the accumulating cycle of energy accumulator 3, 4, 5, 6, 7, and 8 is 20ms. To write "1" into the bit31 of the DSP_CTRL0, the accumulating cycle of energy accumulator 3, 4, 5, 6, 7, and 8 is 40 ms. 1: enable To write "0" into the bit31 of the DSP_CTRL0, the accumulating cycle of energy accumulator 3, 4, and 5 is 10 ms. Energy accumulator 6, 7, and 8 not accumulate. To write "1" into the bit31 of the DSP_CTRL0, the accumulating cycle of energy accumulator 3, 4, and 5 is 20 ms. Energy accumulator 6, 7, and 8 not accumulate.
21	PGA_U	R/W	0	Voltage channel digital PGA: 0: X1 1: X4
20	PHSI_SEL	R/W	0	To select the input source for current zero-crossing. 0: current channel IA 1: current channel IB
19:18	SIGN_SEL	R/W	0	To select the detect method of zero-crossing: 0: negative direction (it indicates the signal changing from positive to negative is occurring a zero-crossing event) 1: positive direction (it indicates the signal changing

0x03, R/W, Metering Control Register 2, DSP_CTRL1				
Bit		R/W	Default Value	Description
				from negative to positive is occurring a zero-crossing event) 2: positive and negative direction 3: disable the zero-crossing detection function
17	AUTO_BAUD	R/W	0	Actively power accumulating data uploads, the upload interface can pass SYS_IOCFGX P0/ P1/ P2/ P3/ P4/ P5/ P6 pin configuration as the actively data uploads. Can use communicating methods to configure UART baud rate. 0: When UART communicates, baud rate is the same as last time serial communication. The baud rate when SPI communication is 4800. 1: When UART communicates, baud rate is as much again of last time serial communication. The baud rate when SPI communication is 9600.
16	AUTO_TX_EN	R/W	0	To enable the active power accumulating data uploads. 0: disable 1: enable
15	EGY_LC_EN	R/W	0	To enable the low-speed energy accumulator and CF counter. The accumulating speed of low-speed energy accumulator is 50 Hz. 0: disable 1: enable.
14	CF2_INV	R/W	0	To control the CF2 polarity. 0: original polarity 1: reverse polarity
13	CF2_EN	R/W	0	To Enable the CF2 output. 0: disable 1: enable.

0x03, R/W, Metering Control Register 2, DSP_CTRL1				
Bit		R/W	Default Value	Description
12	CF2_SEL	R/W	0	To select the input source of CF2. 0: from the energy accumulator 1 1: from the energy accumulator 2
11	Reserved		0	The bit must hold its default value for proper operation.
10	CF1_INV	R/W	0	To control CF1 polarity. 0: original polarity 1: reverse polarity
9	CF1_EN	R/W	0	To enable CF1 output. 0: disable CF1 output 1: enable CF1 output
8	CF1_SEL	R/W	0	To select the input source of CF1. 0: from the energy accumulator 1 1: from the energy accumulator 2
7	CALCEN2	R/W	0	To enable the energy accumulator 2 and CF2 counter. The accumulating speed of energy accumulator 2 is 204.8 KHz. 0: disable 1: enable.
6	CALCEN1	R/W	0	To enable the energy accumulator 1 and CF1 counter. The accumulating speed of energy accumulator 1 is 204.8 KHz. 0: disable 1: enable
5:4	CF_PULSE	R/W	0	To select the CF pulse width 0: 80 ms 1: 40 ms 2: 20 ms 3: 10 ms

0x03, R/W, Metering Control Register 2, DSP_CTRL1				
Bit		R/W	Default Value	Description
3:2	CF_FAST_EN	R/W	0	CF pulse speed up output. 0: Normal mode 1: 4x faster 2: 8x faster 3: 16x faster
1	PWR_CRP_EN	R/W	0	To determine the power of power-creep. The power-creep determination uses continuous 3 average and threshold compare. If lower the threshold, then here will be the power-creep status. 0: disable the power-creep detection 1: enable the power-creep detection
0	CRP_EN	R/W	0	To enable the High-speed energy accumulator. 0: disable the power-creep detection 1: enable the power-creep detection

2.4.3. DSP_CTRL2 Register

Table 2-20 Metering Control Register 2 (0x04, DSP_CTRL2)

0x04, R/W, Metering Control Register 2, DSP_CTRL2				
Bit		R/W	Default Value	Description
31:30	INMODE4	R/W	0	The energy accumulator 4 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable fundamental-wave channel accumulation
29	A_SEL4	R/W	0	To enable the energy accumulator 4, channel A

0x04, R/W, Metering Control Register 2, DSP_CTRL2				
Bit		R/W	Default Value	Description
				accumulating. 0: disable 1: enable
28	B_SEL4	R/W	0	To enable the energy accumulator 4, channel B accumulating. 0: disable 1: enable
27:26	TYPE_SEL4	R/W	0	The energy accumulator 4, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, high bit zero represents accumulating sum; High bit one represents accumulating difference.
25:24	PROCMODE4	R/W	0	For each signal type choices which feed into the energy accumulator 4. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
23:22	INMODE3	R/W	0	The energy accumulator 3 accumulation mode 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel

0x04, R/W, Metering Control Register 2, DSP_CTRL2				
Bit		R/W	Default Value	Description
				accumulation
21	A_SEL3	R/W	0	To enable the energy accumulator 3, channel A accumulating. 0: disable; 1: enable
20	B_SEL3	R/W	0	To enable the energy accumulator 3, channel B accumulating. 0: disable 1: enable
19:18	TYPE_SEL3	R/W	0	The energy accumulator 3, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
17:16	PROCMODE3	R/W	0	For each signal type choices which feed into the energy accumulator 3. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
15:14	INMODE2	R/W	0	The energy accumulator 2 accumulating mode. 0: power accumulation 1: current RMS accumulation

0x04, R/W, Metering Control Register 2, DSP_CTRL2				
Bit		R/W	Default Value	Description
				2: constant accumulation 3: configurable the fundamental wave channel accumulation
13	A_SEL2	R/W	0	To enable the energy accumulator 2, channel A accumulating. 0: disable 1: enable
12	B_SEL2	R/W	0	To enable the energy accumulator 2, channel B accumulating. 0: disable 1: enable
11:10	TYPE_SEL2	R/W		The energy accumulator 2, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
9:8	PROCMODE2	R/W	0	For each signal type choices which feed into the energy accumulator 2. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
7:6	INMODE1	R/W	0	The energy accumulator 1 accumulating mode.

0x04, R/W, Metering Control Register 2, DSP_CTRL2				
Bit		R/W	Default Value	Description
				0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
5	A_SEL1	R/W	0	To enable the energy accumulator 1, channel A accumulating. 0: disable 1: enable
4	B_SEL1	R/W	0	To enable the energy accumulator 1, channel B accumulating. 0: disable 1: enable
3:2	TYPE_SEL1	R/W	0	Multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
1:0	PROCMODE1	R/W	0	For each signal type choices which feed into the energy accumulator 1. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding

2.4.4. DSP_CTRL3 Register

Table 2-21 Metering Control Register 3 (0x05, DSP_CTRL3)

0x05, R/W, Metering Control Register 3, DSP_CTRL3				
Bit		R/W	Default Value	Description
31:30	INMODE8	R/W	0	The energy accumulator 8 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
29	A_SEL8	R/W	0	To enable the energy accumulator 8, channel A accumulating. 0: disable 1: enable
28	B_SEL8	R/W	0	To enable the energy accumulator 8, channel B accumulating. 0: disable 1: enable
27:26	TYPE_SEL8	R/W	0	The energy accumulator 8, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
25:24	PROCMODE8	R/W	0	For each signal type choices which feed into the energy accumulator 8. 0: the positive value of the energy accumulator adding

0x05, R/W, Metering Control Register 3, DSP_CTRL3				
Bit		R/W	Default Value	Description
				1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
23:22	INMODE7	R/W	0	The energy accumulator 7 accumulating mode 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
21	A_SEL7	R/W	0	To enable the energy accumulator 7, channel A accumulating 0: disable 1: enable
20	B_SEL7	R/W	0	To enable the energy accumulator 7, channel B accumulating 0: disable 1: enable
19:18	TYPE_SEL7	R/W	0	The energy accumulator 7, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
17:16	PROCMODE7	R/W	0	For each signal type choices which feed into the energy

0x05, R/W, Metering Control Register 3, DSP_CTRL3				
Bit		R/W	Default Value	Description
				accumulator 7. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
15:14	INMODE6	R/W	0	The energy accumulator 6 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
13	A_SEL6	R/W	0	To enable the energy accumulator 6, channel A accumulating. 0: disable 1: enable
12	B_SEL6	R/W	0	To enable the energy accumulator 6, channel B accumulating. 0: disable 1: enable
11:10	TYPE_SEL6	R/W		The energy accumulator 6, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one

0x05, R/W, Metering Control Register 3, DSP_CTRL3				
Bit		R/W	Default Value	Description
				represents accumulating difference.
9:8	PROCMODE6	R/W	0	For each signal type choices which feed into the energy accumulator 6. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
7:6	INMODE5	R/W	0	The energy accumulator 5 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
5	A_SEL5	R/W	0	To enable the energy accumulator 5, channel A accumulating. 0: disable 1: enable
4	B_SEL5	R/W	0	To enable the energy accumulator 5, channel B accumulating. 0: disable 1: enable
3:2	TYPE_SEL5	R/W	0	The energy accumulator 5, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation

0x05, R/W, Metering Control Register 3, DSP_CTRL3				
Bit		R/W	Default Value	Description
				When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
1:0	PROCMODE5	R/W	0	For each signal type choices which feed into the energy accumulator 5. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding

2.4.5. DSP_CTRL4 Register

Table 2-22 Metering Control Register 4 (0x06, DSP_CTRL4)

0x06, R/W, Metering Control Register 4, DSP_CTRL4				
Bit		R/W	Default Value	Description
31:30	IPERIOD	R/W	0	To select the detection time of over-current or under-current. When the number of sampling points of over-current or under-current in the sampling points during the half-cycle is greater than or equal to the ITH value, it will be considered as the effective half-cycle. If the number of consecutive effective half-cycle reaches the value set by IPERIOD, it will be considered as this event happened. 0: half cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles

0x06, R/W, Metering Control Register 4, DSP_CTRL4				
Bit		R/W	Default Value	Description
29:24	ITH	R/W	0	To determine the threshold of half-cycle is effective half-cycle. 0: 1 time 1: 2 times … 63: 64 times
23:22	UPERIOD	R/W	0	The same as IPERIOD configurable conditions. 0: half cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles
21:16	UTH	R/W	0	The same as ITH configurable conditions. 0: 1 time 1: 2 times … 63: 64 times
15:10	Reserved			These bits must hold its default value for proper operation.
9	IBLCSEL	R/W	0	IB under- current test source. 0: no pass IB wave data of high pass filter 1: pass IB wave data of high pass filter
8	IBOCSEL	R/W	0	IB: over-current test source. 0: no pass IB wave data of high pass filter 1: pass IB wave data of high pass filter
7	IALCSEL	R/W	0	IA under-current test source. 0: no pass IA wave data of high pass filter 1: pass IA wave data of high pass filter

0x06, R/W, Metering Control Register 4, DSP_CTRL4				
Bit		R/W	Default Value	Description
6	IAOCSEL	R/W	0	IA over-current test source. 0: no pass IA wave data of high pass filter 1: pass IA wave data of high pass filter
5	ULVSEL	R/W	0	Channel U under-voltage test source. 0: no pass channel U wave data of high pass filter 1: pass channel U wave data of high pass filter
4	UOVSEL	R/W	0	Channel U over-voltage test source. 0: no pass channel U wave data of high pass filter 1: pass channel U wave data of high pass filter
3	Reserved		0	The bit must hold its default value for proper operation.
2	FDIBEN	R/W	0	To enable the fast detection for IB. 0: disable IB over or under current test 1: enable IB over or under current test
1	FDIAEN	R/W	0	To enable the fast detection for IA. 0: disable IA over or under current test 1: enable IA over or under current test
0	FDUEN	R/W	0	To enable the fast detection. 0: disable channel U over or under voltage test 1: enable channel U over or under voltage test

2.4.6. DSP_CTRL5 Register

Table 2-23 Metering Control Register 5 (0x07, DSP_CTRL5)

0x07, R/W, Metering Control Register 5, DSP_CTRL5				
Bit		R/W	Default Value	Description
31	WAVE_ADDR_CLR	R/W	0	Reset reading the address of waveform storage, write 1 to reset.
30:29	WAVE_MEM_MODE	R/W	0	The operating mode of waveform storage: 0: storage by manual, full then stop. This time is the single storage. 1: storage by manual, trigger or manual stop. This time is the cyclic storage. 2: storage by trigger, full then stop. This time is the single storage. 3: disable
28	WAVE_MEM_EN	R/W	0	Waveform storage to trigger manual switch: write 1 = enable, write 0 = disable 0: disable 1: enable
27	U_DIP_TRIG	R/W	0	Event trigger for the voltage dip. 0: disable 1: enable
26	U_SWELL_TRIG	R/W	0	Event trigger for the voltage swell. 0: disable 1: enable
25	IB_LC_TRIG	R/W	0	Event trigger for the IB under-current. 0: disable 1: enable
24	IB_OC_TRIG	R/W	0	Event trigger for the IB over-current. 0: disable 1: enable
23	IA_LC_TRIG	R/W	0	Event trigger for the IA under-current. 0: disable 1: enable

0x07, R/W, Metering Control Register 5, DSP_CTRL5				
Bit		R/W	Default Value	Description
22	IA_OC_TRIG	R/W	0	Event trigger for the IA over-current. 0: disable 1: enable
21	U_LV_TRIG	R/W	0	Event trigger for Under-voltage. 0: disable 1: enable
20	U_OV_TRIG	R/W	0	Event trigger for Over-voltage. 0: disable 1: enable
19:16	WAVE_LENGTH	R/W	0	To select output waveform length of DMA channel. 0: 1 cycle 1: 2 cycles 2: 3 cycles …… 15: 16 cycles
15	Reserved	-	-	The bit must hold its default value for proper operation.
14	WAVE_U_HPF_SEL	R/W	0	Voltage waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
13	WAVE_IA_HPF_SEL	R/W	0	Current IA waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter

0x07, R/W, Metering Control Register 5, DSP_CTRL5				
Bit		R/W	Default Value	Description
12	WAVE_IB_HPF_SEL	R/W	0	Current IB waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
11	Reserved	-	-	The bit must hold its default value for proper operation.
10	WAVE_U_SEL	R/W	0	To enable the waveform storage and DMA of channel U. The bit decides whether storage or transmit data of channel U: 0: no 1: yes
9	WAVE_IA_SEL	R/W	0	To Enable the waveform storage and DMA of channel IA. The bit decides whether storage or transmit data of channel IA: 0: no 1: yes
8	WAVE_IB_SEL	R/W	0	To enable the waveform storage and DMA of channel IB. The bit decides whether storage or transmit data of channel IB (If waveform storage and configure bit 8, bit 9, and bit 10 enable at the same time, the bit becomes invalid): 0: no 1: yes
7	SP_CHECK	R/W	0	DMA mode parity check choice: 0: odd parity 1: even parity
6	SPI_POL	R/W	0	DMA mode polarity choice: 0: negative 1: positive

0x07, R/W, Metering Control Register 5, DSP_CTRL5				
Bit		R/W	Default Value	Description
5	SPI_PHA	R/W	0	DMA mode phase choice: 0: negative 1: positive
4:3	DMA_MANUALCTRL	R/W	0	DMA channel choice: 0: disable 1: enable by manual 2: stop by manual 3: reserved
2:0	DMA_MODE	R/W	0	DMA channel operating mode: 0: transmit starting by manual, until maximum cycle then stops. 1: transmit starting by manual, trigger or by manual stop. 2: trigger starting, stop by manual. 3: trigger starting, until maximum cycle then stops. 4~7: transmit by manual, stop by manual. Before enabling DMA transmission, at least one channel of waveform storage and upload must be opened.

2.5. Metering Data Register

When power-on reset (POR), RSTN pin reset, RX reset, or global software reset occurs, all metering control registers will be reset to the default value.

2.5.1. DC Component Register

Table 2-24 DC Component Register

Address	Register	R/W	Data Format	Description	
0x22	DSP_DAT_DCU	R	32-bit Complement Code	DC value of voltage channel.	By default, the updating time is 40 ms; stable time is 120 ms.
0x23	DSP_DAT_DCI	R	32-bit Complement Code	DC value of current channel A.	
0x24	DSP_DAT_DCIB	R	32-bit Complement Code	DC value of Current channel B.	

2.5.2. RMS Register

Table 2-25 Voltage/ Current/ Measurement Signal (M) RMS Register

Address	Register	R/W	Data Format	Description	
0x0E	DSP_DAT_RMS0U	R	32-bit Complement Code	Instantaneous RMS of voltage.	By default, the updating time is 10 ms; stable time is 30 ms.
0x0F	DSP_DAT_RMS0IA	R	32-bit Complement Code	Instantaneous RMS of current A.	
0x10	DSP_DAT_RMS0IB	R	32-bit Complement Code	Instantaneous RMS of current B.	
0x19	DSP_DAT_RMS1U	R	32-bit Complement Code	Average RMS of voltage.	Under the default state, the updating time is 40 ms; stable time is 120 ms.
0x1A	DSP_DAT_RMS1IA	R	32-bit Complement Code	Average RMS of Current A.	
0x1B	DSP_DAT_RMS1IB	R	32-bit Complement Code	Average RMS of Current B.	

Address	Register	R/W	Data Format	Description	
0x1E	DSP_DAT_RMSU_AVG	R	32-bit Complement Code	Average RMS of Voltage for 10 or 12 cycles (chose by line frequency.)	
0x1F	DSP_DAT_RMSIA_AVG	R	32-bit Complement Code	Average RMS of Current IA for 10 or 12 cycles (chose by line frequency.)	
0x20	DSP_DAT_RMSIB_AVG	R	32-bit Complement Code	Average RMS of Current IB for 10 or 12 cycles (chose by line frequency.)	

2.5.3. Active/ Reactive Power Register

Table 2-26 Active/ Reactive Power Register

Address	Register	R/W	Data Format	Description	
0x08	DSP_DAT_PA	R	32-bit Complement Code	Instantaneous Active Power of channel A.	By default, the updating time is 20 ms; stable time is 60 ms.
0x09	DSP_DAT_QA	R	32-bit Complement Code	Instantaneous Reactive Power of channel A.	
0x0A	DSP_DAT_SA	R	32-bit Complement Code	Instantaneous Apparent Power of channel A.	
0x0B	DSP_DAT_PB	R	32-bit Complement Code	Instantaneous Active Power of channel B.	

Address	Register	R/W	Data Format	Description	
0x0C	DSP_DAT_QB	R	32-bit Complement Code	Instantaneous Reactive Power of channel B.	
0x0D	DSP_DAT_SB	R	32-bit Complement Code	Instantaneous Apparent Power of channel B.	
0x13	DSP_DAT_PA1	R	32-bit Complement Code	Average Active power of Channel A.	By default, the updating time is 80 ms; stable time is 240 ms.
0x14	DSP_DAT_QA1	R	32-bit Complement Code	Average Reactive power of Channel A.	
0x15	DSP_DAT_SA1	R	32-bit Complement Code	Average Apparent Power of Channel A.	
0x16	DSP_DAT_PB1	R	32-bit Complement Code	Average Active power of Channel B.	
0x17	DSP_DAT_QB1	R	32-bit Complement Code	Average Reactive power of Channel B.	
0x18	DSP_DAT_SB1	R	32-bit Complement Code	Average Apparent Power of Channel B.	

2.5.4. Fundamental Wave Channel Register

Table 2-27 Fundamental Wave Channel Instantaneous Register

Address	Register	R/W	Data Format	Description
0x11	DSP_DAT_CH1	R	32-bit Complement Code	Instantaneous value of Fundamental wave of Channel 1.
0x12	DSP_DAT_CH2	R	32-bit Complement Code	Instantaneous value of Fundamental wave of Channel 2.

Table 2-28 Fundamental Wave Channel Average Register

Address	Register	R/W	Data Format	Description
0x1C	DSP_DAT_CH1_AVG	R	32-bit Complement Code	Average value of Fundamental wave of Channel 1.
0x1D	DSP_DAT_CH2_AVG	R	32-bit Complement Code	Average value of Fundamental wave of Channel 2.

2.5.5. Line Frequency Register

Table 2-29 Line Frequency Register (0x21, DSP_DAT_FRQ)

Address	Register	R/W	Data Format	Description
0x21	DSP_DAT_FRQ	R	32-bit Complement Code	Line frequency is related to FRQ_SEL. By default, the updating time is 320 ms; stable time is 640 ms.

2.6. Energy Accumulator Register

Table 2-30 Energy Accumulator Register

Address	Register	R/W	Data Format	Description
0x39	EGY_PROCTH	R	32-bit Unsigned	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.

Address	Register	R/W	Data Format	Description
0x3A	EGY_PWRTH	R/W	32-bit Unsigned	Accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.
0x3B	EGY_CONST1	R/W	32-bit Unsigned	Energy accumulator 1 accumulating constant.
0x3C	EGY_OUT1L	R/W	32-bit Unsigned	Energy accumulator 1 accumulating low bit.
0x3D	EGY_OUT1H	R/W	32-bit Unsigned	Energy accumulator 1 accumulating high bit Low 14bit effective.
0x3E	EGY_CFCNT1	R/W	32-bit Unsigned	Energy accumulator 1 pulse counter.
0x3F	EGY_CONST2	R	32-bit Unsigned	Energy accumulator 2 accumulating constant.
0x40	EGY_OUT2L	R/W	32-bit Unsigned	Energy accumulator 2 accumulating low bit.
0x41	EGY_OUT2H	R/W	32-bit Unsigned	Energy accumulator 2 accumulating high bit Low 14bit effective.
0x42	EGY_CFCNT2	R/W	32-bit Unsigned	Energy accumulator 2 pulse counter.
0x43	EGY_CONST3	R	32-bit Unsigned	Energy accumulator 3 accumulating constant.
0x44	EGY_OUT3	R/W	32-bit Unsigned	Energy accumulator 3 accumulating value.
0x45	EGY_CFCNT3	R/W	32-bit Unsigned	Energy accumulator 3 pulse counter.
0x46	EGY_CONST4	R	32-bit Unsigned	Energy accumulator 4 accumulating constant.
0x47	EGY_OUT4	R/W	32-bit Unsigned	Energy accumulator 4 accumulating value.
0x48	EGY_CFCNT4	R/W	32-bit Unsigned	Energy accumulator 4 pulse counter.
0x49	EGY_CONST5	R	32-bit Unsigned	Energy accumulator 5 accumulating constant.
0x4A	EGY_OUT5	R/W	32-bit Unsigned	Energy accumulator 5 accumulating value.
0x4B	EGY_CFCNT5	R/W	32-bit Unsigned	Energy accumulator 5 pulse counter.
0x4C	EGY_CONST6	R	32-bit Unsigned	Energy accumulator 6 accumulating constant.
0x4D	EGY_OUT6	R/W	32-bit Unsigned	Energy accumulator 6 accumulating value.
0x4E	EGY_CFCNT6	R/W	32-bit Unsigned	Energy accumulator 6 pulse counter.
0x4F	EGY_CONST7	R	32-bit Unsigned	Energy accumulator 7 accumulating constant.

Address	Register	R/W	Data Format	Description
0x50	EGY_OUT7	R/W	32-bit Unsigned	Energy accumulator 7 accumulating value.
0x51	EGY_CFCNT7	R/W	32-bit Unsigned	Energy accumulator 7 pulse counter.
0x52	EGY_CONST8	R	32-bit Unsigned	Energy accumulator 8 accumulating constant.
0x53	EGY_OUT8	R/W	32-bit Unsigned	Energy accumulator 8 accumulating value.
0x54	EGY_CFCNT8	R/W	32-bit Unsigned	Energy accumulator 8 pulse counter.

2.7. Phase Measurement Register

Table 2-31 Phase Measurement Register

Address	Register	R/W	Data Format	Description
0x61	DSP_PHS_STT	R/W	32-bit Unsigned	To control the phase measurement. Enable phase measurement once for writing operation.
0x62	DSP_PHS_U	R	32-bit Unsigned	Voltage Phase Value.
0x63	DSP_PHS_UN	R	32-bit Unsigned	The waveform data before voltage zero-crossing.
0x64	DSP_PHS_UP	R	32-bit Unsigned	The waveform data after voltage zero-crossing.
0x65	DSP_PHS_I	R	32-bit Unsigned	Current Phase Value.
0x66	DSP_PHS_IN	R	32-bit Unsigned	The waveform data before current zero-crossing.
0x67	DSP_PHS_IP	R	32-bit Unsigned	The waveform data after current zero-crossing.

2.8. Power-creep Threshold Register

Table 2-32 Power-creep Threshold Register

Address	Register	R/W	Data Format	Description
0x55	DSP_OV_THL	R/W	32-bit Complement Code	To set the lower threshold for the power creep detection for instantaneous active power/ reactive power/ apparent power of channel A and B.
0x56	DSP_OV_THH	R/W	32-bit Complement Code	To set the upper threshold for the power creep detection for instantaneous active power/ reactive power/ apparent power of channel A and B.

2.9. Voltage Swell or Dip Threshold Register

Table 2-33 Voltage Swell or Dip Threshold Register

Address	Register	R/W	Data Format	Description
0x57	DSP_SWELL_THL	R/W	32-bit Complement Code	To set the lower threshold for the voltage swell.
0x58	DSP_SWELL_THH	R/W	32-bit Complement Code	To set the upper threshold for the voltage swell.
0x59	DSP_DIP_THL	R/W	32-bit Complement Code	To set the lower threshold for the voltage dip.
0x5A	DSP_DIP_THH	R/W	32-bit Complement Code	To set the upper threshold for the voltage dip.
0x6A	DAT_SWELL_CNT	R/C	32-bit Complement Code	Times records of voltage swell, half wave as a unit. 24bit effective. When write in any value, can clear zero the counter value.
0x6B	DAT_DIP_CNT	R/C	32-bit Complement Code	Times records of voltage dip, half wave as a unit. 24bit effective. When write in any value, can clear zero the counter value.

2.10. Fast Detection Threshold Register

Table 2-34 Fast detection Threshold Register

Address	Register	R/W	Data Format	Description
0x5B	FD_OVTH	R/W	30-bit Complement Code	To set over-voltage threshold for fast detection. Bit width is 30bit.
0x5C	FD_LVTH	R/W	30-bit Complement Code	To set under-voltage threshold for fast detection. Bit width is 30bit.
0x5D	FD_IA_OCTH	R/W	30-bit Complement Code	To set over-current threshold in channel A for fast detection. Bit width is 30bit.
0x5E	FD_IA_LCTH	R/W	30-bit Complement Code	To set under-current threshold in channel A for fast detection. Bit width is 30bit.
0x5F	FD_IB_OCTH	R/W	30-bit Complement Code	To set over-current threshold in channel B for fast detection. Bit width is 30bit.
0x60	FD_IB_LCTH	R/W	30-bit Complement Code	To set under-current threshold in channel B for fast detection. Bit width is 30bit.

2.11. Waveform Data Register

Table 2-35 Waveform Data Register

Address	Register	R/W	Data Format	Description
0x69	DAT_WAVE	R	32-bit Complement Code	Waveform reading. It can repeatable reading the address and obtain the overall wave data. If there is no need to read all data, it would be reset the bit 31 of metering control register (0x07, DSP_CTRL5) to read address.

2.12. Calibration Register

When power-on reset (POR), RSTN pin reset, RX reset, or global software reset occurs, all calibration registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

All the calibration registers need to be configuration verification and self-checking.

2.12.1. DC Bias Setting Register

Table 2-36 DC Bias Setting Register

Address	Register	Default Value	R/W	Format Value	Description
0x34	DSP_CFG_DCU	0	R/W	32-bit Complement Code	To set the DC compensation for the voltage channel.
0x35	DSP_CFG_DCIA	0	R/W	32-bit Complement Code	To set the DC compensation for the current channel A.
0x36	DSP_CFG_DCIB	0	R/W	32-bit Complement Code	To set the DC compensation for the current channel B.
All registers for calibration need to be configuration verification and self-checking.					

2.12.2. RMS Calibration Register

Table 2-37 Voltage/ Current/ Measurement RMS Calibration Register

Address	Register	Default Value	R/W	Data Format	Description
0x2D	DSP_CFG_CALI_RMSU	0	R/W	32-bit Complement Code	To set gain calibration for Voltage RMS.
0x2E	DSP_CFG_RMS_DCU	0	R/W	32-bit Complement Code	To set offset calibration for Voltage RMS.

Address	Register	Default Value	R/W	Data Format	Description
0x2F	DSP_CFG_CALI_RMSIA	0	R/W	32-bit Complement Code	To set gain calibration for Current RMS A.
0x30	DSP_CFG_RMS_DCIA	0	R/W	32-bit Complement Code	To set offset calibration for Current RMS A.
0x31	DSP_CFG_CALI_RMSIB	0	R/W	32-bit Complement Code	To set gain calibration for Current RMS B.
0x32	DSP_CFG_RMS_DCIB	0	R/W	32-bit Complement Code	To set offset calibration for Current RMS.

2.12.3. Power Calibration Register

Table 2-38 Total-wave Active/ Reactive Power Calibration Register

Address	Register	Default Value	R/W	Data Format	Description
0x25	DSP_CFG_CALI_PA	0	R/W	32-bit Complement Code	To set gain calibration for the active power A.
0x26	DSP_CFG_DC_PA	0	R/W	32-bit Complement Code	To set offset calibration for the active power A.
0x27	DSP_CFG_CALI_QA	0	R/W	32-bit Complement Code	To set gain calibration for Reactive power A.
0x28	DSP_CFG_DC_QA	0	R/W	32-bit Complement Code	To set offset calibration for Reactive power A.
0x29	DSP_CFG_CALI_PB	0	R/W	32-bit Complement Code	To set gain calibration for Active power B.
0x2A	DSP_CFG_DC_PB	0	R/W	32-bit Complement Code	To set offset calibration for Active power B.

Address	Register	Default Value	R/W	Data Format	Description
0x2B	DSP_CFG_CALI_QB	0	R/W	32-bit Complement Code	To set gain calibration for Reactive power B.
0x2C	DSP_CFG_DC_QB	0	R/W	32-bit Complement Code	To set offset calibration for Reactive power B.

2.12.4. Threshold Register

Table 2-39 Threshold Register

Address	Register	Default Value	R/W	Data Format	Description
0x39	EGY_PROCTH	0	R/W	32-bit Complement Code	Energy accumulator anti-creep threshold. When anti-creep energy accumulator exceeds the EGY_CRPTH and high-speed energy accumulator not exceeds the EGY_PWRTH, the accumulating value of high-speed accumulator will be cleared. Metering chip has a power-creep energy accumulating register for energy accumulator 1 and 2 respectively, and they have the same accumulation speed. After enabling the power-creep detection in the energy accumulator, the input would be fixed to 1 in this power-creep energy accumulator. User should configure threshold for the power-creep detection register

Address	Register	Default Value	R/W	Data Format	Description
					(EGY_CRPTH) and energy accumulating threshold register (EGY_PWRTH). If the accumulating value of power-creep energy accumulator register reaches the value of EGY_CRPTH first, the energy accumulating register will be cleared, and system enter the power-creep status. When the accumulating value of energy accumulating register reaches the value of EGY_PWRTH first, the power-creep energy register will be cleared, system starts to work and operates normally. The actual bit width of register EGY_CRPTH is 32bit. The register contents will be padded with 0s automatically in the 4 least significant bits when the power-creep calculated. It would be calculated after extended to 36 digits.
0x3A	EGY_PWRTH	0	R/W	32-bit Complement Code	Accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.

Address	Register	Default Value	R/W	Data Format	Description
0x55	DSP_OV_THL	0	R/W	32-bit Complement Code	To set the lower threshold for the power-creep determination.
0x56	DSP_OV_THH	0	R/W	32-bit Complement Code	To set the upper threshold for the power-creep determination.

2.12.5. Phase Calibration Register

Table 2-40 Phase Calibration Register (0x33, DSP_CFG_PHC)

Address	Register	Default Value	R/W	Data Format	Description
0x33	DSP_CFG_PHC	0	R/W	32-bit Complement Code	Phase Error Calibration Register. The register needs to be configuration verification and self-checking. [10:0]= phase error calibration value for channel A; [26:16]= phase error calibration value for channel B; Where the range is from -766 to 767.

2.12.6. Bandpass Filter Register

Table 2-41 Bandpass Filter Register (0x37, DSP_CFG_BPF)

Address	Register	Default Value	R/W	Data Format	Description
0x37	DSP_CFG_BPF	0	R/W	32-bit Complement Code	Band-pass filter coefficient. Related to setting the DSP_MODE by Bit[7:4] of metering control register 0

Address	Register	Default Value	R/W	Data Format	Description
					(0x02,DSP_CTRL0) Setting 0x806764B6 at DSP_MODE=0, 1, 2; Setting 0x80DD7A8C at DSP_MODE=6, 7; Setting 0x82B465F0 at DSP_MODE=8. The frequency of other modes would be not supported to measure, so setting to 0x0.

2.13. Checksum Register

Table 2-42 Checksum Register (0x38, DSP_CFG_CKSUM)

Address	Register	Default Value	R/W	Data Format	Description
0x28	DSP_CFG_CKSUM	0	R/W	32-bit Complement Code	This register needs to participate in parameter configuration self-check. This register participates in parameter configuration self-check along with the addresses 0x0 ~ 0x7, 0x25 ~ 0x3A, 0x55 ~ 0x60. If all the above register values add up to 0xFFFFFFFF, the parameter configuration self-check passes. To ensure parameter configuration self-check successful, the register should write correct value (0xFFFFFFFF - the sum of the configuration values of other registers participating in the check).

Table 2-43 Self-checking Register

Name	Type	Address	Description	Default
ANA_CTRL0	R/W	0x00	Analog Control Register 0.	0x00000000
ANA_CTRL1	R/W	0X01	Analog Control Register 1.	0x00000000
DSP_CTRL0	R/W	0x02	Metering Control Register 0.	0x00000000
DSP_CTRL1	R/W	0x03	Metering Control Register 1.	0x00000000
DSP_CTRL2	R/W	0x04	Metering Control Register 2.	0x00000000
DSP_CTRL3	R/W	0x05	Metering Control Register 3.	0x00000000
DSP_CTRL4	R/W	0x06	Metering Control Register 4.	0x00000000
DSP_CTRL5	R/W	0x07	Metering Control Register 5.	0x00000000
DSP_CFG_CALI_PA	R/W	0x25	To set gain calibration for the active power A.	0x00000000
DSP_CFG_DC_PA	R/W	0x26	To set offset calibration for the active power A.	0x00000000
DSP_CFG_CALI_QA	R/W	0x27	To set gain calibration for Reactive power A.	0x00000000
DSP_CFG_DC_QA	R/W	0x28	To set offset calibration for Reactive power A.	0x00000000
DSP_CFG_CALI_PB	R/W	0x29	To set gain calibration for Active power B.	0x00000000
DSP_CFG_DC_PB	R/W	0x2A	To set offset calibration for Active power B.	0x00000000
DSP_CFG_CALI_QB	R/W	0x2B	To set gain calibration for Reactive power B.	0x00000000
DSP_CFG_DC_QB	R/W	0x2C	To set offset calibration for Reactive power B.	0x00000000
DSP_CFG_CALI_RMSU	R/W	0x2D	To set gain calibration for Voltage RMS.	0x00000000
DSP_CFG_RMS_DCU	R/W	0x2E	To set offset calibration for Voltage RMS.	0x00000000
DSP_CFG_CALI_RMSIA	R/W	0x2F	To set gain calibration for Current RMS A.	0x00000000
DSP_CFG_RMS_DCIA	R/W	0x30	To set offset calibration for Current RMS A.	0x00000000
DSP_CFG_CALI_RMSIB	R/W	0x31	To set gain calibration for Current RMS B.	0x00000000
DSP_CFG_RMS_DCIB	R/W	0x32	To set offset calibration for Current RMS.	0x00000000
DSP_CFG_PHC	R/W	0x33	Phase Error Calibration Registers. [10:0]= phase error calibration value for channel A	0x0000000

			[26:16]= phase error calibration value for channel B. Where the range is from -766 to 767.	
DSP_CFG_DCU	R/W	0x34	To set the DC compensation for the voltage channel.	0x00000000
DSP_CFG_DCIA	R/W	0x35	To set the DC compensation for the current channel A.	0x00000000
DSP_CFG_DCIB	R/W	0x36	To set the DC compensation for the current channel B.	0x00000000
DSP_CFG_BPF	R/W	0x37	Band-pass filter coefficient. Related to setting the DSP_MODE by Bit[7:4] of metering control register 0 (0x02,DSP_CTRL0). Setting 0x806764B6 at DSP_MODE=0,1,2; setting 0x80DD7A8C at DSP_MODE=6,7; setting 0x82B465F0 at DSP_MODE=8. The frequency of other modes would be not supported to measure, so setting to 0x0.	0x00000000
DSP_CFG_CKSUM	R/W	0x38	Configuration register for checksum.	0x00000000
EGY_PROCTH	R/W	0x39	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.	0x00000000
EGY_PWRTH	R/W	0x3A	Accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384;	0x00000000

			the accumulated value of the low-speed energy accumulator equals to this value*4.	
DSP_OV_THL	R/W	0x55	To set the lower threshold for the no-load determination.	0x00000000
DSP_OV_THH	R/W	0x56	To set the upper threshold for the no-load determination.	0x00000000
DSP_SWELL_THL	R/W	0x57	To set the lower threshold for the voltage dip.	0x00000000
DSP_SWELL_THH	R/W	0x58	To set the upper threshold for the voltage swell.	0x00000000
DSP_DIP_THL	R/W	0x59	To set the lower threshold for the voltage dip.	0x00000000
DSP_DIP_THH	R/W	0x5A	To set the upper threshold for the voltage swell.	0x00000000
FD_OVTH	R/W	0x5B	To set over-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
FD_LVTH	R/W	0x5C	To set under-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
FD_IA_OCTH	R/W	0x5D	To set over-current threshold in channel A for fast detection. Bit width is 30bit.	0x00000000
FD_IA_LCTH	R/W	0x5E	To set under-current threshold in channel A for fast detection. Bit width is 30bit.	0x00000000
FD_IB_OCTH	R/W	0x5F	To set over-current threshold in channel B for fast detection. Bit width is 30bit.	0x00000000
FD_IB_LCTH	R/W	0x60	To set under-current threshold in channel B for fast detection. Bit width is 30bit.	0x00000000

3. Main Power Supply

Features of V93XX main power system as below:

- 3.3V single main power supply, the voltage input range: 2.6~3.6V
- The power supply of the internal digital circuit comes from the Digital main power circuit (DVCCLDO)
- The power supply of the oscillator circuit comes from 3.3V main power
- Supporting power down detection
- Controllable CF detection of power down alarm

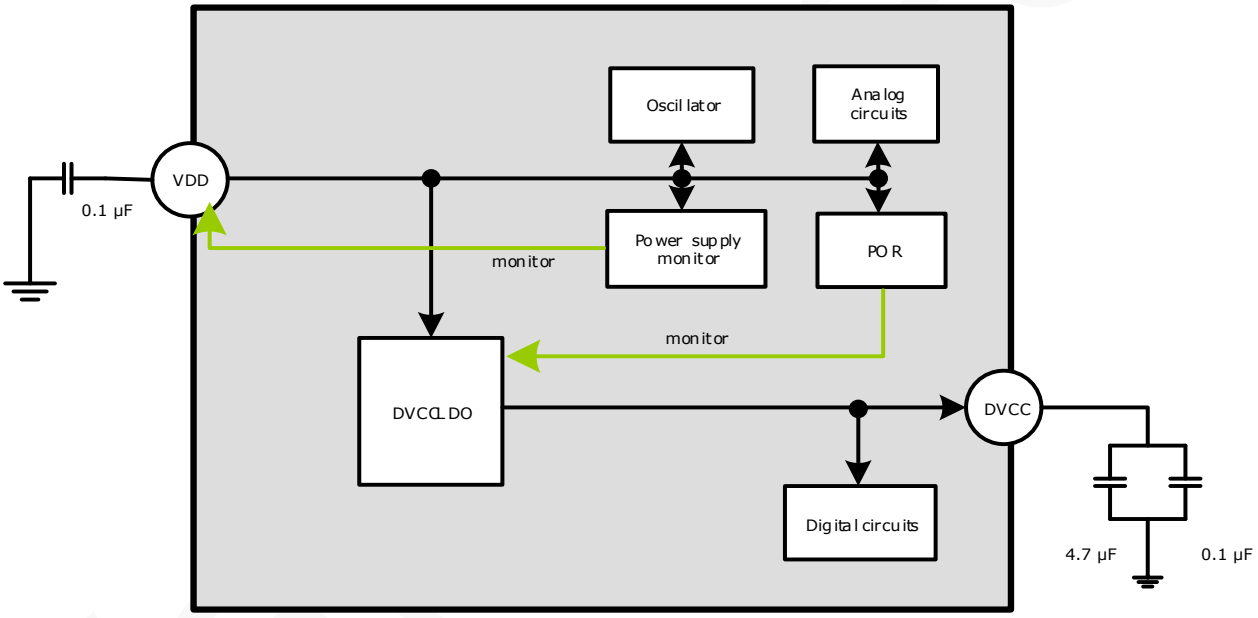


Figure 3-1 Main Power System

3.1. Power Supply Monitoring Circuit

V93XX integrates an internal power-down detection circuit to supervise the voltage on pin "VDD" all the time. When the voltage on the pin "VDD" is lower than 2.8V (±7%), the power-down interrupt would be generated. The power supply monitoring circuit is always on work.

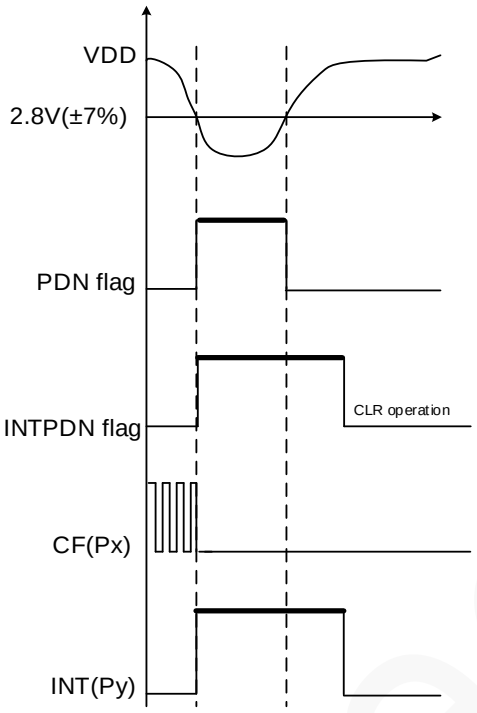


Figure 3-2 Power-down monitoring

3.2. Digital Power Supply

V93XX integrates an on-chip LDO (DVCCLDO) and supplies voltage for digital circuit. This circuit could output stable voltage with the power supply (VDD) has ripple noise. It is recommended to decouple the pin DVCC externally with a ≥4.7 μF capacitor in parallel with a 0.1 μF capacitor. LDO is always on work.

The DVCCLDO has a driving capability of 35 mA. When the load current on the digital circuits is less than 35 mA, the DVCCLDO outputs stable voltage. When the load current is higher than 35mA, the output voltage reduces as the current increases.

3.3. Power on Reset Circuit

The internal power-on reset circuit supervises the output voltage on **"DVCCLDO"** all the time. When the output voltage is lower than 1.3V, POR reset signal will be generated and force the chip into the reset state. When the output voltage is higher than 1.3V, the reset signal will be released, and the chip will get to the Default State.

POR is always on work.

4. Bandgap circuit

In the V93XX, the Bandgap circuit outputs a reference voltage and bias current, about 1.21V with a typical temperature coefficient of 10 ppm/°C, for ADCs and the 6.5 MHz RC oscillator. By default, the Bandgap circuit was enabled. This circuit consumes about 0.09 mA (typical).

Users can configure RESTL<1:0> (Bit[4:3]) and REST<2:0> (Bit[2:0]) of analog control register (0x01, ANA_CTRL1) to adjust the temperature coefficient of Bandgap circuit to cancel the temperature coefficient introduced by the external components, with the following steps:

1) Assume the current settings of relative bits are REST<2:0>='010' and RESTL<1:0>='00', which corresponds to the temperature coefficient of Bandgap is +14 ppm.
2) Measure meter errors in high and low temperature conditions. For example, this meter has 0 error at 20℃, and the measuring errors are 0.6% at 80℃ and -0.4% at -40℃ respectively. Then a -(0.6%-(-0.4%))/2=-0.5% measuring error needs to be compensated relative to high temperature working condition, equivalent to -0.5%/(80-20)=-5000/60=-83 ppm.
3) As measured error is minus two times of Reference temperature coefficient error, to compensate a -83 ppm error, an additional +41.5 ppm of Bandgap REF temperature coefficient adjustment is needed. Taking the initial +14 ppm setting into consideration, the actual adjustment should be +55.5 ppm. According to the lookup table of RESTL<1:0> and REST<2:0>, user should set register RESTL<1:0> to '11' and REST<2:0> to '000', whose combination equals to a +56 ppm temperature coefficient adjustment.

Attention: For the adjustment of Reference temperature parameters would influence the basic error; therefore, when customers designed each new product, please first confirm the temperature parameter of Reference then calibrate the error of the meter.

A temperature coefficient drift of x in the Bandgap circuit results in a drift of -2x in the measurement error.

Figure 4-1 Register for Bandgap Circuit

Register	Bit	Default Value	Description
	Bit[4:3]	0	To roughly adjust the temperature coefficient of the Bandgap

Register	Bit	Default Value	Description
ANA_CTRL1	RESTL<1:0>		circuit. 00: 0 ppm 01: -58 ppm 10: +111 ppm 11: +56 ppm In order to obtain the best metering performance and temperature performance during normal metering, it must be iterated according to the calculated result.
	Bit[2: 0] REST<2:0>	0	To finely adjust the temperature coefficient of the Bandgap circuit 000: 0 ppm 001: +7 ppm 010: +14 ppm 011: +28 ppm 100: -32 ppm 101: -21 ppm 110: -14 ppm 111: -7 ppm In order to obtain the best metering performance and temperature performance during normal metering, it must be iterated according to the calculated result.

5. Clock

The on-chip RC oscillator circuit and the external input clock provide clocks for the V93XX:

- An external 6.5536 MHz of the pins "CTI", "CLK1". After the frequency divider, SDIV, controlled by DSP_MODE (Bit<7:4>, Table 2-18 Metering Control Register 0 (0x02, DSP_CTRL0)). This clock source for all digital block uses. After the frequency divider, ADIV, controlled by ADCKSEL (Bit25<31:30>, analog control register, 0x01, ANA_CTRL1). This clock source for ADC uses. After POR, RSTN pin reset, RX reset, or global software reset, this oscillator circuit starts to run automatically.
- On-chip 6.5 MHz (The deviation is within ±20% from chip to chip for mass production. The temperature deviation from -40~85 degree for each specific chip is less than ±5%.) RC oscillator generates the clock, "CLK2". When the CTI external input clock was disabled, it would be an optional clock source for digital block uses. This circuit can be disabled.
- On-chip 32 KHz (±50%) RC oscillator generates the clock," CLK3". This clock source for IO ports filter use. This circuit keeps on working until the system is powered off.
- External CLK (32768 Hz), input from X32KIN pin. This clock source for low-speed energy accumulator uses. The clock source of energy accumulator would be controlled by EGY_CLK_SEL (bit23, metering control register 1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1))).

  As mentioned above, the relationship between the 4 clocks source as the shown below:

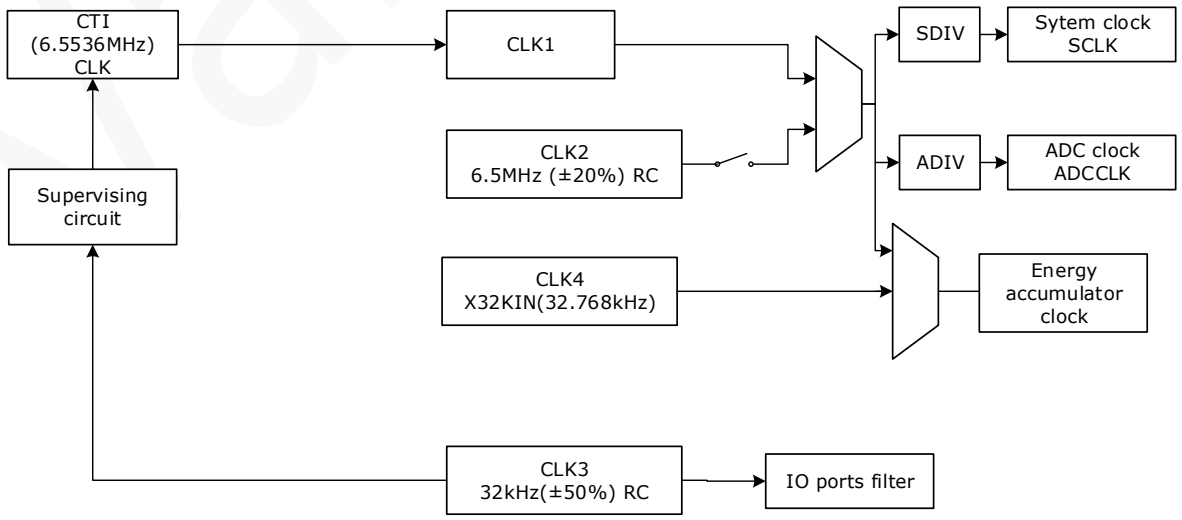


Figure 5-1 Clock generation

Table 5-1 Clock Generation Related Registers

Register	Bit	Default Value	Description
ANA_CTRL1	Bit7 XRST_PD	0	The external input CTI clock enable. 0: enable 1: disable
	Bit[22] RCCLK_PD	0	To enable the 6.5-MHz RC clock. 0: enable 1: disable The bit must be set to 0 for proper operation.
	Bit[23] XTALPD	0	To disable the CTI external input clock by set this bit to 1. By default, this circuit is enabled.
	Bit[29:24] RCTRIM<5:0>	0	To adjust the 6.5M RC frequency. 000000~011111: step-up the frequency by 1.25% 100000~111111: step-down the frequency by 1.25%
	Bit[31:30] ADCKSEL<1:0>	0	To select the clock frequency for the ADC. 00 corresponds to 819.2 KHz. 00: ×1 01: ×2 10: ×1/4 11: ×1/2
DSP_CTRL0 (Table 2-18 Metering Control Register 0 (0x02, DSP_CTRL0))	Bit[7:4] DSP_MODE<1:0>	0	DSP Operating Mode. 0: 128 sampling points per cycle by DSP at 6.5536 MHz system clock 1: 64 sampling points per cycle by DSP at 6.5536 MHz system clock 2: 32 sampling points per cycle by DSP at 6.5536 MHz system clock. 3, 4, and 5: Reserved.

Register	Bit	Default Value	Description
			6: 64 sampling points per cycle by DSP at 3.2768 MHz system clock 7: 32 sampling points per cycle by DSP at 3.2768 MHz system clock 8: 32 sampling points per cycle by DSP at 819.2 KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) 9: 16 sampling points per cycle by DSP at 409.6 KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) Others: the same as mode 0
DSP_CTRL1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1))	Bit23 EGY_CLK_SEL	0	To selection the clock for Energy accumulator. It needs the stable time around 107 us when CLK switch over. Please disable CF before it is stable. 0: 204.8 KHz 1: 32768 Hz

5.1. External input high-frequency clock

Users can input 6.5536 MHz clock in CTI pin. CLK1 clock is provided for V93XX for system, metering VMA, ADC, UART/ SPI interface and energy module. If the CTI pin does not have external clock, the system automatically uses the RCH clock (CLK2 clock) for V93XX for system, metering VMA, ADC, UART/ SPI interface and energy module.

5.2. High-Frequency RC Oscillator

The V93XX has an internal high-frequency 6.5 MHz RC oscillator (The deviation is within ±20% from chip to chip for mass production. The temperature deviation from Celsius -40~85 degree for each specific chip is less than ±5 %.)

Under the metering mode, when CTI external input clock error, the circuit will automatically turn on and

produce clock (CLK2) to work as an optional clock source for digital circuits.

After POR, RSTN pin reset, RX reset, or global software reset, this circuit and Bandgap circuit will be working automatically.

5.3. Low-Frequency RC Oscillator

V93XX the low-frequency RC oscillator can generate a 32 KHz (±50%) RC clock (CLK3) to drive the IO ports filter (RSTN/ RX/ A0/ A1 pin) for using the signal input.

This oscillator is always on work until the system is powered off.

5.4. External Input Clock

The external can inject a 32768 Hz frequency clock into the X32KIN pin of V93XX to provide CLK4 clock for low-speed accumulation of energy barrel of V93XX.

6. RESET

6.1. Reset Related Registers

Table 6-1 Reset Related Registers

<table>
<tr><th>Register</th><th>Bit</th><th>Description</th></tr>
<tr><td>0x74

SYS_STS</td><td>Bit[22:20]

RST_SOURCE</td><td>Flag bits to indicate the reset source
<table>
<tr><th>Bit22</th><th>Bit21</th><th>Bit20</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>A POR event occurred.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>A RSTN event occurred.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>An RX reset event occurred.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>A global software reset occurred.</td></tr>
</table></td></tr>
<tr><td colspan="2">0x6c, SFTRST

Software Reset Control Register</td><td>Writable only, in the form of 32-bit 2’ complement.

Write “0x4572BEAF” to the register to reset the system and all circuit is back to initial state.</td></tr>
</table>

6.2. Power-On Reset (POR)

In V93XX, the internal power-on reset circuit supervises the output voltage on **“DVCCLDO”** all the time. When the output voltage is lower than 1.3 V, the reset signal will be generated and force the chip into the reset state. When the output voltage is higher than 1.3 V, the reset signal will be released, and the chip will get to the Default State in 500 μs.

When a POR event occurs, the bit **“RST_SOURCE”** (Bit[22:20], 0x74, SYS_STS) will be reset to **“0b001”**.

In the reset state, the master MCU and the VMA metering architecture cannot access RAM. When the chip exits from the reset state, RAM will implement the self-checking in about 1.25 ms. If there is no error occurring, RAM can be accessed.

In the reset state, the UART/SPI serial interface is idle. The UART/SPI serial interface starts to run immediately once the chip exits from the reset state.

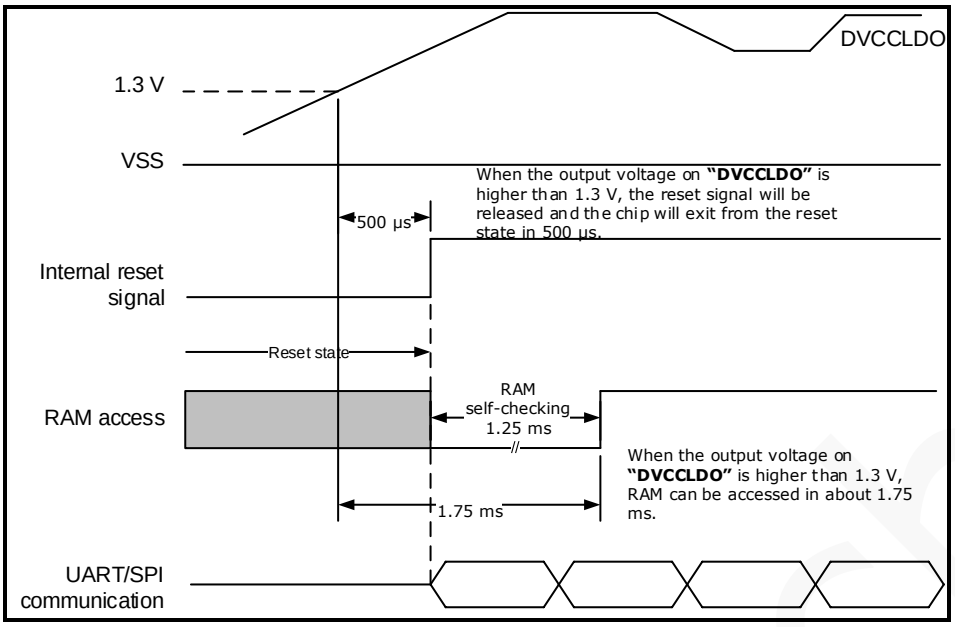


Figure 6-1 Timing for POR

6.3. External Reset

In V93XX, the external reset circuit supervises the status on pin **"RSTN"** all the time. When the input on pin **"RSTN"** must be driven low for at least 2 ms to force the chip into the reset state. Pull to the logic high, and 900µs later the chip will exit from the reset state and get back to the Default State.

When a RSTN event occurs, the bit **"RST_SOURCE"** (Bit[22:20], 0x74, SYS_STS) will be reset to **"0b010"**.

In the reset state, the master MCU and the VMA metering architecture cannot access RAM. When the chip exits from the reset state, RAM will implement the self-checking in about 1.25 ms. If there is no error occurring, RAM can be accessed.

In the reset state, the UART/ SPI serial interface is idle. The UART/SPI serial interface starts to run immediately once the chip exits from the reset state.

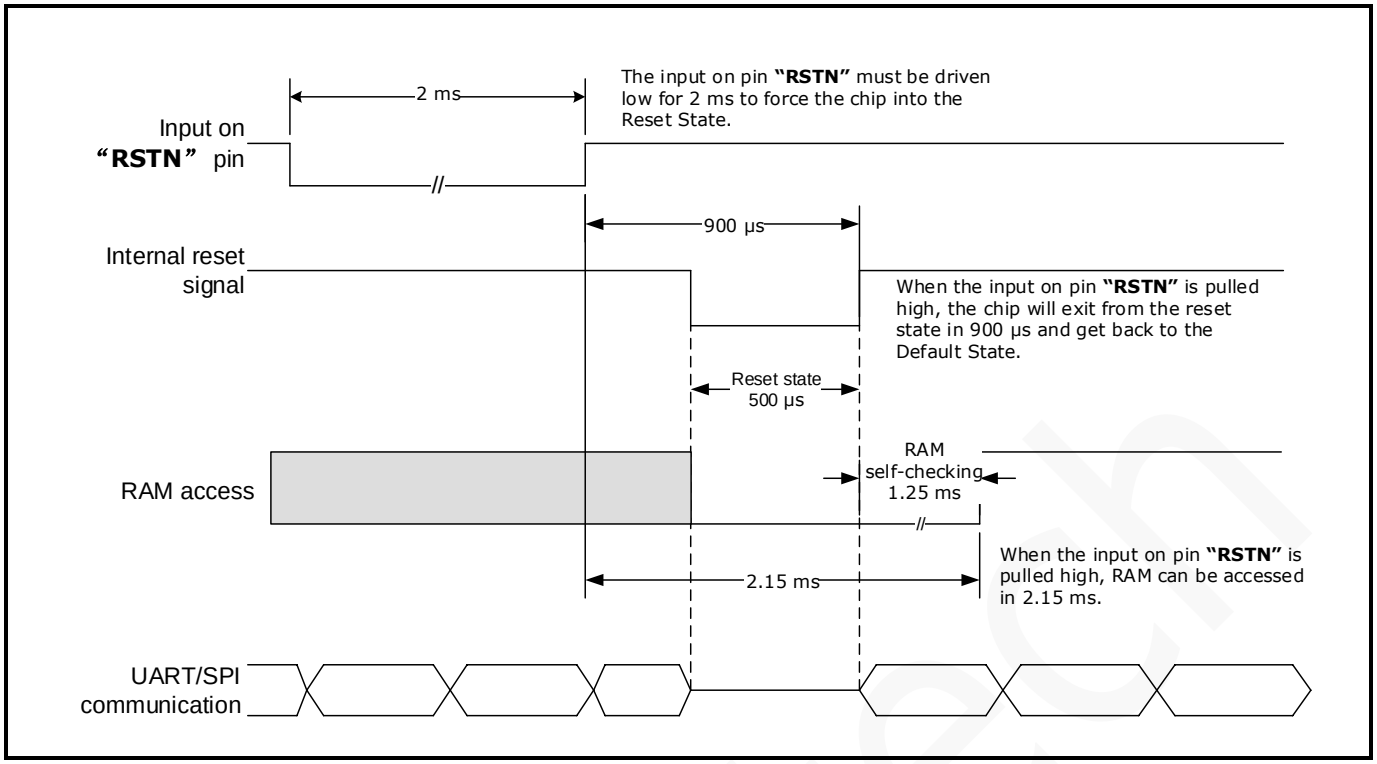


Figure 6-2 Timing for RSTN

6.4. RX Reset

"RX" reset depends on the communication type.

In the UART mode, when the **"RX/ MOSI"** pin continuously inputs a low level of 92.5 ms to force the chip into the reset state. Pull to the logic high, and 900 µs later the chip will exit from the reset state and get back to the Default State.

In the SPI mode, when the **"RX/ MOSI"** pin and **"A1/ SPCSN"** pin continuously inputs a low level of 92.5 ms and fed a clock source on pin **"A0/ SPCK"** which the frequency above the 50 Hz, then force the chip into the reset state. Pull to the logic high, and 900 µs later the chip will exit from the reset state and get back to the Default State

When the **"RX"** reset occurs, the bit **"RST_SOURCE"** (Bit[22:20], 0x74, SYS_STS) will be reset to **"0b011"**.

In the reset state, the master MCU and the VMA metering architecture cannot access RAM. When the chip exits from the reset state, RAM will implement the self-checking in about 1.25 ms. If there is no error occurring, RAM can be accessed.

In the reset state, the UART/SPI serial interface is idle. The UART/SPI serial interface starts to run

immediately once the chip exits from the reset state.

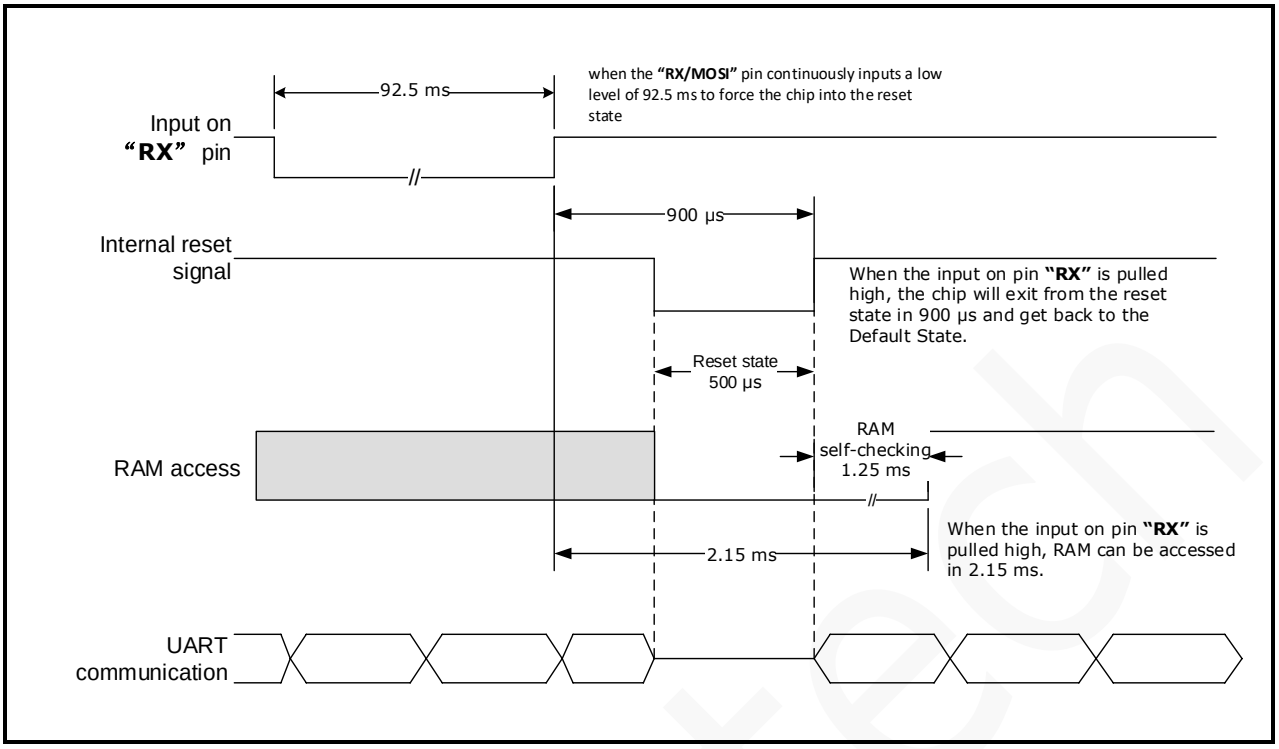


Figure 6-3 Timing for RX Reset of UART

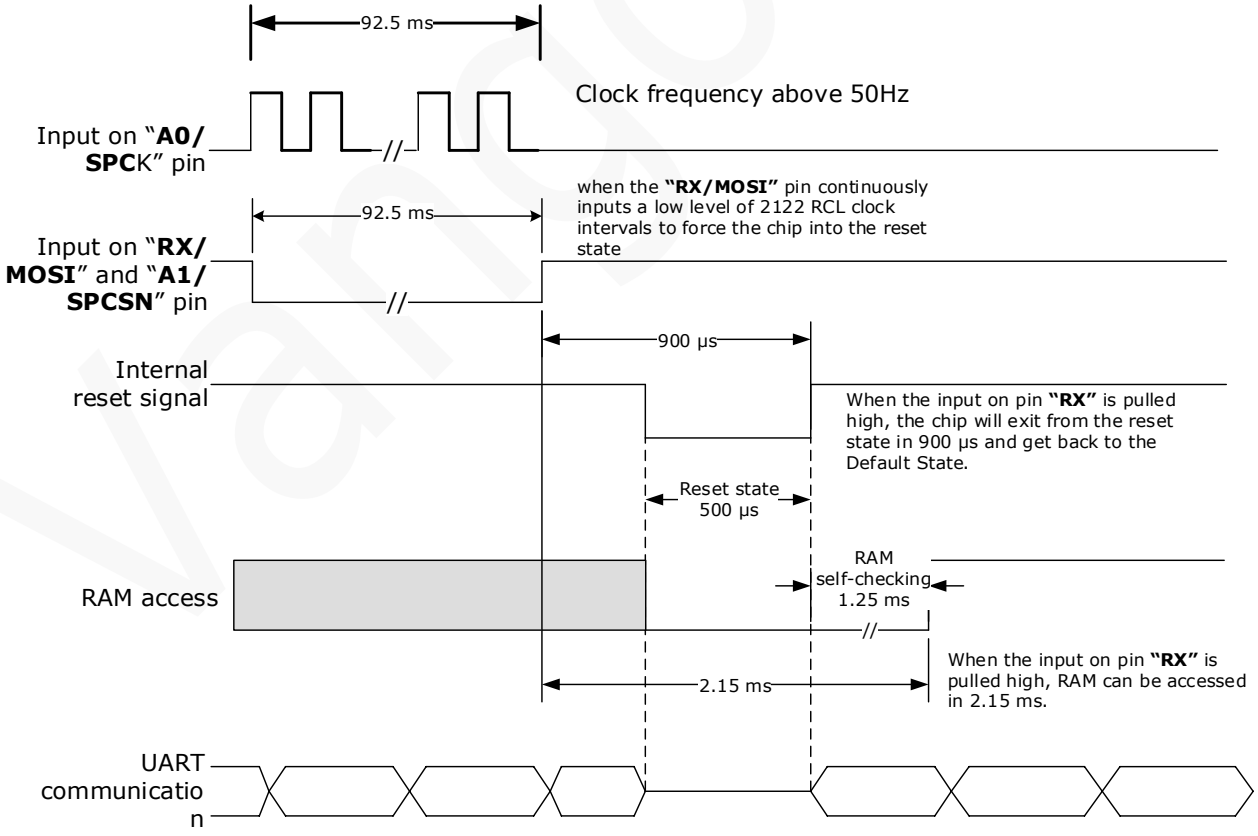


Figure 6-4 Timing for RX Reset of SPI

6.5. Global Software Reset

In V93XX, writing of **"0x4572BEAF"** in the register **"SYS_SFTRST"** (0x6C) can force the chip into the Reset State, and the chip will exit and get back to Default State in 650 μs.

When the global software reset occurs, the bit **"RST_SOURCE"** (Bit[22:20], 0x74, SYS_STS) will be reset to **"0b100"**.

In the Reset State, the master MCU and the VMA metering architecture cannot access RAM. When the chip exits from the Reset State, RAM will implement the self-checking in about 1.25ms. If there is no error occurring, RAM can be accessed.

In the Reset State, the UART serial interface is idle. The UART serial interface starts to run immediately once the chip exits from the Reset State.

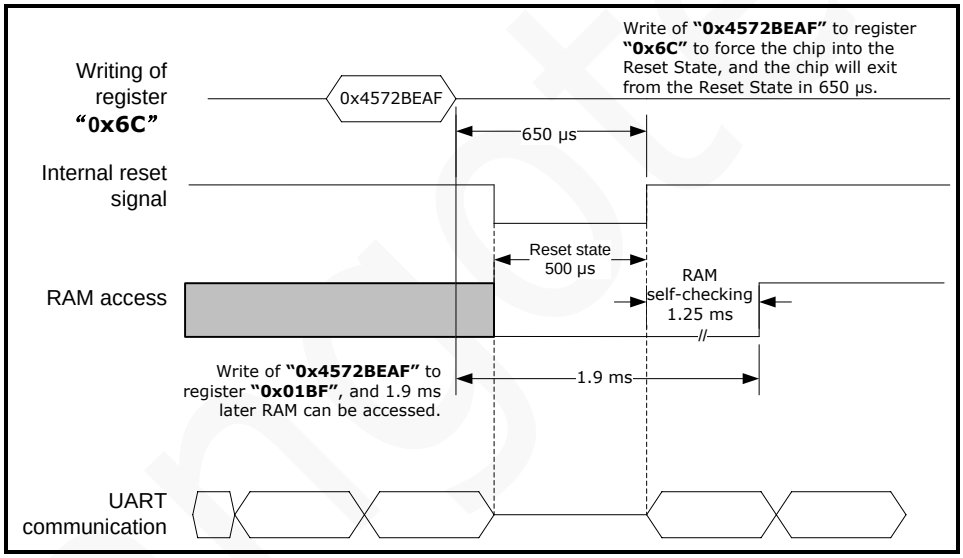


Figure 6-5 Timing of Global Software Reset

7. UART

7.1. Overview

V93XX supports two communication modes, UART and SPI, which can switch between SPI communication and UART communication without using external hardware jumper. After POR reset, RSTN reset, RX reset or soft reset, V93XX uses UART communication by default. If you want to communicate by SPI, you must initialize the SPI interface once through the SPI protocol.

Support multi-machine mode, that is, when the output data port is idle, it is a high resistance state. Up to 4 V93XX share a single data bus via physical addresses A0 and A1.

The data byte received and transmitted via the UART serial interface of the V93XX is composed of 11 bits, including 1-bit start bit (logic low), 8-bit data bits, 1-bit odd parity bit and 1-bit stop bit (logic high), as shown in the following figure. When the V93XX sends command, the least significant bit and least significant byte always are shifted out firstly.

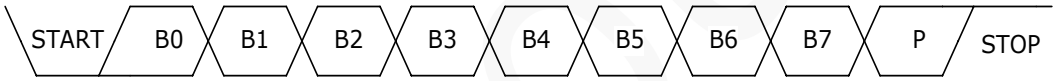


Figure 7-1 Structure of an 11-Bit data byte (from LSB to MSB)

UART protocol is a half-duplex protocol. The end of the send command for 1ms later, then V93XX would upload data.

UART supports 1200bps to 19200bps baud rate and it can self-adapting the baud rate which received from the first frame header. The baud rate will also be fine-tuned through the following communication. If the baud rate of communication has a large change, it needs rerunning the baud rate self-adapting. Before this event, it needs to set the UARTAUTOEN Bit0 of SYS_MISC to 1.

V93XX also has the command for continually writing or broadcast writing. This mode can save the parameter configurable time.

Under the following conditions, the UART transmission will be aborted and back to IDLE state.

Table 7-1 UART communication errors

No	Conditions	UARTERR set to 1
1	UART frame header error.	NO
2	UART overtime, each 2 Bytes needs to shorter than 20 ms.	YES
3	UART parity bit error.	YES

4	UART sends checksum byte from master MCU has error.	YES

7.2. Broadcast Communication

--Supports writing to consecutive registers of 1~16 addresses

--Don't care about device address{A1,A0}

--V93XX no response

Batch writes to register for multiple V93XX devices via broadcast writing by master MCU. This mode can save the parameter configurable time. The figure below is the command frame for broadcast writing operation.

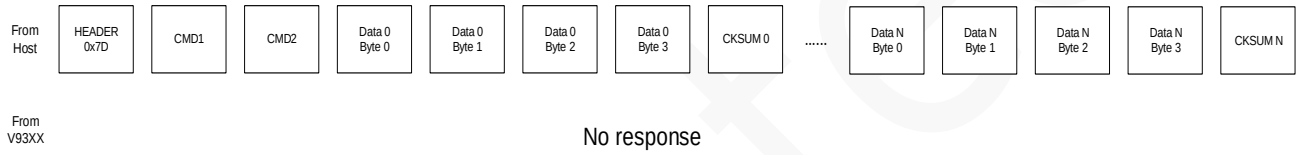


Figure 7-2 command frame for broadcast writing operation

Table 7-2 Structure of Data Byte (B7:B0) From Master MCU to V93XX on Broadcast Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on broadcast writing (N) 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits				X*	X*	0	0
3	CMD2	X*	Start address for broadcast writing operation (D_0)						
4	Data 0 Byte 0	**"Bit[7:0]"** of the target data write into register (address D_0)							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
5	Data 0 Byte 1	**"Bit[15:8]"** of the target data write into register (address D_0)							
6	Data 0 Byte 2	**"Bit[23:16]"** of the target data write into register (address D_0)							
7	Data 0 Byte 3	**"Bit[31:24]"** of the target data write into register (address D_0)							
8	CKSUM 0	Checksum 0. Add the above 4 target data bytes (Data 0 Byte 0~3), CMD1, and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM 0 = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3)							
…	…	…							
5xN+4	Data N Byte 0	**"Bit[7:0]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+5	Data N Byte 1	**"Bit[15:8]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+6	Data N Byte 2	**"Bit[23:16]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+7	Data N Byte 3	**"Bit[31:24]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+8	CKSUM N	Checksum N. Add the above 4×(N+1) target data bytes (Data 0~N Byte 0~3), CMD1, and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM N = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 + ….. + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3)							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
*X could be 0 or 1. If the length N equals to 0 on broadcast writing operation, master MCU only sends first 8 bytes of command frame to V93XX.									

7.3. Read Operation

--Supports writing to consecutive registers of 1~16 addresses

--device address {A1,A0} must be matched correctly

--V93XX would be responded

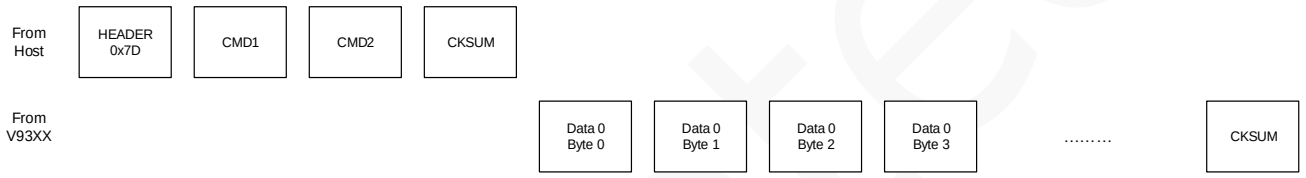


Figure 7-3 Communication protocol for read operation

Table 7-3 Structure of Data Byte (B7:B0) From Master MCU to V93XX on Read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on read operation 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits				A1	A0	0	1
3	CMD2	X*	Start address for read operation (D_0)						
4	CKSUM	Checksum. Add the above CMD1 and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below:							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		CKSUM = 0x33 + ~(CMD1 + CMD2)							
* X could be 0 or 1.									

Table 7-4 Structure of Data Byte (B7:B0) From V93XX to Master MCU on read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Data 0 Byte 0	**"Bit[7:0]"** of the target data read from register (address D_0)							
2	Data 0 Byte 1	**"Bit[15:8]"** of the target data read from register (address D_0)							
3	Data 0 Byte 2	**"Bit[23:16]"** of the target data read from register (address D_0)							
4	Data 0 Byte 3	**"Bit[31:24]"** of the target data read from register (address D_0)							
…	…	…							
4xN+1	Data N Byte 0	**"Bit[7:0]"** of the target data read from register (address $D_N=D_0+N$)							
4xN+2	Data N Byte 1	**"Bit[15:8]"** of the target data read from register (address $D_N=D_0+N$)							
4xN+3	Data N Byte 2	**"Bit[23:16]"** of the target data read from register (address $D_N=D_0+N$)							
4xN+4	Data N Byte 3	**"Bit[31:24]"** of the target data read from register (address $D_N=D_0+N$)							
4xN+5	CKSUM	Checksum. Add the above 4×(N+1) target data bytes (Data 0~N Byte 0~3, comes from V93XX), CMD1, and CMD2(comes from MCU), invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		0 Byte 2 + Data 0 Byte 3 + ….. + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3)							
*X could be 0 or 1. If the length N equals to 0 on read operation, V93XX only sends 5 bytes of response frame to master MCU.									

7.4. Write Operation

--Supports writing to consecutive registers of 1~16 addresses

--device address {A1, A0} must be matched correctly

--V93XX would be responded

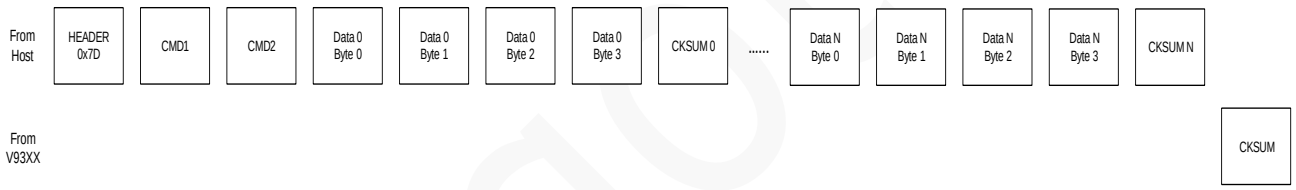


Figure 7-4 Communication protocol for write operation

Table 7-5 Structure of Data Byte (B7:B0) From Master MCU to V93XX on Write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on write operation 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits				A1	A0	1	0

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
3	CMD2	X*	Start address for write operation (D_0)						
4	Data 0 Byte 0	**"Bit[7:0]"** of the target data write into register (address D_0)							
5	Data 0 Byte 1	**"Bit[15:8]"** of the target data write into register (address D_0)							
6	Data 0 Byte 2	**"Bit[23:16]"** of the target data write into register (address D_0)							
7	Data 0 Byte 3	**"Bit[31:24]"** of the target data write into register (address D_0)							
8	CKSUM 0	Checksum 0. Add the above 4 target data bytes (Data 0 Byte 0~3), CMD1, and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM 0 = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3)							
…	…	…							
5xN+4	Data N Byte 0	**"Bit[7:0]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+5	Data N Byte 1	**"Bit[15:8]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+6	Data N Byte 2	**"Bit[23:16]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+7	Data N Byte 3	**"Bit[31:24]"** of the target data write into register (address $D_N=D_0+N$)							
5xN+8	CKSUM N	Checksum N. Add the above 4×(N+1) target data bytes (Data 0~N Byte 0~3), CMD1, and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below:							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		CKSUM N = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 + ….. + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3)							
*X could be 0 or 1. If the length N equals to 0 on broadcast writing operation, master MCU only sends first 8 bytes of command frame to V93XX.									

Table 7-6 Structure of Data Byte (B7:B0) From V93XX to Master MCU on Write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	CKSUM	Checksum (comes from V93XX). Used to verify that the write operation was successful. If CKSUM and CKSUM N (comes from master MCU) was equal, this time write operation was succeeded. If CKSUM and CKSUM N (comes from master MCU) was not equal, this time write operation was failed.							

7.5. Block Reading Operation

In order to facilitate the user to read the required data at one time and improve communication efficiency, V93XX provides address mapping function: The user maps the address of the data item that needs to be continuously operated to the address register, so that the user can perform the block read operation on the data in different places by operating the address register.

Up to 16 data register addresses can be mapped.

The block reading operation can start from any position in the mapped address register. If the address plus the number of reads exceeds the buffer size, the read is started from the beginning. For example, 10 data are read from the 13th mapping address, and after the 16th address, the data of 6 addresses is continuously read from the first one.

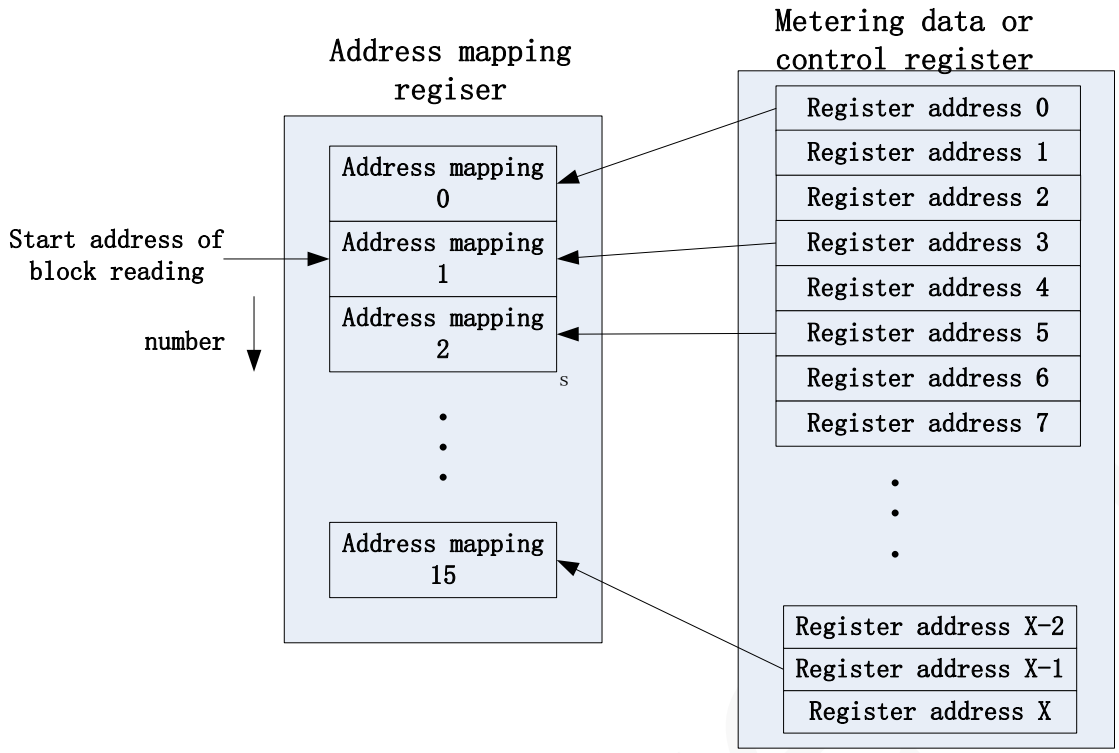


Figure 7-5 address mapping for block reading

Feature:

--Support block reading operation by address mapping from 1~16 addresses that are not consecutive.

--Device address {A1,A0} must be matched correctly.

--V93XX would be responded.

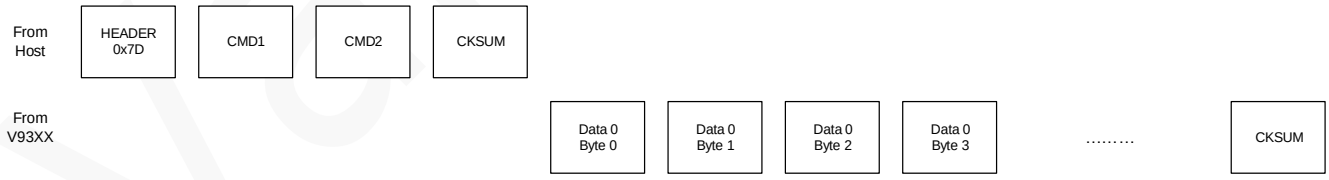


Figure 7-6 Communication protocol for block reading operation

Table 7-7 Structure of Data Byte (B7:B0) From Master MCU to V93XX on block reading Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on block				A1	A0	1	1

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		reading operation 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits							
3	CMD2	X*	X*	X*	X*	To select the start address on block reading operation 16 block reading addresses are set by 4 registers of SYS_BLKX_ADDR For example: if N=4 (length is 5) and M=4(setting start address), it would start to read address from the bit7~0 of SYS_BLK1_ADDR register in the ADDR4. The 5 register addresses for block reading operation as below: 1: stored address ADDR4 in the Bit7~0 of the SYS_BLK1_ADD 2: stored address ADDR5 in the Bit15~8 of the SYS_BLK1_ADD 3: stored address ADDR6 in the Bit23~16 of the SYS_BLK1_ADD 4: stored address ADDR7 in the Bit31~24 of the SYS_BLK1_ADD 5: stored address ADDR8 in the Bit7~0 of the SYS_BLK2_ADD			
4	CKSUM	Checksum. Add the above CMD1 and CMD2, invert the sum, and then add it to							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		"0x33" to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~ (CMD1 + CMD2)							
*X could be 0 or 1.									

Table 7-8 Structure of Data Byte (B7:B0) From V93XX to Master MCU on block reading Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Data 0 Byte 0	**"Bit[7:0]"** of the target data read from register (address $ADDR_M$)							
2	Data 0 Byte 1	**"Bit[15:8]"** of the target data read from register (address $ADDR_M$)							
3	Data 0 Byte 2	**"Bit[23:16]"** of the target data read from register (address $ADDR_M$)							
4	Data 0 Byte 3	**"Bit[31:24]"** of the target data read from register (address $ADDR_M$)							
…	…	…							
4xN+1	Data N Byte 0	**"Bit[7:0]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+2	Data N Byte 1	**"Bit[15:8]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+3	Data N Byte 2	**"Bit[23:16]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+4	Data N Byte 3	**"Bit[31:24]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+5	CKSUM	Checksum. Add the above 4×(N+1) target data bytes (Data 0~N Byte 0~3, comes from V93XX), CMD1, and CMD2(comes from MCU), invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below:							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		CKSUM = 0x33 + ~ (CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 + ….. + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3)							
*X could be 0 or 1. If the length N equals to 0 on read operation, V93XX only sends 5 bytes of response frame to master MCU.									

8. SPI

8.1. Overview

V93XX supports two communication modes, UART and SPI, which can switch between SPI communication and UART communication without using external hardware jumper. After POR reset, RSTN reset, RX reset or soft reset, V93XX uses UART communication by default. If you want to communicate by SPI, you must initialize the SPI interface once through the SPI protocol.

Support multi-machine communication mode, that is, when the output data port is idle, it is a high-resistance state. Through SPICSN chip selection signal support multiple V93XX to share a data bus.

The SPI interface of V93XX is a standard 4-wire or 3-wire SPI interface. 4-wire SPI mode must have a 50μs interval between every 2 read and write operations. 3-wire SPI mode has been low at chip select pin. When the V93XX sends command, the least significant byte and most significant bit always are shifted out firstly. The polarity and phase are 0.

When SPI reading register, the maximum speed can be 1/4 of system CLK; when reading RAM, the maximum speed can be 1/16 of system CLK. When the MCU reads the RAM or register of V93XX, if V93XX does not get the data in time, V93XX will send the wrong checksum byte to the MCU.

The RAM address range is 0x11~0x38, 0x43~0x54, 0x68, and 0x69. The remaining addresses are registers.

Before performing SPI read and write, it needs to write 0x5A7896B4 to the 0x7F addresses. If it does not do this, any SPI communication will be ignored.

SPI overtime mechanism: During communication, the time between the rising edges of every 2 SPCK needs to be shorter than 20ms, otherwise an SPI timeout is considered to occur.

Under the following conditions, an exception occurs in the SPI communication.

Table 8-1 SPI communication errors

No	Condition	SPI_ERR set to 1	The condition for the next successful communication
1	SPI overtime (rising edge of every 2 SPCK needs	Yes	No

	to shorter than 20 ms).		
2	4-wire SPI CLK error (not equals to 48 clocks).	Yes	No
3	V93XX reset happens.	No	Re-initialize SPI interface

8.2. Write Operation

After the write operation is completed, V93XX will not return a valid response to the MCU. It needs to read back the value of the register to confirm the success of the write operation.

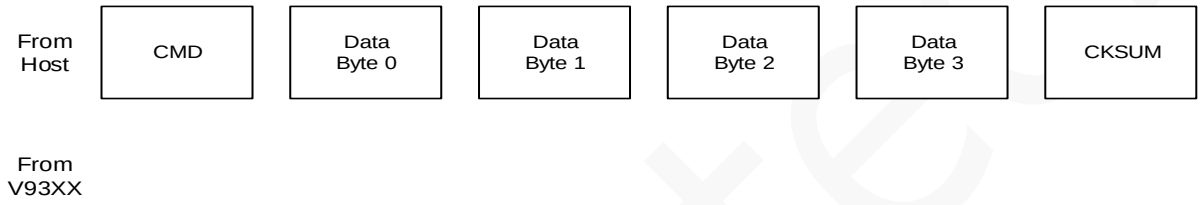


Figure 8-1 Communication protocol for SPI write operation

Table 8-2 Structure of Data Byte (B7:B0) From Master MCU to V93XX on write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	CMD	Register address for write operation							0
2	Data Byte 0	**"Bit[7:0]"** of the target data write into register							
3	Data Byte 1	**"Bit[15:8]"** of the target data write into register							
4	Data Byte 2	**"Bit[23:16]"** of the target data write into register							
5	Data Byte 3	**"Bit[31:24]"** of the target data write into register							
6	CKSUM	Checksum 0. Add the above 5 target data bytes (Data Byte 0~3) and CMD1, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below:							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		CKSUM = 0x33 + ~(CMD + Data Byte 0 + Data Byte 1 + Data Byte 2 + Data Byte 3)							

8.3. Read Operation

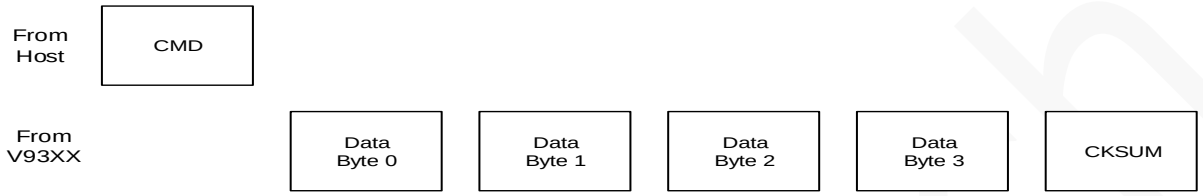


Figure 8-2 Communication protocol for SPI read operation

Table 8-3 Structure of Data Byte (B7:B0) From Master MCU to V93XX on read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	CMD	Register address for read operation							1
2	-*	MCU generates 40 clocks is used for receiving 5 bytes of response frame sent back by V93XX. MCU sends any data has no effect on the operation.							
3	-*								
4	-*								
5	-*								
6	-*								
*- this byte could be any value									

Table 8-4 Structure of Data Byte (B7:B0) From V93XX to Master MCU on read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	-*	When the MCU sends a CMD to the V93XX, the data received by the MCU doesn't have to be concerned.							
2	Data Byte 0	**"Bit[7:0]"** of the target data read from register							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
3	Data Byte 1	**"Bit[15:8]"** of the target data read from register							
4	Data Byte 2	**"Bit[23:16]"** of the target data read from register							
5	Data Byte 3	**"Bit[31:24]"** of the target data read from register							
6	CKSUM	Checksum. Add the above 4 target data bytes (Data Byte 0~3, comes from V93XX) and CMD1 (comes from MCU), invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~(CMD + Data Byte 0 + Data Byte 1 + Data Byte 2 + Data Byte 3)							
*- this byte could be any value									

8.4. Initialize interface

The default communication interface of V93XX is UART. If it wants to initialize the SPI communication interface, it needs to write 0x5A7896B4 to the 0x7F address, that is, the MCU must sends the following 6 bytes of data to V93XX via the SPI protocol.

Table 8-5 SPI interface initialization data (hexadecimal)

CMD	Data Byte 0	Data Byte 1	Data Byte 2	Data Byte 3	CKSUM
0xFE	0xB4	0x96	0x78	0x5A	0x18

Because of the SPI write operation, V93XX will not send a valid response to the MCU. After writing 0x5A7896B4 to the 0x7F address to complete the SPI interface initialization, it cannot directly confirm whether the initialization is valid. It is recommended to read any readable register and check if the checksum byte is correct to confirm that the SPI interface initialization process is completed correctly.

After POR, RSTN pin reset, RX reset, or global software reset occurs, the SPI interface is reset and the V93XX is restored to the UART communication interface. After that, the initialization process of SPI

interface needs to be performed again before SPI read-write operation.

8.5. 4-wire SPI Mode

-- SPI interface initialization must be performed after POR, RSTN pin reset, RX reset, or global software reset occurs on V93XX

-- There must be a 50 μs interval between every 2 read or write operations

-- The number of clocks per read or write must be 48

-- Chip select pin must be pulled back high after each read or write operation

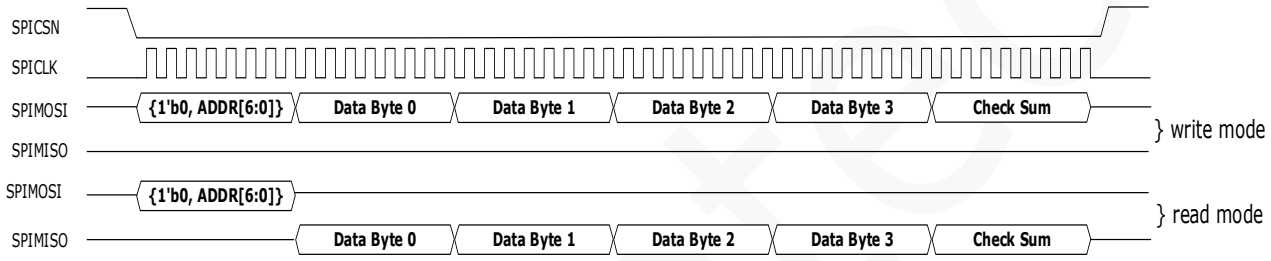


Figure 8-3 Communication protocol for 4 wire SPI mode

8.6. 3-wire SPI Mode

-- SPI interface initialization must be performed after POR, RSTN pin reset, RX reset, or global software reset occurs on V93XX

-- Chip select pin is always low

-- The number of clocks per read or write must be 48

-- The clock pin must be pulled low for at least 400μs before each read or write operation

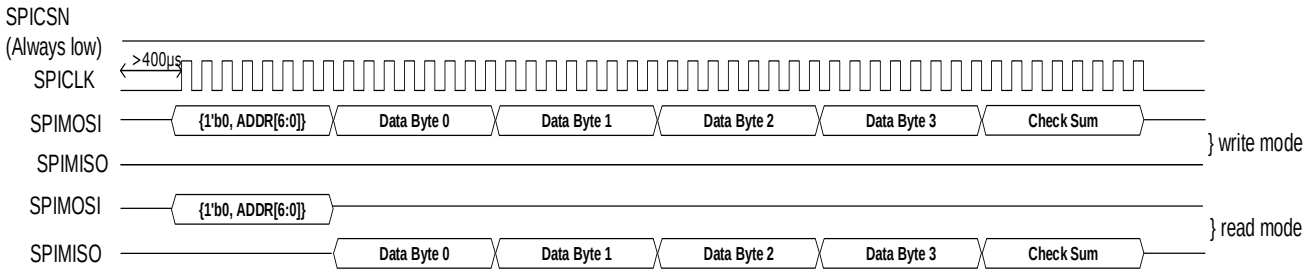


Figure 8-4 Communication protocol for 3 wire SPI mode

9. DSP

9.1. Overview

Metering DSP are mainly used in calculating total-wave active power, fundamental-wave active power, total/ fundamental-wave reactive power, total-wave apparent power, total-wave RMS and fundamental-wave RMS; also provides power grid events to detect and waveform storage functions.

The energy accumulator can flexible configuration, providing 2 high-speed energy accumulators and 6 low-speed energy accumulators.

Waveform data can output to external by DMA or internal storage.

9.2. Features

--Support 1 voltage channel and 2 current channels metering at the same time

--Selectable the full-wave bandwidth

--Provide 2 configurable fundamental-wave channels which can calculate power and RMS of fundamental-wave.

--Selectable refresh time for average power value or average RMS.

--Provide the average RMS of 10 or 12 cycles which used in voltage flicker detection.

--Support to determine the power-creep, voltage swell or dip, over or under- voltage and over or under- current.

9.3. Functional Diagram

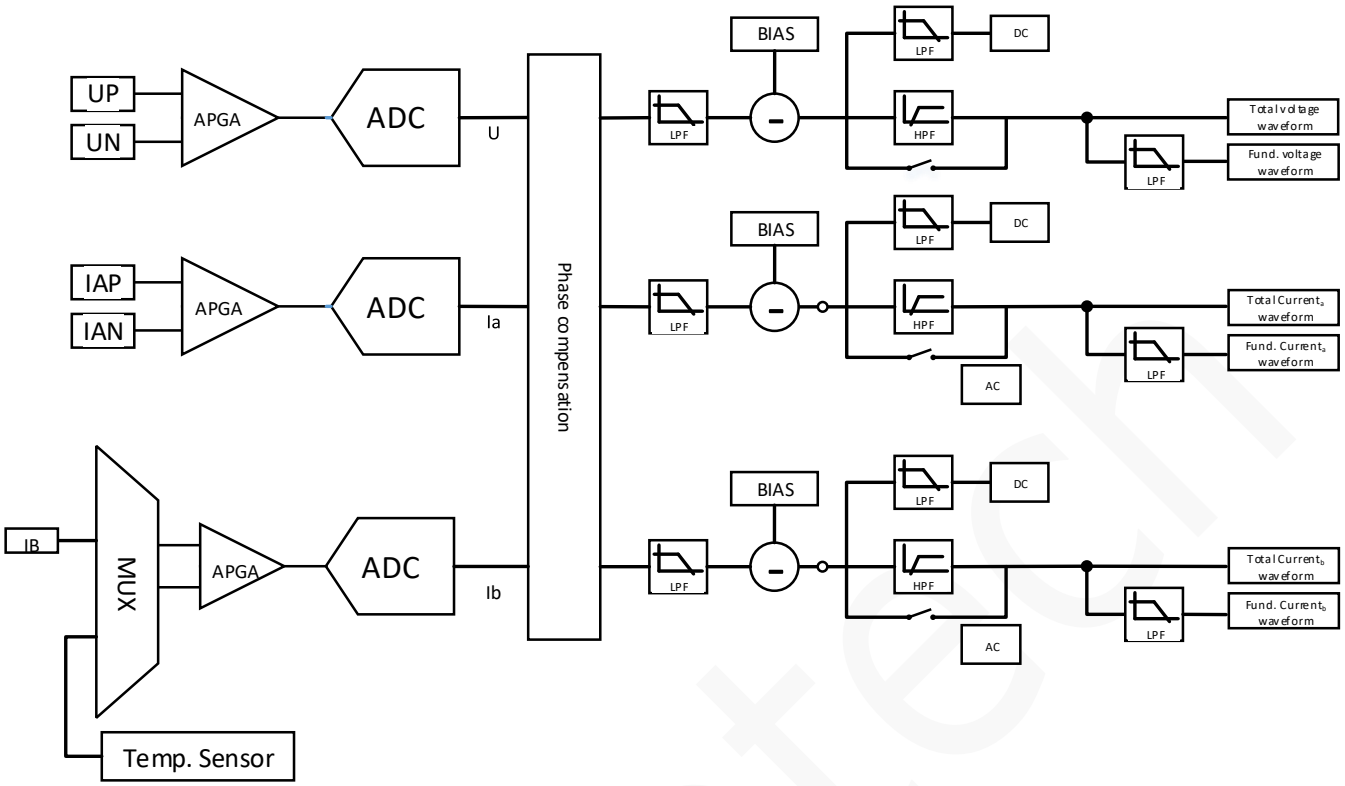


Figure 9-1 Functional Diagram 1 of Metering DSP

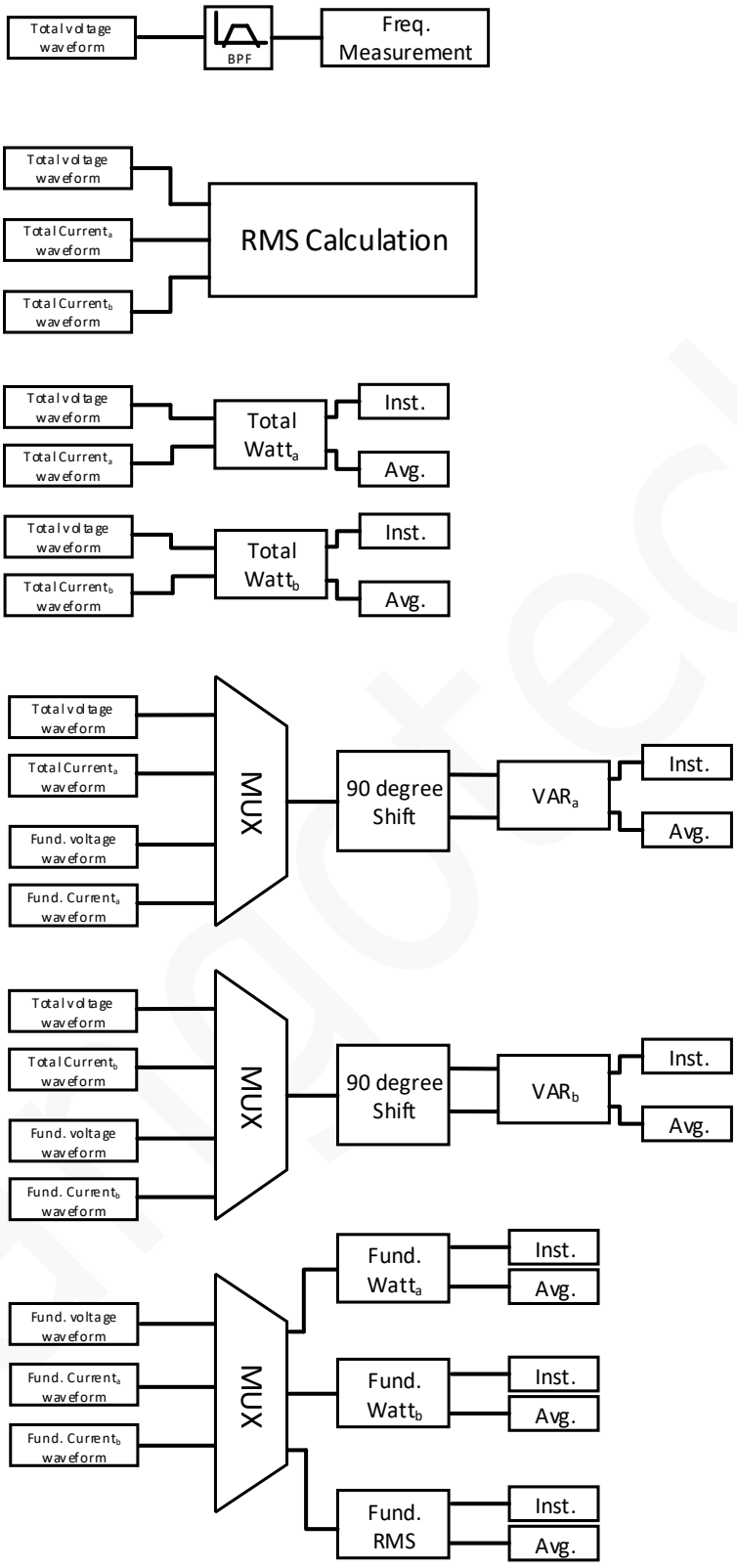


Figure 9-2 Functional Diagram 2 of Metering DSP

9.4. Application Description

9.4.1. Phase Calibration

Table 9-1 Phase Calibration Description

DSP_MODE	calibration accuracy(degree)	Calibration range(degree)
0x00, 0x01, 0x02	0.005493164	±4.21875
0x06, 0x07	0.010986328	±8.4375
0x08	0.021972656	±16.855

Phase correction of IA phc_ia = Angle to be corrected /calibration_acuracy

Phase correction of IB phc_ib = Angle to be corrected /calibration_acuracy

IA and IB error correction values are combined in complement form and written into the error correction register (0x33, DSP_CFG_PHC).

9.4.2. Frequency Calculation

V93XX supports frequency measurement, which is stored in the grid frequency register (0x21, DSP_DAT_FRQ). Users need to configure the bandpass filter coefficient according to different DSP_MODE (Table 2-18 Metering Control Register 0 (0x02, DSP_CTRL0)). For details, please refer to the bandpass filter coefficient register (Table 2-41 Bandpass Filter Register (0x37, DSP_CFG_BPF)).

The user accumulates the number of cycles and the DSP_MODE configuration frequency constant through the FRQ_SEL configuration frequency test of the metering control register 0 (0x02, DSP_CTRL0).

Grid frequency = wave_cnt*freq_const/DSP_DAT_FRQ

Table 9-2 Frequency register source FRQ_SEL description

RQ_SEL	wave_cnt
0	16

1	1
2	64

Table 9-3 Frequency Constant Description

DSP_MODE	Frequency constant
0x08	1600
0x06, 0x07	3200
0x00, 0x01, 0x02	6400

9.4.3. Phase Test

Metering chip supports voltage phase and current phase measurement. The operation principle is, master MCU sends command to register DSP_PHS_STT (0x5f) and sets to 1 via UART/SPI interface. After the metering chip is decoded as a phase measurement command, it starts to use the 6.4 KHz for sampling frequency (When DSP_MODE is 0, 1, 2, the sampling frequency of voltage signal used for phase testing is 6.4 KHz. When DSP_MODE is 6 and 7, the sampling frequency of voltage signal used for phase testing is 3.2 KHz) to counting. Until positive zero-crossing events happened, it stops counting. This counting value will write into the voltage phase register DSP_PHS_U (0x62) and current phase register DSP_PHS_I (0x65). It also records two voltage sampling values before and after the positive zero-crossing DSP_PHS_UN (0x63), DSP_PHS_UP (0x64) and two current sampling values before and after the zero-crossing DSP_PHS_IN (0x66), DSP_PHS_IP (0x67). User can obtain better accurate phase value by interpolation method.

9.4.4. Power-creep Detection

Active power, reactive power, and apparent power support the power-creep function. See Table 2-32 Power-creep Threshold Register. When the instantaneous active power/reactive power/apparent power of the channel A and the channel B are higher than the upper threshold, the startup state is entered. When the instantaneous active power/reactive power/apparent power of the channel A and the channel

B are lower than the upper threshold, the power-creep state is entered.

The user can check whether the instantaneous active power/reactive power/apparent power is in the power-creep state by Bit17~Bit12 of the SYS_STS system status register description (0x74, SYS_STS).

10. Active Waveform upload and buffer

V93XX waveform data can be transferred through DMA, or stored locally through waveform buffer. Trigger mode supports command trigger and event trigger.

10.1. Active Waveform upload

10.1.1. Overview

The V93XX supports the DMA mode for data transmission and sends up to 3 original waveform data to the external MCU through the SPI interface host mode. The user can set the active waveform upload through the metering control register 5 (0x07, DSP_CTRL5), and configure the active waveform data upload IO port P0~P6 through IO configuration register 0 (0x7D, SYS_IOCFG0) and IO configuration register 1 (0x7E, SYS_IOCFG1).

The number of sampling points per cycle of the DMA transmission data is related to DSP_MODE (Bit[7:4]) of DSP_CTRL0 (Table 2-18 Metering Control Register 0 (0x02, DSP_CTRL0)); the number of channels is related to Bit10~8 of DSP_CTRL5 (0x07, DSP_CTRL5). Its relationship is shown in the following table:

Table 10-1 Active waveform data upload configuration

The number of waveform transmission	Sampling points (related to DSP_MODE)	Baud Rate
1	256	819.2 KHz
3	128	819.2 KHz
2	128	819.2 KHz
1	128	409.6 KHz
3	64	409.6 KHz
2	64	409.6 KHz
1	64	204.8 KHz
1、2、3	32	204.8 KHz

10.1.2. Timing and Format

The V93XX transmits the original waveform of the signal to the peripheral device via the DMA SPI interface. The SPI polarity and phase are configurable. When the polarity is 0 and the phase is 0, the transmission timing is as follows:

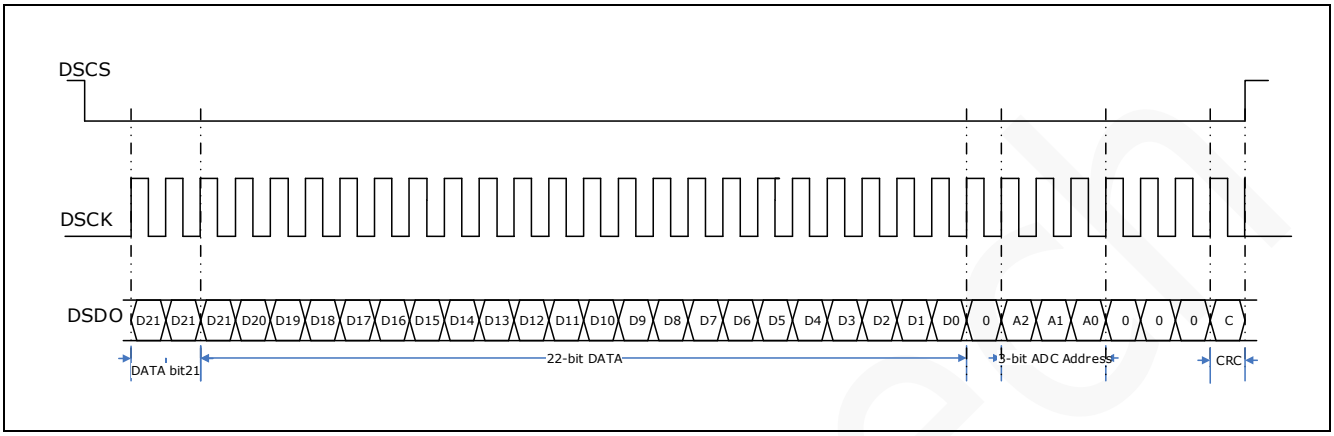


Figure 10-1 Communication timing of DMA SPI

Transmission mode: The transmission of 32-bit data is completed at one time. The format of the data frame for each transmission is as follows:

Table 10-2 Active waveform data upload format

Bit	Contents
31:30	Same as Bit29.
29:8	The original waveform of 22-bit for each channel ADC signal source.
7	0
6	Indicates whether the present waveform data is from a voltage channel. 0: no 1: yes
5	Indicates whether the present waveform data is from a channel IA. 0: no 1: yes

4	Indicates whether the present waveform data is from a channel IB 0: no 1: yes
3:1	000
0	Odd parity bit. The check range is the forward 31bit.

10.2. Waveform Buffer

After the waveform buffer function is enabled, the waveform data is stored in the RAM, supporting single-channel waveform data storage and dual-channel waveform data simultaneous storage mode. If the waveform buffer of three channels is enabled at the same time, the channel IB is invalid. The user can configure the waveform buffer and start and end condition selection by metering control register 5 (0x07, DSP_CTRL5). After the waveform buffer configuration is completed, the user can check whether the waveform buffer is completed by the WAVE_STORE of the system interrupt status register (0x72, SYS_INTSTS). After completion, the user can obtain waveform buffer data by repeatedly reading the waveform data register (0x69, DAT_WAVE), and it can read up to 309 data every time.

Table 10-3 waveform buffer data format

channel	High 16Bit	Low 16Bit
IA	$IADATA_{2n+1}$	$IADATA_{2n}$
IB	$IBDATA_{2n+1}$	$IBDATA_{2n}$
U	$UDATA_{2n+1}$	$UDATA_{2n}$
IA+IB	$IBDATA_n$	$IADATA_n$
IA+U	$IADATA_n$	$UDATA_n$
IB+U	$IBDATA_n$	$UDATA_n$
IA+IB+U (the channel IB is invalid at this time)	$IADATA_n$	$UDATA_n$

Where the range of n is 0~308

11. Electrical Signal monitoring

11.1. Zero-crossing Detection

The V93XX supports zero-crossing detection for voltage channel and current channel (the zero-crossing channel can be selected as the channel IA or channel IB by Bit20 of Metering Control Register 1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)). The zero-crossing direction can be selected by Bit19~Bit18 of the metering control register 1 (0x03, DSP_CTRL1). When the voltage/current channel signal has a zero-crossing event, the voltage zero-crossing flag USIGN/current zero-crossing flag ISIGN of the system interrupt status register (0x72, SYS_INTSTS) is set to 1. The user needs to write 1 to clear.

When the voltage/current zero-crossing interrupt output is enabled, USIGN/ISIGN of the system interrupt enable register (0x73, SYS_INTEN) is set to 1. To configure the voltage/current zero-crossing interrupt output by configuring IO Configuration Register 0 (0x7D, SYS_IOCFG0) or IO Configuration Register 1 (0x7E, SYS_IOCFG1). The output level of pin Px is automatically inverted according to the voltage zero-crossing flag USIGN/current zero-crossing flag ISIGN.

To configure the voltage/current zero-crossing interrupt output square wave by configuring IO Configuration Register 0 (0x7D, SYS_IOCFG0) or IO Configuration Register 1 (0x7E, SYS_IOCFG1).The output level of pin Px is automatically inverted according to the voltage/current zero-crossing status in real time. Each time a zero-crossing event occurs, the IO port is inverted once.

The following figure is configured to enable the zero-crossing interrupt output. When the zero-crossing detection mode is selected as the negative zero-crossing point, the USIGN/ISIGN flag bit, the zero-crossing interrupt output, and the zero-crossing output square wave waveform.

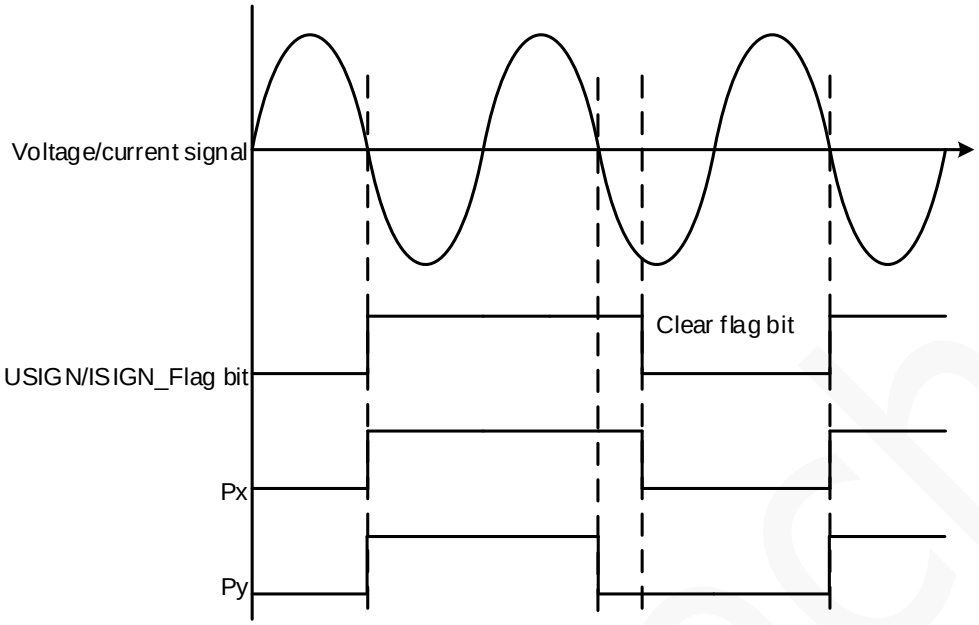


Figure 11-1 output waveform for voltage/current zero-crossing

11.2. Voltage Swell/Dip

The V93XX can be programmed to indicate voltage swell/dip. See Table 2-33 Voltage Swell or Dip Threshold Register.

When the voltage RMS value is above the upper limit of the voltage swell threshold, the voltage swell status bit (USWELL of the SYS_STS system status register (0x74, SYS_STS)) is set to 1. At the same time, the voltage swell flag (USWELL of the system interrupt status register (0x72, SYS_INTSTS)) is set to 1, and the flag bit is written to 1 to clear.

When the voltage RMS value is lower than the lower limit of the voltage swell threshold, the voltage swell status bit (USWELL of the SYS_STS system status register description (0x74, SYS_STS)) is restored to 0.

When the voltage RMS value is lower than the lower limit of the voltage dip threshold, the voltage dip status bit (UDIP of the SYS_STS system status register (0x74, SYS_STS)) is set to 1. At the same time, the voltage dip flag (UDIP of the system interrupt status register (0x72, SYS_INTSTS)) is set to 1, and the flag bit is written to 1 to clear.

When the voltage RMS value is higher than the high limit of the voltage dip threshold, the voltage dip status bit (UDIP of the SYS_STS system status register description (0x74, SYS_STS)) is restored to 0.

At the same time, the voltage swell/sag time record can be obtained by reading the register DAT_SWELL_CNT/DAT_DIP_CNT, and the half wave is in units. 24Bit is valid. Write any value to this register to clear the count value.

The voltage swell interrupt flag and voltage dip interrupt flag can be configured by configuring the IO port output. See Table 2-14 IO Configuration Register 0 (0x7D, SYS_IOCFGX0) and Table 2-16 IO Configuration Register 1 (0x7E, SYS_IOCFGX1).

11.3. Over-voltage and under-voltage/Over-current and under-current

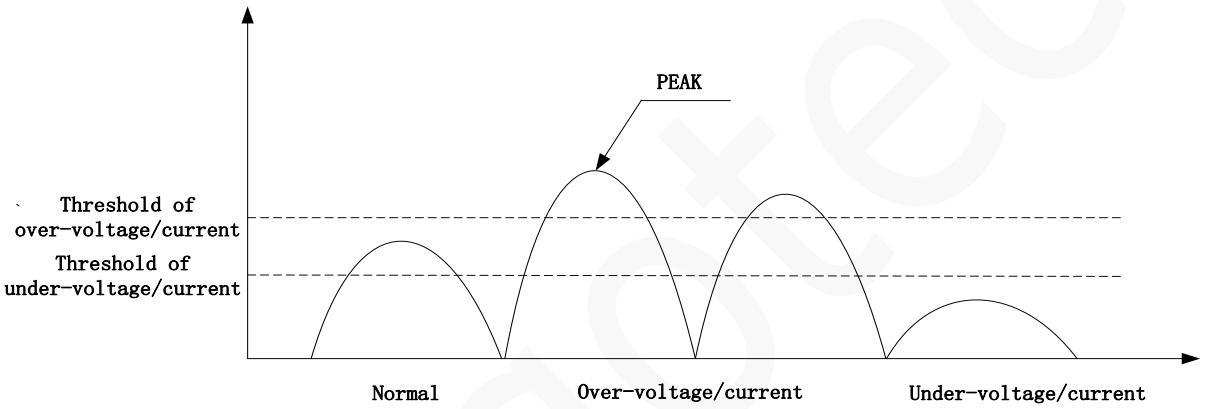


Figure 11-2 Over-voltage and under-voltage/Over-current and under-current detect

The V93XX can be programmed to indicate over-voltage/under-voltage of channel U, over-voltage/under-voltage of channel IA, and over-voltage/under-voltage of channel IB. See Table 2-34 Fast detection Threshold Register. The user can enable the detection for over-voltage/under-voltage of channel U, over-current/under-current of channel IA, and over-current/under-current of channel IB by FDUEN, FDIAEN, and FFIBEN of metering control register 4 (Table 2-22 Metering Control Register 4 (0x06, DSP_CTRL4)). The detection source supports high-pass filters and by-pass. The over-voltage or under-voltage/over-current or under-current detection time length is selectable.

1) Support waveform monitoring of three ADCs.

2) Each ADC waveform monitor has two thresholds: upper threshold (over-voltage, over-current); lower threshold (under-voltage, under-current)

3) Exceeding the upper limit threshold sample points: For example, if the set value is 4, it means that if more than 4 of the half cycle sampling points exceed the upper limit threshold, the half cycle waveform

is considered to exceed the upper limit.

4) Exceeding the upper threshold half-cycle number: For example, if the set value is 2, it means that if two consecutive half-cycles are exceeding the upper limit, an over-voltage or over-current event is considered to occur.

5) Below the lower limit threshold sample points: For example, if the set value is 4, it means that if low than or equal to 4 of the half cycle sampling points exceed the low limit threshold, the half cycle waveform is considered to below the lower limit.

6) below the lower threshold half-cycle number: For example, if the set value is 2, it means that if two consecutive half-cycles are below the lower limit, an over-voltage or over-current event is considered to occur.

7) When the event occurs, the flag bit is generated. The user can check the system status bit (SYS_STS system status register (0x74, SYS_STS)) and the flag bit (system interrupt status register (0x72, SYS_INTSTS)).

8) The corresponding event flag can be configured by interrupt enable and IO port output.

9) Response time: When the half-wave number is set to 1 and enabled or disabled the high-pass filter, the response time is 10 ms, that is, when the input signal exceeds the threshold, the event interrupt can be output after a half cycle.

12. Energy Accumulator

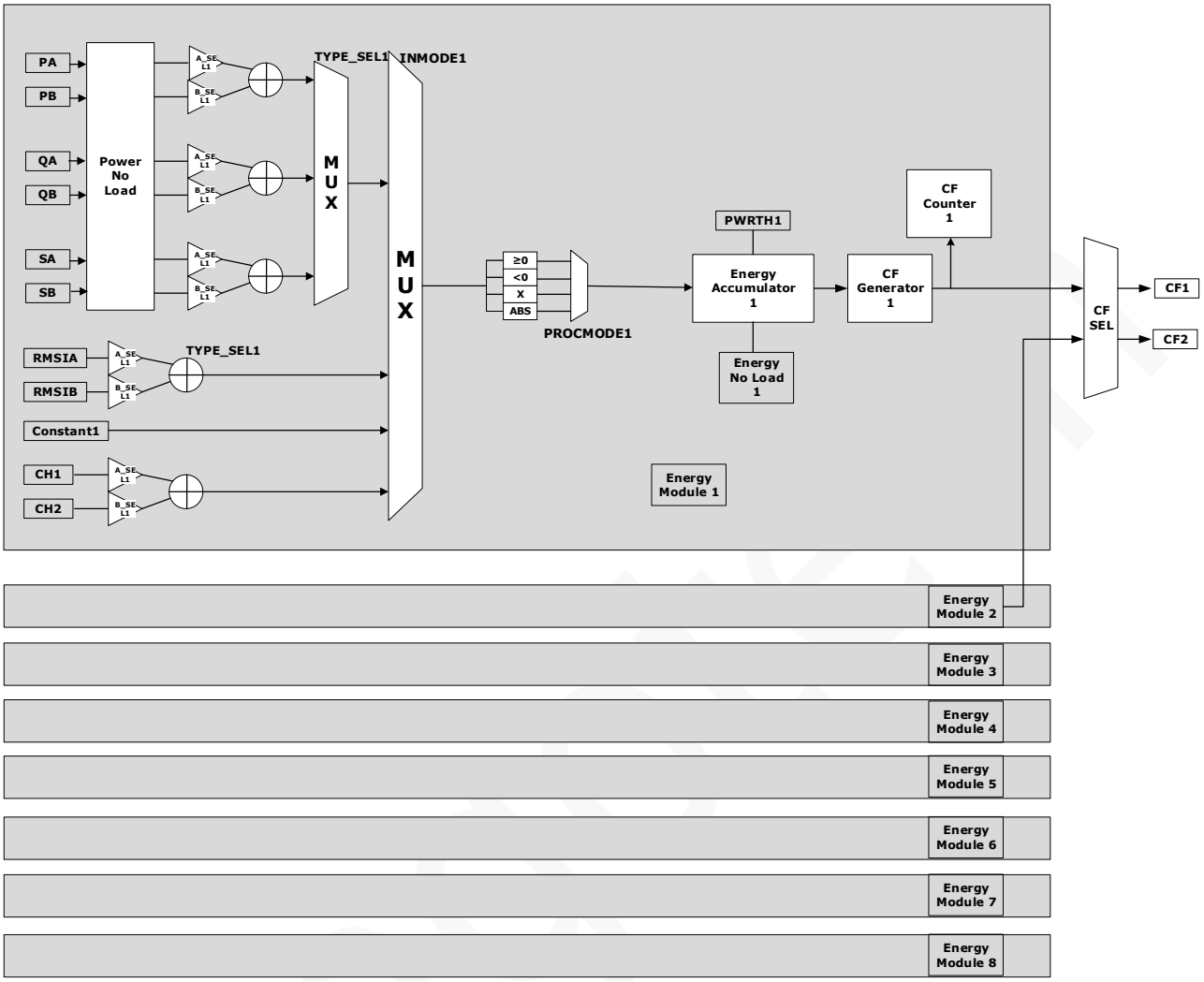


Figure 12-1 Functional block diagram of energy bucket

The V93XX has eight energy accumulators, including two high-speed energy accumulators and six low-speed energy accumulators. Each energy accumulators have four accumulation modes: power accumulation, current RMS accumulation, constant accumulation, and configurable fundamental channel accumulation.

The power accumulation is enabled by the channel an accumulation (A_SEL) and the channel B accumulation (B_SEL), which can realize only accumulating channel A power, only accumulating channel B power, and accumulating A and B power. Power can be selected for active power, reactive power and apparent power by TYPE_SEL.

The current accumulation is enabled by the channel An accumulation (A_SEL) and the channel B accumulation (B_SEL), which can realize only accumulating channel IA RMS, only accumulating channel

IB RMS, and accumulating IA and IB RMS. Accumulating two-channel IA and IB RMS value can be selected by TYPE_SEL to accumulate the summation or accumulation difference of two channels (RMSIA+RMSIB or RMSIA-RMSIB).

The constant accumulation is not affected by enabling the A/B channel accumulation.

The power accumulation is enabled by the channel an accumulation (A_SEL) and the channel B accumulation (B_SEL), which can realize only accumulating channel A power, only accumulating channel B power, and accumulating A and B power. Power can be selected for active power, reactive power and apparent power by TYPE_SEL.

Configurable fundamental channel accumulation, enabled by A channel accumulation (A_SEL) and B channel accumulation switch, which can realize only accumulating fundamental channel 1 data, accumulating only fundamental channel 2 data, accumulating fundamental channel 1 plus accumulating fundamental channel 2.

There are four types of data operation that are accumulated for each input energy accumulator. Taking the active power of two channels as an example, the operation method is as follows.

0: The energy accumulator only accumulates positive numbers. Only accumulate data with PA+PB>0. If PA+PB<0, do not accumulate.

1: The energy accumulator only accumulates negative numbers (in this case, the actual accumulated value is a positive value of the original value conversion). Only data with PA+PB<0 (abs (PA+PB)) is added. If PA+PB>0, do not accumulate.

2: The energy accumulator accumulates the original value. Accumulate PA+PB.

3: The energy accumulator accumulates the absolute value. Accumulate abs (PA+PB)

12.1. High-speed Energy Accumulator

To enable high-speed energy accumulator 1, it needs to configure CALCEN1 (Bit[6]) in DSP_CTRL1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)). To enable high-speed energy accumulator 2, it needs to configure CALCEN2 (Bit[7]) in DSP_CTRL1. The default accumulative acceleration of the high-speed energy accumulator is 204.8 KHz, and 32768 Hz can also be selected by the energy accumulator clock (bit23 in DSP_CTRL1).

High-speed energy accumulator supports CF output.

12.2. Low-speed Energy Accumulator

The six low-speed energy accumulators are enabled by DGY_LC_EN (Bit[15]) in DSP_CTRL1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)). The default accumulated acceleration is 50 Hz.

The accumulation speed of low-speed energy accumulator is controlled by CURDAT_RATE (Bit[31]) in DSP_CTRL0 (Table 2-18 Metering Control Register 0 (0x02, DSP_CTRL0)) and LCF_ACC (Bit[22]) in DSP_CTRL1.

When CURDAT_RATE=0:

LCF_ACC=0, the accumulation period of the energy buckets 3, 4, 5, 6, 7, 8 is 20 ms;

LCF_ACC=1, the accumulation period of the energy buckets 3, 4, and 5 is 10 ms, and the energy buckets 6, 7, and 8 are not accumulated.

- When CURDAT_RATE=0:

  LCF_ACC=0, the accumulation period of the energy accumulators 3, 4, 5, 6, 7, 8 is 20 ms;

  LCF_ACC=1, the accumulation period of the energy accumulators 3, 4, and 5 is 10 ms, and the energy accumulators 6, 7, and 8 are not accumulated.

- When CURDAT_RATE=1:

  LCF_ACC=0, the accumulation period of the energy accumulators 3, 4, 5, 6, 7, 8 is 40 ms;

  LCF_ACC=1, the accumulation period of the energy accumulators 3, 4, and 5 is 20 ms, and the energy accumulators 6, 7, and 8 are not accumulated.

12.3. CF Output

V93XX supports 2 channels of CF. The CF output is configured by the Meter Control Register 1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)) to select the IO port output.

CF supports source selection. It can be selected from the energy accumulator 1 or the energy accumulator 2.

CF supports polarity selection, pulse width selection, and accelerated weak-signal calibration.

Refer to the description of CF in Metering Control Register 1 (0x03, DSP_CTRL1) for details.

12.4. Energy Accumulator Power-creep Detection

Energy accumulator anti-creep threshold. When anti-creep energy accumulator exceeds the EGY_CRPTH and high-speed energy accumulator not exceeds the EGY_PWRTH, the accumulating value of high-speed accumulator will be cleared.

There is a power-creep energy accumulating register for energy accumulator 1 and 2, which they have the same accumulation speed.

User should configure threshold for the power-creep threshold register (EGY_CRPTH) and energy accumulating threshold register (EGY_PWRTH). If the accumulating value of power-creep energy accumulator register reaches the value of EGY_CRPTH first, the energy accumulating register will be cleared, and system enter the power-creep status. When the accumulating value of energy accumulating register reaches the value of EGY_PWRTH, the power-creep energy register will be cleared, system start to work and operating normally.

The actual bit width of register EGY_CRPTH is 32bit. The register contents will be padded with 0s automatically in the 4 least significant bits when the power-creep calculated. It would be calculated after extended to 36 digits.

User can judge whether in power-creep status through SYS_STS (BIT19, BIT18) .

12.5. Active Accumulation uploading Interface

Active data uploading interface can configure pins, P0/ P1/ P2/ P3/ P4/ P5/ P6, to be the active data interface through SYS_IOCFGX.

1. Asynchronous transfer mode by 1 data wire.

2. Interface configuration: 11-bit transmission (start bit + 8 data bit + parity bit + stop bit)

Communication baud rate: SPI communication data rate is 4800, it also can operate at 9600. UART communication data rate is same as present baud rate, also double the present baud rate.

To enable the function of double baud rate if BIT17 setting to 1 at the metering control register 1 (Table 2-19 Metering Control Register 2 (0x03, DSP_CTRL1)).

3. Communication time interval: 20 ms/ 40 ms (the same to instantaneous power refresh time)

4. Frame header: 0x7D

5. Checksum: the energy accumulator 1 accumulating data plus the energy accumulator 2 accumulating data. Total accumulate 8 bytes and reverse them, then plus 0x33 to obtain the checksum.

6. Frame length: 10 bytes

7. To enable this block by BIT 16 of metering control register 1 (DSP_CTRL1).

Protocol format as below:

frame header	the energy accumulator 1 accumulating data	the energy accumulator 2 accumulating data	checksum
0x7D	4 bytes	4 bytes	1 byte

13. Signal IO Ports

13.1. Overview

The V93XX provides up to seven signal outputs, and seven output signals are used to map the internal output sources.

13.2. Functional Description

The seven signal output ports can be configured as CF output, energy upload interface, waveform active upload DMA channel interface, zero-crossing square wave and four types of interrupt output. The signal output port can be set to output a single signal, or it can be set to output certain types of interrupt signals. See Table 2-14 IO Configuration Register 0 (0x7D, SYS_IOCFGX0) and Table 2-16 IO Configuration Register 1 (0x7E, SYS_IOCFGX1) for details.

1st type interruption: current zero-crossing interruption, voltage zero-crossing interruption, high-speed energy accumulator 1/2 overflow interruption.

2nd type interruption: waveform refreshes interruption, instantaneous RMS refresh interruption, average RMS refreshes interruption, instantaneous power value refresh interruption, average power value refreshes interruption, waveform storage finish interruption, waveform storage overflow interruption and waveform data upload finished interruption.

3rd type interruption: IB channel under-current interruption, IB channel over-current interruption, IA channel under-current interruption, IA channel over-current interruption, voltage channel under-voltage interruption, voltage channel over-voltage interruption, voltage dip interruption and voltage swell interruption.

4th type interruption: SPI communicating error interruption, UART communicating error interruption, parameters self-checking error interruption, phase measurement finished interruption, power-down interruption, reference error interruption, CTI external input clock error interruption and RAM self-checking error interruption.

Figure 13-1 Functional Block Diagram of signal IO ports

Description:

1) When the output port is used as the CF output, it is supported to set the width of the output pulse and select the output polarity. When the output period is less than twice the CF output pulse width, CF is output at a duty cycle of 50%. For example, if the output width is 80 ms and the output period is less than 160 ms, it will be output according to the duty cycle of 50%.

2) Using the UART protocol when the TX output for energy upload.

3) When used as the interrupt event output port, the output port defaults to low level output. If the event occurs, it outputs a high level until the user clears the event flag bit, and the output state returns to the default level.

4) When used as a zero-crossing square wave output, the output port defaults to a low-level output. If configured as a positive zero-crossing, the IO port flips when the signal transitions from a negative signal to a positive signal.

5) When used as a DMA output port, the SPI protocol is required, and the user is required to select the SPLK, SPDO, and SOCS ports.

14. Outline Dimensions

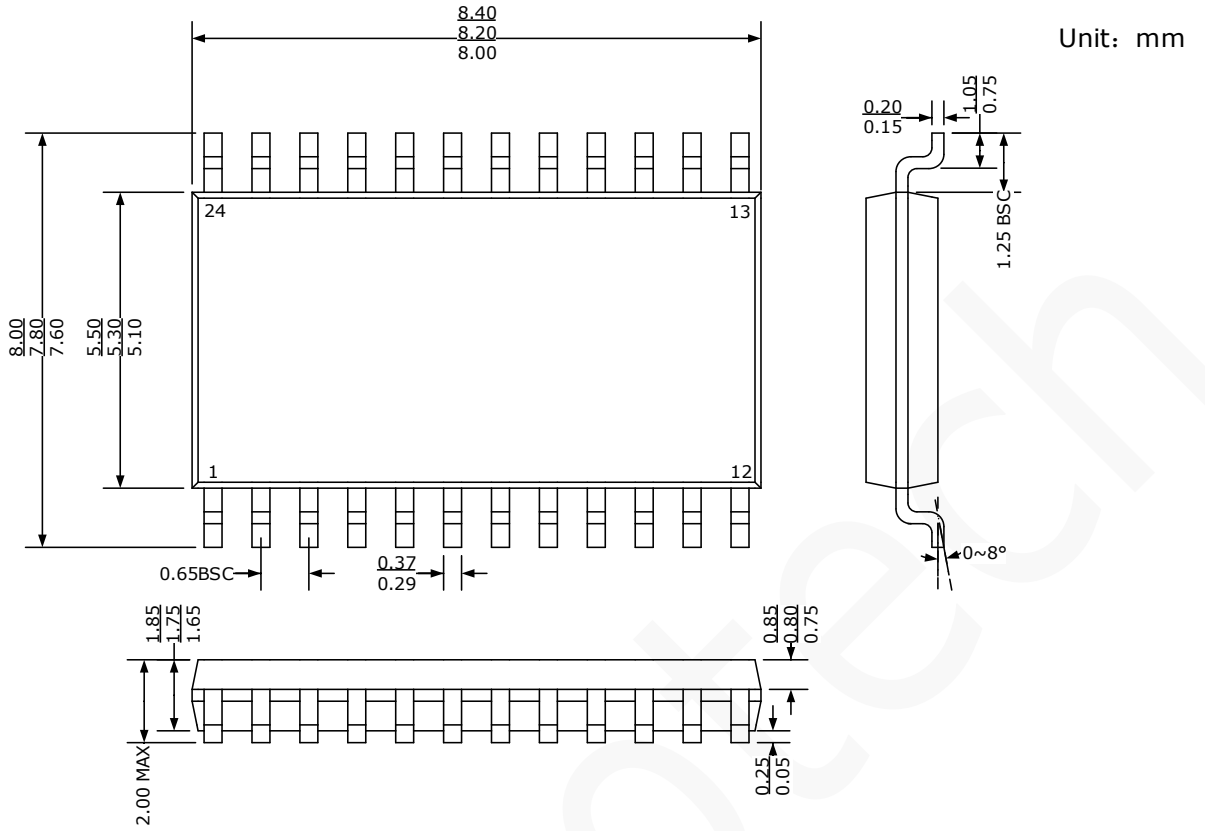
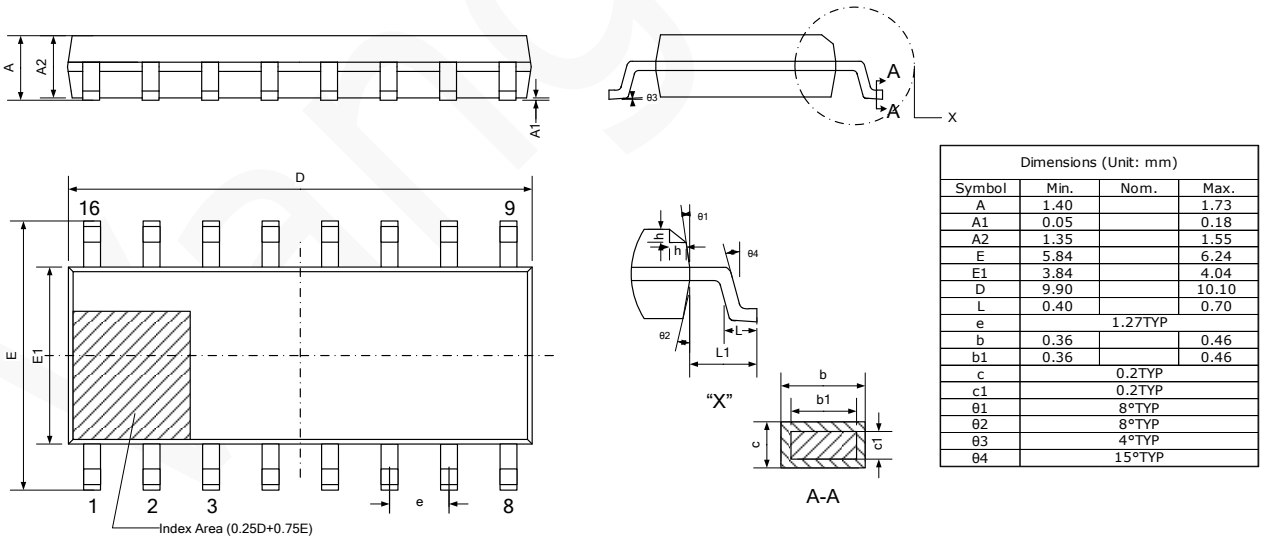
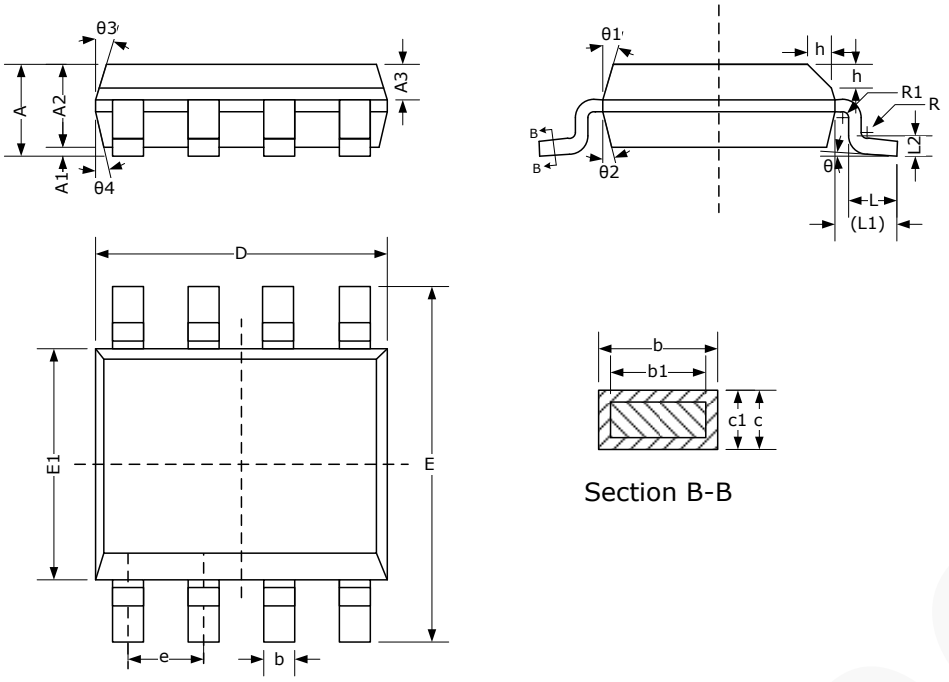


Figure 14-1 Outline dimension for V9381



Dimensions (Unit: mm)			
Symbol	Min.	Nom.	Max.
A	1.40		1.73
A1	0.05		0.18
A2	1.35		1.55
E	5.84		6.24
E1	3.84		4.04
D	9.90		10.10
L	0.40		0.70
e	1.27TYP		
b	0.36		0.46
b1	0.36		0.46
c	0.2TYP		
c1	0.2TYP		
θ1	8°TYP		
θ2	8°TYP		
θ3	4°TYP		
θ4	15°TYP		

Figure 14-2 Outline dimension for V9360



Dimensions (Unit: mm)

Symbol	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
θ	0°	-	8°
θ1	15°	17°	19°
θ2	11°	13°	15°
θ3	15°	17°	19°
θ4	11°	13°	15°

Figure 14-3 Outline dimension for V9340/V9340T