V84XXX

User Manual

Specifications are subject to change without notice.

V84XXX is based on ARM® 32-bit Cortex®-M4F MCU+FPU with 1024 or 5120 KB Flash, USB, 17 timers, 1 ADCs, 17 communication interfaces

Feature

■ **Core: ARM® 32-bit Cortex®-M4F CPU with FPU**

– 180 MHz maximum frequency, with a memory protection unit (MPU)

– Single-cycle multiplication and hardware division

– Floating point unit (FPU)

– DSP instructions

■ **Memories**

– 1024 Kbytes of Flash (V8410N, V8410S, V8411S, V8410C) or 5120 Kbytes (V8411N) internal flash program/data memory

– SPIM interface: (only V8410C) provides up to 16M bytes of external SPI flash memory program data memory expansion interface

– 1024 K bytes or 640 K bytes of SRAM

– External memory controller (XMC) with 2 Chip Select. Supports multiplexed NOR/PSRAM and NAND memories

– LCD parallel interface, 8080/6800 modes

■ **Clock, reset, and supply management**

– 2.6 to 3.6 V application supply and I/Os

– POR, PDR, and programmable voltage detector (PVD)

– 4 to 25 MHz crystal oscillator

– Internal 48 MHz factory-trimmed RC (accuracy 1 % at T_A = 25 °C, 2.5 % at T_A = - 40 to +85 °C), with automatic clock calibration (ACC)

– Internal 40 kHz RC oscillator with calibration

– 32 kHz oscillator with calibration

■ **Low power**

– Sleep, Stop, and Standby modes

– V_{BAT} supply for RTC and 64 16-bit backup registers

– 4 WKUP pins, can wake up from standby mode

■ **1 x 12-bit, 0.5 µs A/D converters (up to 16 channels)**

– Conversion range: 0 to 3.6V

– Triple sample-and-hold capability

– Temperature sensor

■ **DMA: 14-channel DMA controller**

– Supported peripherals: timers, ADC, I^2S, SPI, I^2C, and USART

■ **Debug mode**

– Serial wire debug (SWD) and JTAG interfaces

■ **Up to 80 fast I/O**

– 80 multi-functional bi-directional I/Os, all I/Os can be mapped to 16 external interrupt vectors and almost all 5 V-tolerant

– All fast I/Os, control registers accessable with f_{AHB} speed

■ **Up to 17 timers**

– Up to 8 x 16-bit timers + 2 x 32-bit timers, each with 4 IC/ OC/ PWM or pulse counter and quadrature (incremental) encoder input

– Up to 2 x 16-bit motor control PWM advanced timers with dead-time generator and emergency stop

– 2 x watchdog timers (Independent and Window)

– SysTick timer: a 24-bit downcounter

– 2 x 16-bit basic timers

■ **Up to 17 communication interfaces**

– Up to 3 x I^2C interfaces (SMBus/PMBus)

– Up to 8 x USARTs (ISO7816 interface, LIN, IrDA capability, modem control)

– Up to 4 x SPIs (36 Mbit/s), all with I^2S interface multiplexed

– CAN interface (2.0B Active)

– USB 2.0 full speed interface

■ **CRC calculation unit**

■ **Packages**

– QFN48 7 x 7 mm (V8411S)

– LQFP100 14 x 14 mm (V8410N, V8411N)

– LQFP128 14 x 14 mm (V8410C)

Table 1 Device summary

Internal Flash	SPIM	Model
1024 Kbytes	Not support	V8410N
5120 Kbytes	Not support	V8411N
1024 Kbytes	Not support	V8411S
1024 Kbytes	support	V8410C

Contents

List of Tables

List of figures

Revision History

Revision	Date	Description
1.0	Sep.23,2020	Initial Version
1.1	Jan.11,2021	Delete TRACESWO function
1.2	Jul.23,2021	V8411S support 3 SPI: SPI1, SPI2 and SPI4.
1.3	Aug.30,2021	V8411S supports 4 USART and 3 UART; Modify the pin description and package information for V8411S;
1.4	Sep.9,2021	Update LQFP100 package information
1.5	Dec.29,2021	Delete TRACESWO function
1.6	Jan.4,2022	Supplementary description: The 3-way SPI interface of V8411S is SPI1, SPI2, SPI4, without SPI3
1.7	Mar.1,2022	V8411S supports 2 USARTs and 3 UARTs; Modify V8411S pin definition diagram and package diagram; Supplement V8411S 35/36 pin description
1.8	Jul.13,2022	Update LQFP100 encapsulation data
1.9	Oct.21,2022	Increase Bit 6 description of USART_CTRL1

1 Introduction

This article gives the function information of the V84XXX series products.
The introduction of the V84XXX series must be read together with the V84XXX series product manual and the V84XXX series reference manual. About internal flash storage Information about programming, erasing and protection of the device can also be obtained in the V84XXX series reference manual. For information about the Cortex®-M4 core, please refer to The Cortex-M4 technical reference manual can be downloaded from the ARM website: http://infocenter.arm.com

2 Description

The V84XXX incorporates the high-performance ARM® Cortex®-M4F 32-bit RISC core operating at 180MHZ. The Cortex®-M4F core features a Floating point unit (FPU) single precision which supports all ARM single-precision data processing instructions and data type. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The V84XXX incorporates high-speed embedded memories (up to 1024 Kbytes or 5120 Kbytes of Flash memory, 1024 Kbytes or 640 Kbytes of SRAM), the extensive external SPI Flash (up to 16 Mbytes addressing capability), and enhanced I/Os and peripherals connected to two APB buses.

The V84XXX offers one 12-bit ADC , eight general-purpose 16-bit timers plus two general- purpose 32-bit timers, and up to two PWM timers for motor control, as well as standard and advanced communication interfaces, up to three I^2Cs, four SPIs (all multiplexed as I^2S), eight USART/UART, an USB, and a CAN

The V84XXX operates in the -40 to +85 °C temperature range, from a 2.6 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

2.1 Device overview

The V84XXX offers devices in four different package types: from 48 pins, 100 pins and 128pins. The description below gives an overview of the complete range of peripherals proposed in different devices.

Table 2 V84XXX series device function and configuration

Part Number		**V8411S**		**V8410N**		**V8411N**		**V8410C**	
CPU frequency (MHz)		180							
Int. Flash(1)	ZW (Kbytes)(2)	128	512	128	512	128	512	128	512
	NZW (Kbytes)(2)	896	512	896	512	4992	4608	896	512
	Total (Kbytes)	1024		1024		5120		1024	
SRAM (Kbytes)(2)		1024	640	1024	640	1024	640	1024	640
SPIM(3)			-	-		-		1	

Timers	Advanced-control	2			
	32-bit general- purpose	2			
	16-bit general- purpose	8			
	Basic	2			
	SysTick	1			
	IWDG	1			
	WWDG	1			
	RTC	1			
Communication	I^2C	1	3		
	SPI/I^2S	3/3	4/4		
	USART+UART	2+3	4+4		
	USB Device	1	1		
	CAN	0	1		
Analog	12-bit ADC numbers/channels	1/16			
GPIOs		42	80		
XMC		1			
Operating temperatures		-40 to +85 °C			
Packages		QFN48 7 x 7 mm	LQFP100 14 x 14 mm	LQFP100 14 x 14 mm	LQFP128 14 x 14 mm

(1) ZW = zero wait-state, up to SYSCLK 180MHZ NZW = non-zero wait-state

(2) Support the allocation of flash memory and SRAM by selecting byte settings.

(3) SPIM = External SPI Flash memory extension (for both program execution and data storage) with encryption capability.

2.2 Overview

The ARM Cortex®-M4F with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

2.2.1 ARM® Cortex®-M4F with FPU core and DSP instruction set

The ARM Cortex®-M4F with FPU 32-bit RISC processor features exceptional code efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software

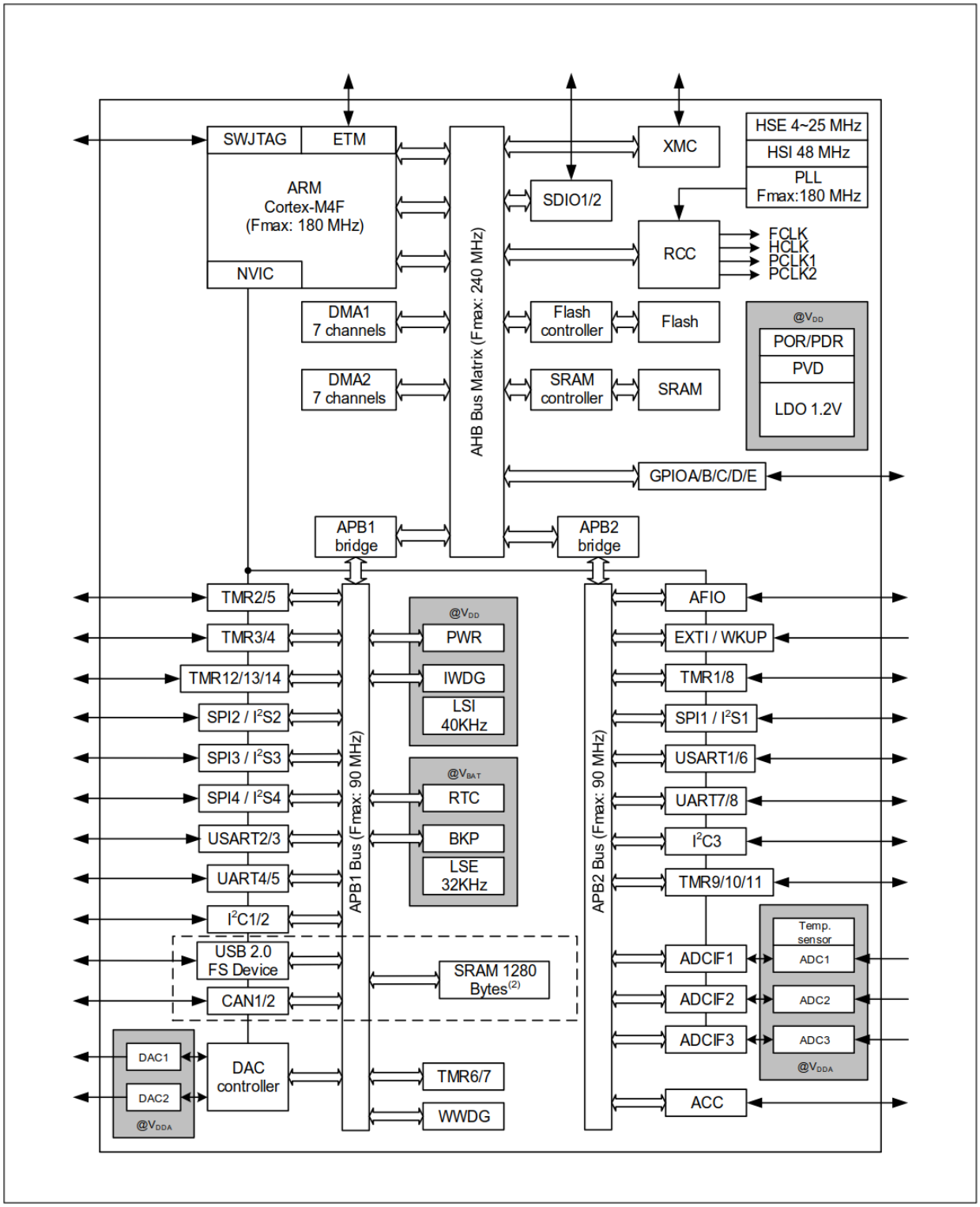
development by using meta language development tools, while avoiding saturation.

With its embedded ARM core, the V84XXX is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the V84XXX.

Note:Cortex®-M4F with FPU is binary compatible with Cortex®-M3.

Figure 1 V84XXX block diagram



2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is

organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.3 Flash memory

Up to 1024 Kbytes or 5120 Kbytes of embedded Flash is available for storing programs and data.

The V8410C provides extra interface called SPIM (SPI memory), which interfaces the external SPI Flash memory storing programs and data. With maximum 16 Mbytes addressing capability, SPIM can be used as an extensive Flash memory Bank 3.

2.2.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32- bit data word and a fixed generator polynomial among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

2.2.5 Embedded SRAM

Up to 1024 Kbytes or 640 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.6 External memory controller (XMC)

The XMC is embedded in the V84XXX. It has two Chip Select outputs supporting the following modes: multiplexed PSRAM/NOR and 16/8-bit NAND memory.

Function overview:

- Write FIFO
- Code execution from external memory of the multiplexed PSRAM/NOR

2.2.7 LCD parallel interface

The XMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD

modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.8 Nested vectored interrupt controller (NVIC)

The V84XXX embed a nested vectored interrupt controller able to manage 16 priority levels and handle up to 66 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.9 External interrupt/event controller (EXTI)

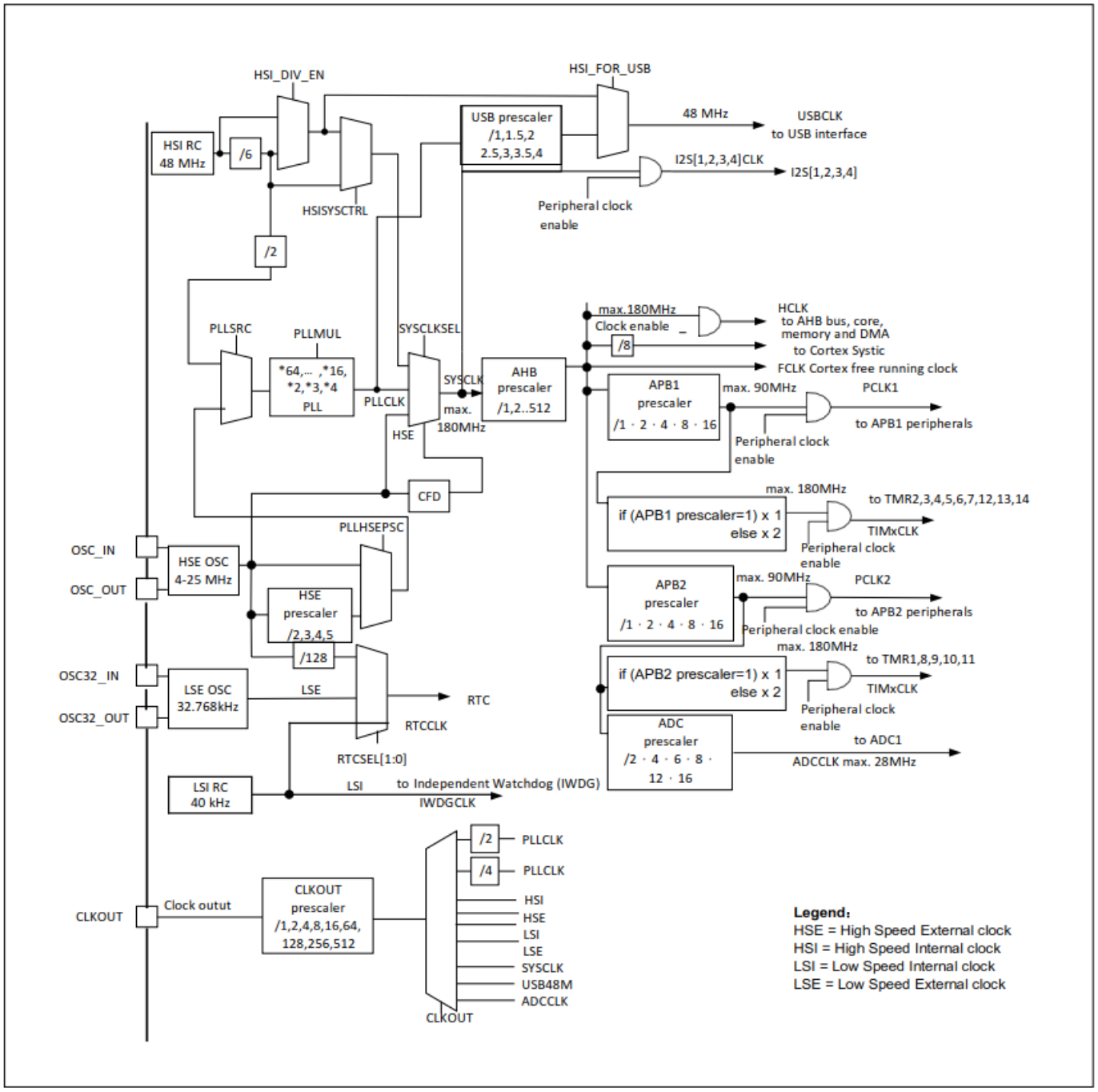
The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.2.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 48 MHz oscillator (HSI) through a divided-by-6 divider (8 MHz) is selected as default CPU clock on reset. An external 4 to 25 MHz clock (HSE) can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Multiple prescalers allow the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 180MHZ. The maximum allowed frequency of the APB domains are 90 MHz See *Figure 2* for details on the clock tree.

Figure 2 Clock tree



(1) When using USB function and its clock source is from PLL, CPU frequency must be 48 MHz, 72 MHz, 96 MHz, 120 MHz, 144 MHz, or 168 MHz;

2.2.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash. By default, boot from Flash memory bank 1 is selected. User can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is stored in system memory. The flash memory can be reprogrammed via USART1, USART2, or USB . *Table 3* provides the supporting interfaces of the bootloader to different V84XXX part

numbers and pin configurations.

Table 3 The bootloader supporting part numbers and pin configurations

Interface	Pin
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PD5: USART2_TX (remapped) PD6: USART2_RX (remapped)
USB	PA11: USB_DM PA12: USB_DP

2.2.12 Power supply schemes

● V_{DD} = 2.6～3.6 V: external power supply for I/Os and the internal regulator provided externally through V_{DD} pins.

● V_{DDA} = 2.6～3.6 V: external analog power supplies for ADC. V_{DDA} and V_{SSA} must be connected to V_{DD} and VSS, respectively.

● V_{BAT} = 1.8～3.6 V: power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more detail on how to connect power pins, refer to *Figure 9.*

2.2.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when VDD is below a specified threshold, VPOR/PDR, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the VPVD threshold and/or when VDD is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 13* for the characteristic values of $V_{POR/PDR}$ and V_{PVD}.

2.2.14 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power down.

● Main mode (MR) is used in the nominal regulation mode (Run) and in the Stop mode

● Low-power mode (LPR) can be used in the Stop mode

● Power down mode is used in Standby mode: the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption of the regulator (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.2.15 Low-power modes

The V84XXX supports three low-power modes to achieve the best compromise between low- power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator is put in normal mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, or the USB wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.
Note: he RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.16 Direct Memory Access Controller (DMA)

The flexible 14-channel general-purpose DMAs (7 channels for DMA1 and 7 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory, and memory-to- peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic, and advanced-control timers TMRx, I^2S, and ADC.

2.2.17 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied with V_{DD}. The backup registers are sixty- four 16-bit registers used to store 128 bytes of user application data. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low- power RC oscillator, or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using a divied-by-64 output of TAMPER pin to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.18 Timers and watchdogs

The V84XXX devices include up to 2 advanced-control timers, up to 10 general-purpose timers, 2 basic timers, 2 watchdog timers, and a SysTick timer.

The table below compares the features of the advanced-control, general-purpose, and basic timers.

Table 4 Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TMR1, TMR8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TMR2, TMR5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR3, TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR9, TMR12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TMR10, TMR11, TMR13, TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TMR6, TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timers (TMR1 and TMR8)

The two advanced-control timers (TMR1 and TMR8) can each be seen a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted

dead-times. They can also be seen as a complete general- purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR timers which have the same architecture. The advanced-control timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

General-purpose timers (TMRx)

There are 10 synchronizable general-purpose timers embedded in the V84XXX.

- **TMR2, TMR3, TMR4, and TMR5**

The V84XXX has 4 full- featured general-purpose timers: TMR2, TMR3, TMR4, and TMR5.The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They all feature four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs.

The TMR2, TMR3, TMR4, and TMR5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers via the link feature for synchronization or event chaining. In debug mode, their counter can be frozen. Any of these general-purpose timers can be used to generate PWM outputs.

The TMR2, TMR3, TMR4, and TMR5 are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TMR9 and TMR12**

TMR9 and TMR12 are based on a 16-bit auto-reload up-counter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

- TMR10, TMR11, TMR13, and TMR14

These timers are based on a 16-bit auto-reload up-counter, a 16-bit prescaler, and one independent channels for input capture/output compare, PWM, or one-pulse mode output.

They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured

general- purpose timers. They can also be used as simple time bases.

Basic timers (TMR6 and TMR7)

These two timers can be used as a generic 16-bit time base.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.19 Inter-integrated-circuit interface (I^2C)

Up to 3 I^2C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.20 Universal synchronous/asynchronous receiver transmitters (USART)

The V84XXX embeds 4 universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3, and USART6) and 4 universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These eight interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability.

These eight interfaces are able to communicate at speeds of up to 5.625 Mbit/s.
USART1, USART2, and USART3 provide hardware management of the CTS and RTS signals. USART1, USART2, USART3, and USART6 also provide Smart Card mode (ISO7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 5 USART/UART feature comparison

USART/UART name	USART1	USART2	USART3	UART4	UART5	USART6	UART7	UART8
Hardware flow control for modem	Yes	Yes	Yes	-	-	-	-	-
Continuous communication using DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multiprocessor communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Synchronous mode	Yes	Yes	Yes	-	-	Yes	-	-
Smartcard mode	Yes	Yes	Yes	-	-	Yes	-	-
Single-wire half-duplex communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IrDA SIR ENDEC block	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LIN mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.2.21 Serial peripheral interface (SPI)

Up to four SPIs are able to communicate up to 36 Mbits/s in slave and master modes in full- duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC modes.

All SPIs can be served by the DMA controller.

2.2.22 Inter-integrated sound interface (I^2S)

Four standard I^2S interfaces (multiplexed with SPI) are available, that can be operated in master or slave mode in half-duplex mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external CODEC at 256 times the sampling frequency.

2.2.23 Controller area network (CAN)

Two CANs are compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.2.24 Universal serial bus (USB)

V84XXX embeds a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software- configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL.

2.2.25 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current- capable.

The I/Os alternate function configuration can be locked, if needed, in order to avoid spurious writing to the I/Os registers by following a specific sequence.

2.2.26 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 6*; it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the V84XXX reference manual for software considerations.

2.2.27 Analog to digital converter (ADC)

Three 12-bit analog-to-digital converters are embedded into V84XXX devices and they share up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced-control timers (TMR1 and TMR8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.2.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.6 V ≤ V_{DDA} ≤ 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure 3 V8411S QFN48 pinout

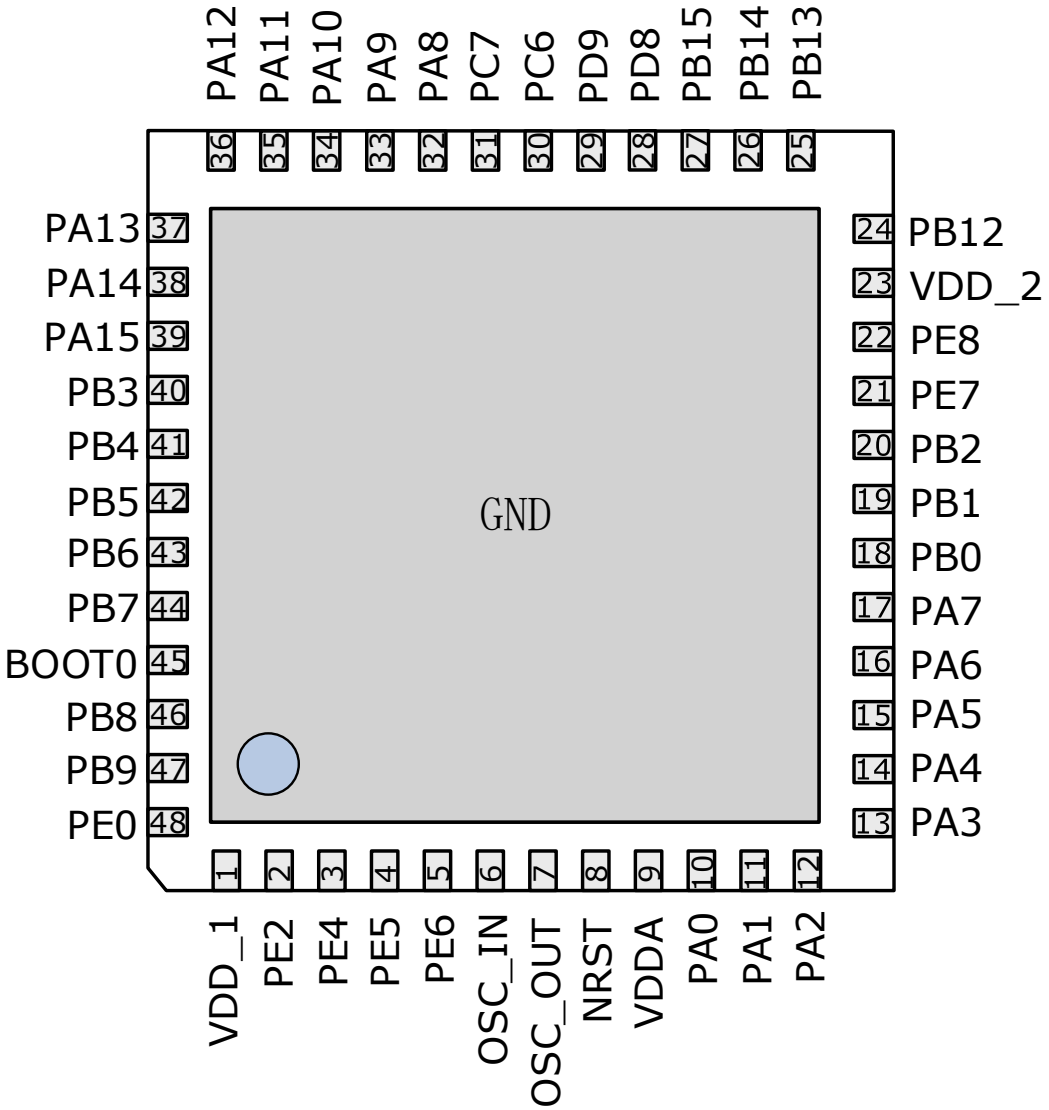


Figure 4 V8410N/V8411N LQFP100 pinout

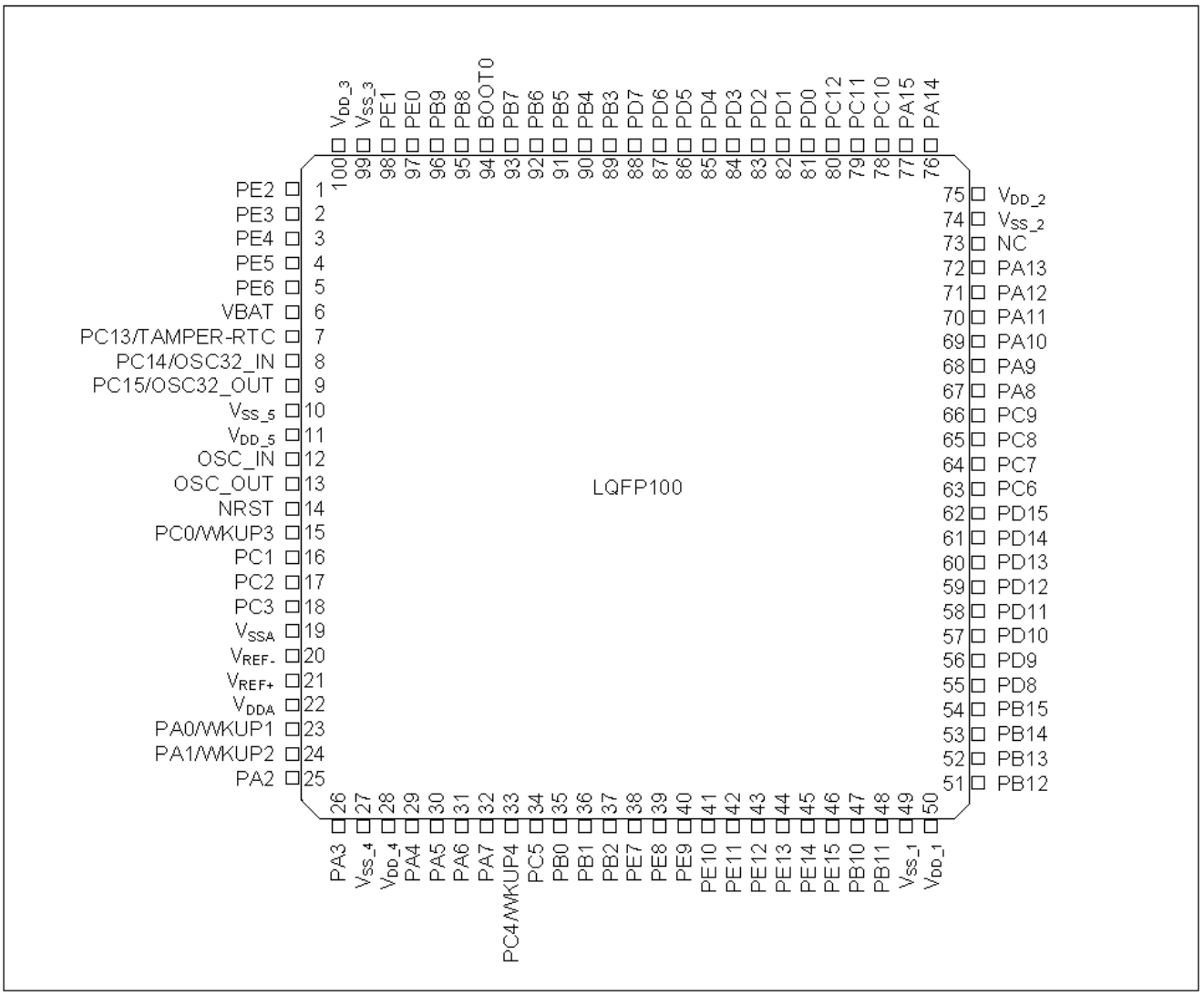
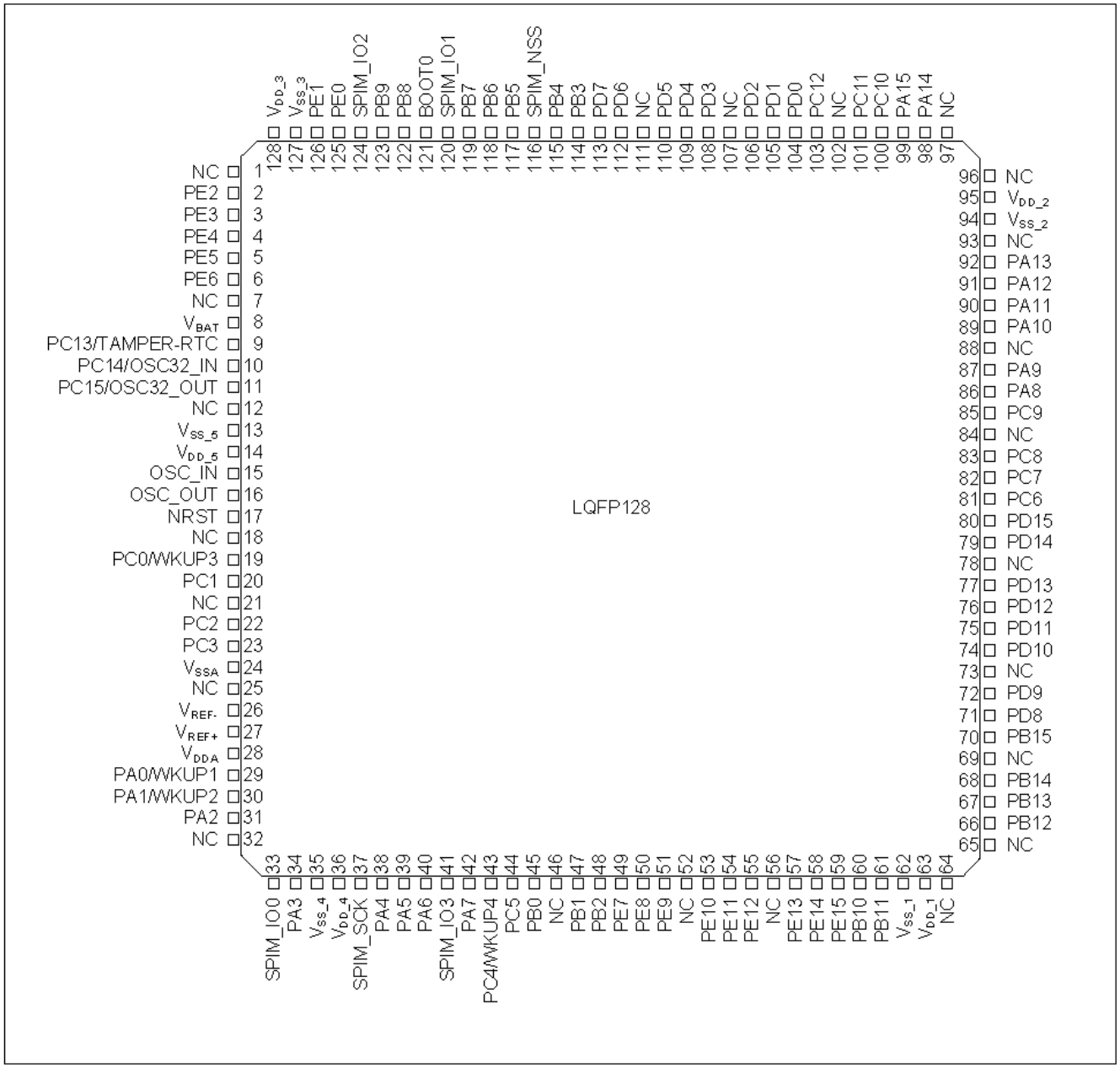


Figure 5 V8410C LQFP128 pinout



The following table is the pin definition of V84XXX series. The multiplexing functions are arranged in order of priority. The basic principle is that the analog signal is higher than the digital signal, and the output digital signal is higher than the input digital signal.

Table 6 V84XXX series pin definitions

Pin number			Pin name	Type (1)	IO lever (2)	Main function (3)	Alternate functions (4)	
V8410N/ V8411N	V8410C	V8411S					Default Remap	Default Remap
-	1		NC	not connected				
1	2	2	PE2	I/O	FT	PE2	SPI4_SCK(7)/ I2S4_CK(7)/ XMC_A23/ TRACECK	-
2	3		PE3	I/O	FT	PE3	XMC_A19/ TRACED0	-
3	4	3	PE4	I/O	FT	PE4	SPI4_NSS(7)/ I2S4_WS(7)/ XMC_A20/ TRACED1	-
4	5	4	PE5	I/O	FT	PE5	SPI4_MISO(7)/ XMC_A21/ TRACED2	TMR9_CH1
5	6	5	PE6	I/O	FT	PE6	SPI4_MOSI(7)/ I2S4_SD(7)/ XMC_A22/ TRACED3	TMR9_CH2
-	7		NC	not connected				
6	8		VBAT	S	-	VBAT	-	-
7	9		TAMPER-RTC/ PC13 (5)	I/O	TC	PC13 (6)	TAMPER-RTC	-
8	10		OSC32_IN/ PC14(5)	I/O	TC	PC14(6)	OSC32_IN	-
9	11		OSC32_OUT/ PC15(5)	I/O	TC	PC15	OSC32_OUT	-
-	12		NC	not connected				
10	13		VSS_5	S	-	VSS_5	-	-
11	14		VDD_5	S	-	VDD_5	-	-
12	15	6	OSC_IN	I/O	TC	OSC_IN	-	-
13	16	7	OSC_OUT	I/O	TC	OSC_OUT	-	-
14	17	8	NRST	I/O	-	NRST	-	-
-	18		NC	not connected				
15	19		PC0/ WKUP3	I/O	FTa	PC0	ADC1_IN10 / WKUP3	-
16	20		PC1	I/O	FTa	PC1	ADC1_IN11	-
-	21		NC	not connected				
17	22		PC2	I/O	FTa	PC2	ADC1_IN12	UART8_TX / XMC_NWE
18	23		PC3	I/O	FTa	PC3	ADC1_IN13 / XMC_A0	UART8_RX
19	24		VSSA	S	-	VSSA	-	-
-	25		NC	not connected				
20	26		VREF-	S	-	VREF-	-	-
21	27		VREF+	S	-	VREF+	-	-
22	28	9	VDDA	S	-	VDDA	-	-
23	29	10	PA0 / WKUP1	I/O	TC	PA0	ADC1_IN0 / WKUP1/ USART2_CTS(7)/ TMR2_CH1(7) / TMR2_ETR(7)/	UART4_TX

							TMR5_CH1 / TMR8_ETR	
24	30	11	PA1 / WKUP2	I/O	FTa	PA1	ADC1_IN1 / WKUP2/ USART2_RTS(7)/ TMR2_CH2(7) / TMR5_CH2	UART4_RX
25	31	12	PA2	I/O	FTa	PA2	ADC1_IN2 / USART2_TX(7)/ TMR2_CH3(7) / TMR5_CH3/ TMR9_CH1(7)	XMC_D4
-	32		NC	not connected				
-	33		SPIM_IO0	I/O	TC	SPIM_IO0	-	-
26	34	13	PA3	I/O	FTa	PA3	ADC1_IN3 / USART2_RX(7)/ TMR2_CH4(7) / TMR5_CH4/ TMR9_CH2(7)	I2S2_MCK / XMC_D5
27	35		VSS_4	S	-	VSS_4	-	-
28	36		VDD_4	S	-	VDD_4	-	-
-	37		SPIM_SCK	O	TC	SPIM_SCK	-	-
29	38	14	PA4	I/O	FTa	PA4	ADC1_IN4 / USART2_CK(7)/ SPI1_NSS(7) / I2S1_WS(7)	USART6_TX /SPI3_NSS(9) / I2S3_WS /XMC_D6
30	39	15	PA5	I/O	FTa	PA5	ADC1_IN5 /SPI1_SCK(7)/ I2S1_CK(7)	USART6_RX /XMC_D7
31	40	16	PA6	I/O	FTa	PA6	ADC1_IN6 / SPI1_MISO(7)/ TMR3_CH1(7) / TMR8_BKIN/ TMR13_CH1	I2S2_MCK / TMR1_BKIN
-	41		SPIM_IO3	I/O	TC	SPIM_IO3	-	-
32	42	17	PA7	I/O	FTa	PA7	ADC1_IN7/ SPI1_MOSI(7) / I2S1_SD(7)/ TMR3_CH2(7) / TMR8_CH1N/ TMR14_CH1	TMR1_CH1N
33	43		PC4/ WKUP4	I/O	FTa	PC4	ADC1_IN14/ WKUP4/ XMC_NE4	-
34	44		PC5	I/O	FTa	PC5	ADC1_IN15	XMC_NOE
35	45	18	PB0	I/O	FTa	PB0	ADC1_IN8/ I2S1_MCK(7)/ TMR3_CH3(7)/ TMR8_CH2N	TMR1_CH2N
-	46		NC	not connected				
36	47	19	PB1	I/O	FTa	PB1	ADC1_IN9 /TMR3_CH4(7)/ TMR8_CH3N	TMR1_CH3N
37	48	20	PB2	I/O	FT	PB2 / BOOT1	-	-
38	49	21	PE7	I/O	FT	PE7	UART7_RX(7)/ XMC_D4(7)	TMR1_ETR
39	50	22	PE8	I/O	FT	PE8	UART7_TX(7)/ XMC_D5(7)	TMR1_CH1N
40	51		PE9	I/O	FT	PE9	XMC_D6(7)	TMR1_CH1
-	52		NC	not connected				
41	53		PE10	I/O	FT	PE10	XMC_D7(7)	TMR1_CH2N

42	54		PE11	I/O	FT	PE11	XMC_D8	SPI4_SCK/ I2S4_CK/ TMR1_CH2
43	55		PE12	I/O	FT	PE12	XMC_D9	SPI4_NSS / I2S4_WS/ TMR1_CH3N
-	56		NC	not connected				
44	57		PE13	I/O	FT	PE13	XMC_D10	SPI4_MISO / TMR1_CH3
45	58		PE14	I/O	FT	PE14	XMC_D11	SPI4_MOSI / I2S4_SD/ TMR1_CH4
46	59		PE15	I/O	FT	PE15	XMC_D12	TMR1_BKIN
47	60		PB10	I/O	FT	PB10	USART3_TX(7) / I2C2_SCL	I2S3_MCK / TMR2_CH3
48	61		PB11	I/O	FT	PB11	USART3_RX(7) / I2C2_SDA	TMR2_CH4
49	62		VSS_1	S	-	VSS_1	-	-
50	63	1	VDD_1	S	-	VDD_1	-	-
-	64		NC	not connected				
-	65		NC	not connected				
51	66	24	PB12	I/O	FT	PB12	USART3_CK(7) / I2C2_SMBA/ SPI2_NSS / I2S2_WS/ TMR1_BKIN(7)	XMC_D13
52	67	25	PB13	I/O	FT	PB13	USART3_CTS(7)/SPI2 _SCK / I2S2_CK/ TMR1_CH1N(7)	-
53	68	26	PB14	I/O	FT	PB14	USART3_RTS(7)/ SPI2_MISO/ TMR1_CH2N(7)/ TMR12_CH1	XMC_D0
-	69		NC	not connected				
54	70	27	PB15	I/O	FT	PB15	SPI2_MOSI/ I2S2_SD/ TMR1_CH3N(7)/ TMR12_CH2	-
55	71	28	PD8	I/O	FT	PD8	XMC_D13(7)	USART3_TX
56	72	29	PD9	I/O	FT	PD9	XMC_D14	USART3_RX
-	73		NC	not connected				
57	74		PD10	I/O	FT	PD10	XMC_D15	USART3_CK
58	75		PD11	I/O	FT	PD11	XMC_A16	USART3_CTS
59	76		PD12	I/O	FT	PD12	XMC_A17	USART3_RTS/ TMR4_CH1
60	77		PD13	I/O	FT	PD13	XMC_A18	TMR4_CH2
-	78		NC	not connected				
61	79		PD14	I/O	FT	PD14	XMC_D0(7)	TMR4_CH3
62	80		PD15	I/O	FT	PD15	XMC_D1(7)	TMR4_CH4
63	81	30	PC6	I/O	FT	PC6	USART6_TX(7) / I2S2_MCK(7)/ TMR8_CH1	XMC_D1 / TMR3_CH1
64	82	31	PC7	I/O	FT	PC7	USART6_RX(7)/ I2S3_MCK(7)/ TMR8_CH2	TMR3_CH2
65	83		PC8	I/O	FT	PC8	USART6_CK / I2S4_MCK(7)/ TMR8_CH3	TMR3_CH3
-	84		NC	not connected				
66	85		PC9	I/O	FT	PC9	I2C3_SDA(7) / TMR8_CH4	TMR3_CH4
67	86	32	PA8	I/O	FT	PA8	CLKOUT / USART1_CK/ I2C3_SCL /	-

							USB_SOF/ TMR1_CH1(7)	
68	87	33	PA9	I/O	FT	PA9	USART1_TX(7) / I2C3_SMBA/ TMR1_CH2(7)	-
-	88		NC	not connected				
69	89	34	PA10	I/O	FT	PA10	USART1_RX(7) / TMR1_CH3(7)	I2S4_MCK
70	90	35	PA11	I/O	TC	PA11	USB_DM / USART1_CTS/ CAN1_RX(7)/ TMR1_CH4(7)	-
71	91	36	PA12	I/O	TC	PA12	USB_DP / USART1_RTS/ CAN1_TX(7) / TMR1_ETR(7)	-
72	92	37	PA13	I/O	FT	JTMS-SWDIO	-	PA13
73	93		NC	not connected				
74	94		VSS_2	S	-	VSS_2	-	-
75	95	23	VDD_2	S	-	VDD_2	-	-
-	96		NC	not connected				
-	97		NC	not connected				
76	98	38	PA14	I/O	FT	JTCK-SWCLK	-	PA14
77	99	39	PA15	I/O	FT	JTDI	SPI3_NSS(7) (9) / I2S3_WS(7)	PA15/ SPI1_NSS / I2S1_WS/ TMR2_CH1/ TMR2_ETR
78	100		PC10	I/O	FT	PC10	UART4_TX(7)	USART3_TX/SPI3_SCK / I2S3_CK
79	101		PC11	I/O	FT	PC11	UART4_RX(7)	USART3_RX / SPI3_MISO/ XMC_D2
-	102		NC	not connected				
80	103		PC12	I/O	FT	PC12	UART5_TX(7)	USART3_CK/SPI3_MOSI/ I2S3_SD/ XMC_D3
81	104		PD0	I/O	FT	PD0	XMC_D2(7)	CAN1_RX
82	105		PD1	I/O	FT	PD1	XMC_D3(7)	CAN1_TX
83	106		PD2	I/O	FT	PD2	UART5_RX(7) / TMR3_ETR	XMC_NWE
-	107		NC	not connected				
84	108		PD3	I/O	FT	PD3	XMC_CLK	USART2_CTS
85	109		PD4	I/O	FT	PD4	XMC_NOE(7)	USART2_RTS
86	110		PD5	I/O	FT	PD5	XMC_NWE(7)	USART2_TX
-	111		NC	not connected				
87	112		PD6	I/O	FT	PD6	XMC_NWAIT	USART2_RX
88	113		PD7	I/O	FT	PD7	XMC_NE1 / XMC_NCE2	USART2_CK
89	114	40	PB3	I/O	FT	JTDO	SPI3_SCK(7) (9) / I2S3_CK(7)	PB3/ UART7_RX/ SPI1_SCK/ I2S1_CK/ TMR2_CH2
90	115	41	PB4	I/O	FT	NJTRST	SPI3_MISO(7) (9)	PB4/ SPI1_MISO / I2C3_SDA/ UART7_TX/ TMR3_CH1
-	116		SPIM_NSS	O	TC	SPIM_NSS	-	-
91	117	42	PB5	I/O	FT	PB5	SPI3_MOSI(7) (9) / I2S3_SD(7)/ I2C1_SMBA(7)	SPI1_MOSI / I2S1_SD/ TMR3_CH2
92	118	43	PB6	I/O	FT	PB6	I2C1_SCL(7) / TMR4_CH1(7)	USART1_TX/ I2S1_MCK/ SPI4_NSS/ I2S4_WS

93	119	44	PB7	I/O	FT	PB7	I2C1_SDA(7) / XMC_NADV /TMR4_CH2(7)	USART1_RX/ SPI4_SCK/ I2S4_CK
-	120		SPIM_IO1	I/O	TC	SPIM_IO1	-	-
94	121	45	BOOT0	I	-	BOOT0	-	-
95	122	46	PB8	I/O	FT	PB8	TMR4_CH3(7) / TMR10_CH1	UART5_RX/ SPI4_MISO/ I2C1_SCL / CAN1_RX
96	123	47	PB9	I/O	FT	PB9	TMR4_CH4(7) / TMR11_CH1	UART5_TX/ SPI4_MOSI/ I2S4_SD/ I2C1_SDA/ CAN1_TX
-	124		SPIM_IO2	I/O	TC	SPIM_IO2	-	-
97	125	48	PE0	I/O	FT	PE0	UART8_RX(7) / XMC_NBL0 /TMR4_ETR	-
98	126		PE1	I/O	FT	PE1	UART8_TX(7) / XMC_NBL1	-
99	127		VSS_3	S	-	VSS_3	-	-
100	128		VDD_3	S	-	VDD_3	-	-

(1) I = input, O = output, S = supply.

(2) TC = standard 3.3 V I/O, FT = general 5 V-tolerant I/O, FTa = 5 V-tolerant I/O with analog functionalities. FTa pin is 5 V- tolerant when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when configured as analog mode. Meanwhile, its input level should not higher than VDD + 0.3 V.

(3) Function availability depends on the chosen device.

(4) If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).

(5) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the normal sourcing/sinking strength should be used with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

(6) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the V84XXX reference manual.

(7) This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the V84XXX reference manual.

(8) V8411S package middle pad (GND) is grounded

(9) V8411S support 3 SPI：SPI1, SPI2 and SPI4.

Table 7 XMC pin definition

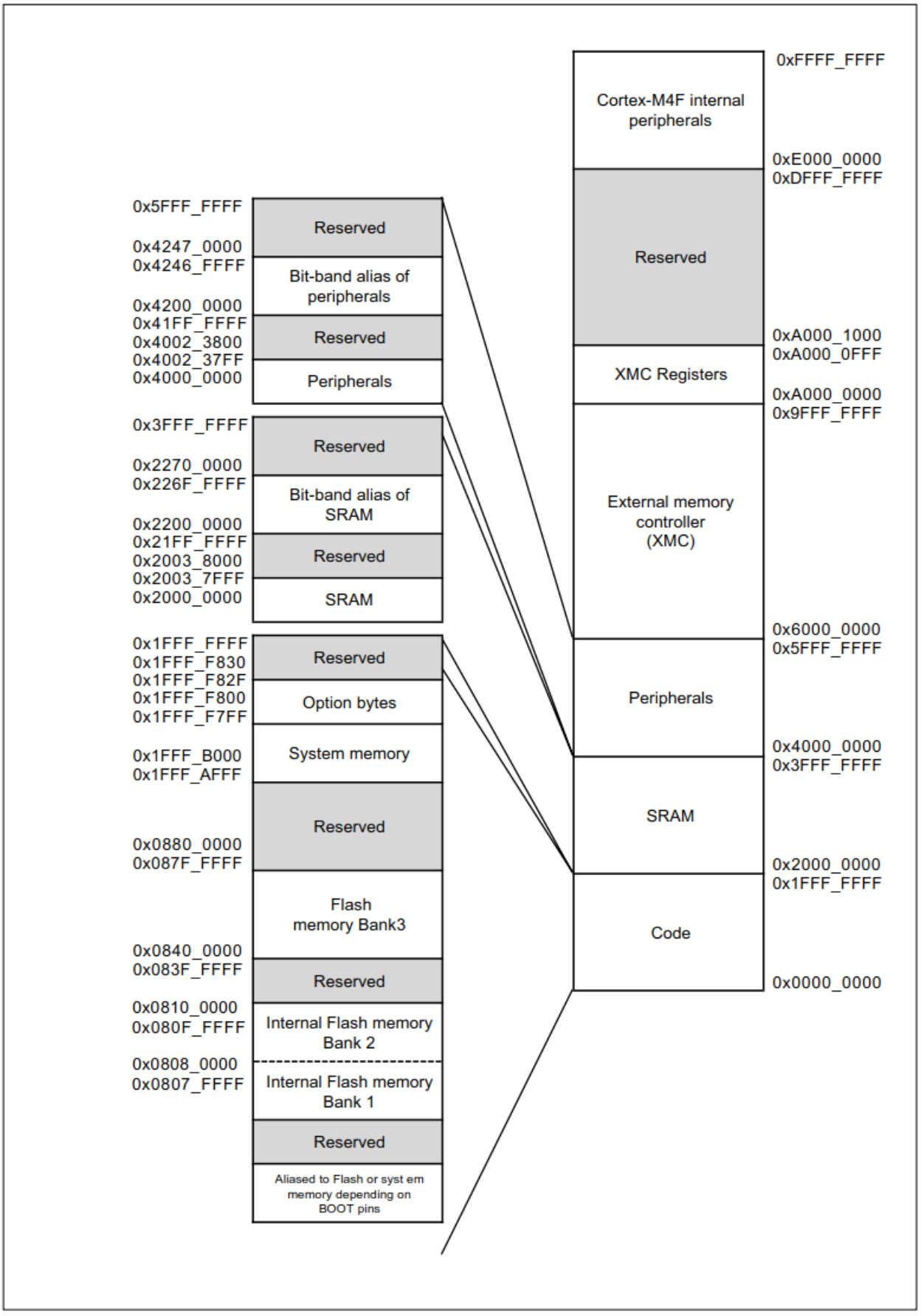
Pins	XMC		
	Multiplexed NOR/PSRAM	LCD	NAND

PE2	A23	A23	-
PE3	A19	A19	-
PE4	A20	A20	-
PE5	A21	A21	-
PE6	A22	A22	-
PC2	NWE	NWE	NWE
PC3	-	A0	-
PA2	AD4	D4	D4
PA3	AD5	D5	D5
PA4	AD6	D6	D6
PA5	AD7	D7	D7
PC4	NE4	NE4	-
PC5	NOE	NOE	NOE
PE7	AD4	D4	D4
PE8	AD5	D5	D5
PE9	AD6	D6	D6
PE10	AD7	D7	D7
PE11	AD8	D8	D8
PE12	AD9	D9	D9
PE13	AD10	D10	D10
PE14	AD11	D11	D11
PE15	AD12	D12	D12
PB12	AD13	D13	D13
PB14	AD0	D0	D0
PD8	AD13	D13	D13
PD9	AD14	D14	D14
PD10	AD15	D15	D15
PD11	A16	A16	CLE
PD12	A17	A17	ALE
PD13	A18	A18	-
PD14	AD0	D0	D0
PD15	AD1	D1	D1
PC6	AD1	D1	D1
PC11	AD2	D2	D2

PC12	AD3	D3	D3
PD0	AD2	D2	D2
PD1	AD3	D3	D3
PD2	NWE	NWE	NWE
PD3	CLK	-	-
PD4	NOE	NOE	NOE
PD5	NWE	NWE	NWE
PD6	NWAIT	-	NWAIT
PD7	NE1	NE1	NCE2
PB7	NADV	-	-
PE0	NBL0	-	-
PE1	NBL1	-	-

4 Memory mapping

Figure 6 Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production with an ambient temperature at T_A = 25 °C and T_A = T_A max.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V. They are given only as design guidelines and are not tested.

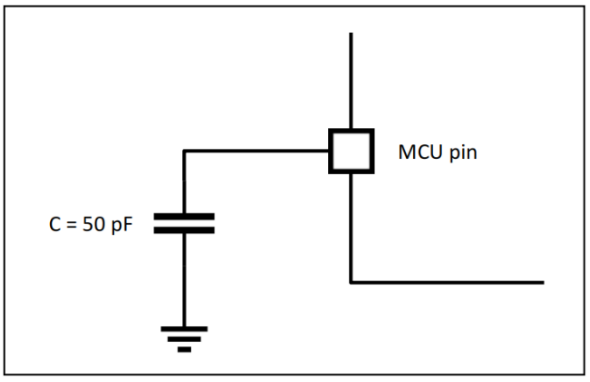
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

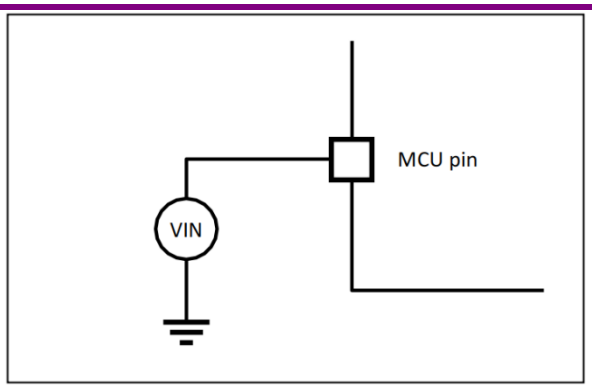
Figure 7 Pin loading conditions



5.1.5 Pin input voltage

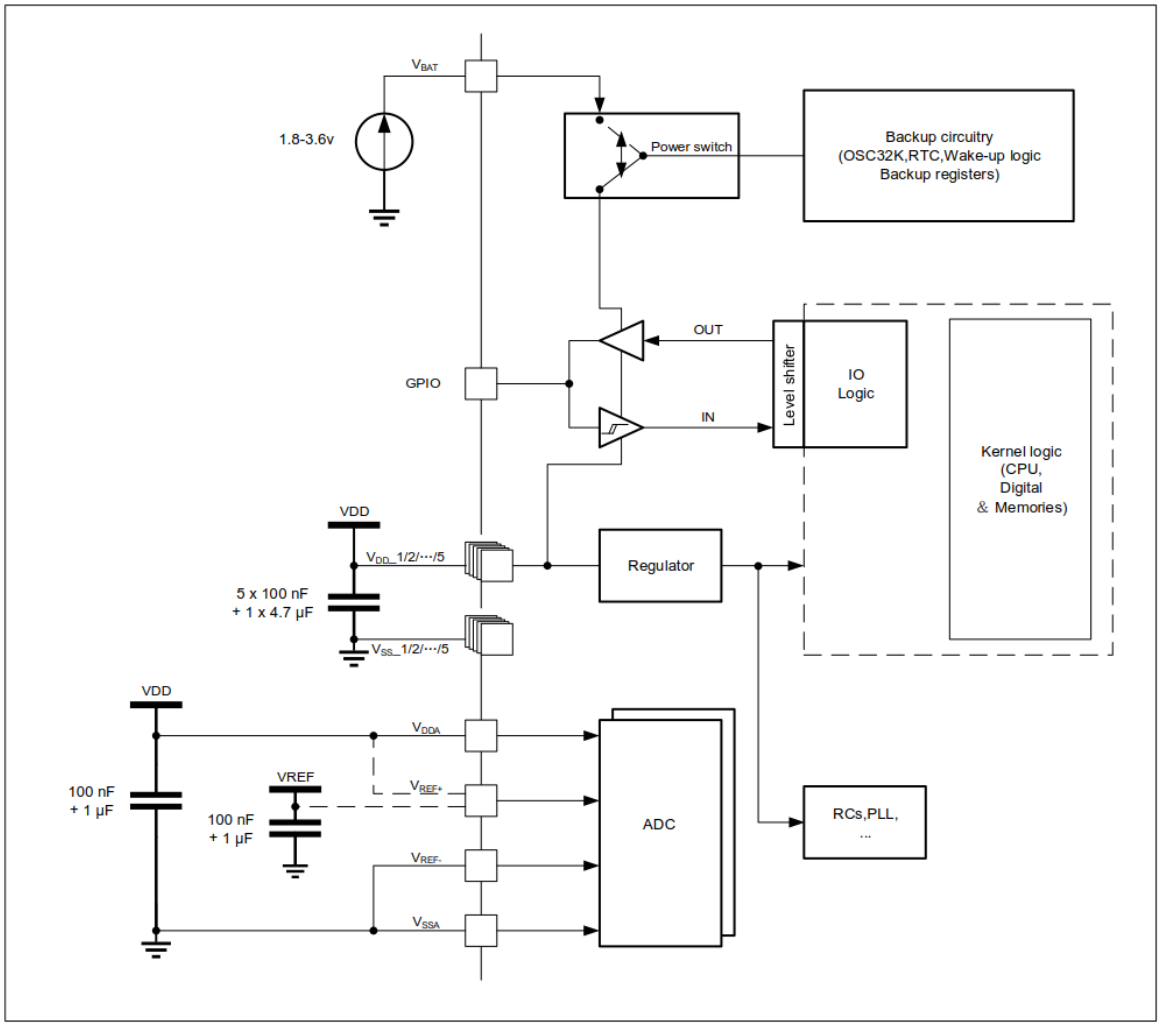
The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 8 Pin input voltage



5.1.6 Power supply scheme

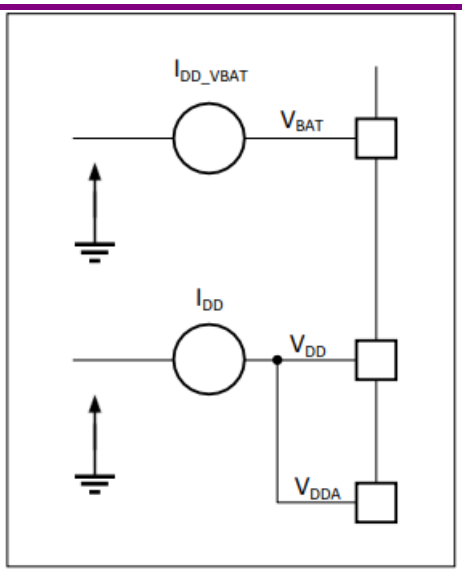
Figure 9 Power supply scheme



Caution: In this figure, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 10 Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 8*,*Table 9*,and*Table 10* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on FT I/O	V_{SS}-0.3	6.0	
	Input voltage on FTa I/O (set as input floating, input pull-up, or input pull-down mode)			
	Input voltage on TC I/O	V_{SS}-0.3	4.0	
	Input voltage on FTa I/O (set as analog mode)			
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins (2)	-	50	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(2) V_{REF-} included.

Table 9 Current characteristics

Symbol	Ratings	Max	Unit

I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 10 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	105	

5.3 Operating conditions

5.3.1 General operating conditions

Table 11 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	V8410N/V8411N/V8411S V8410C not use SPIM	0	180	MHz
		V8410C use SPIM	0	120	
f_{PCLK1}	Internal APB1 clock frequency	-	0	90	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	90	MHz
V_{DD}	Standard operating voltage	-	2.6	3.6	V
V_{DDA}(1)	Analog operating voltage	Must be the same potential as V_{DD}(1)	2.6	3.6	V
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
P_D	Power dissipation: T_A = 85 °C	-	-	373	mW
T_A	Ambient temperature	-	-40	85	°C

(1): It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Operating conditions at power-up / power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in *Table 11*.

Table 12 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞(1)	ms/V

	V_{DD} fall time rate	-	20	∞	μs/V

(1)If V_{DD} rising time rate is slower than 120 ms/V, the code should access the backup registers after V_{DD} higher than V_{POR} + 0.1V.

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 11*.

Table 13 Embedded reset and power control block characteristics

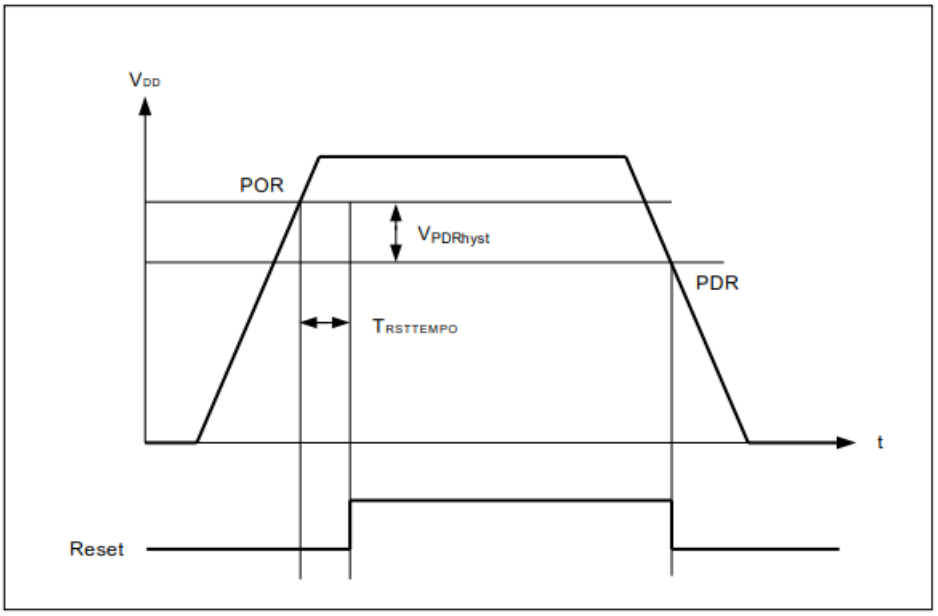
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0] = 001 (rising edge)(1)	2.19	2.28	2.37	V
		PLS[2:0] = 001 (falling edge)(1)	2.09	2.18	2.27	V
		PLS[2:0] = 010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0] = 010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0] = 011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0] = 011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0] = 100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0] = 100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0] = 101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0] = 101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0] = 110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0] = 110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0] = 111 (rising edge)	2.76	2.88	3	V
		PLS[2:0] = 111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.85(3)	2.0	2.24	V
		Rising edge	2.03	2.16	2.42	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	160	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	EOPB0=1	-	70	-	ms
		EOPB0=0	-	270	-	

(1) PLS[2:0] = 001 may be not available for its voltage detector level may be lower than $V_{POR/PDR}$.

(2) Guaranteed by design, not tested in production.

(3) The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

Figure 11 Power on reset/power down reset waveform



5.3.4 Embedded reference voltage

The parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 11*.

Table 14 Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
T_{Coeff}(2)	Temperature coefficient	-	-100	-	100	ppm/°C

(1)Shortest sampling time can be determined in the application by multiple iterations.

(2)Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, and executed binary code.

The current consumption is measured as described in *Figure 11*.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled except when explicitly mentioned
- Prefetching in ON (reminder: this bit must be set before clock setting and bus pre-scaling

- When the peripherals are enabled:

– $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$ if $f_{HCLK} > 90$ MHz

– $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$ if $f_{HCLK} \leq 90$ MHz

- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*.

Table 15 Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(2)	180 MHz	57.6	33	mA
			144 MHz	46.6	26.8	
			100MHz	35.5	20.7	
			72 MHz	28.2	15.1	
			48 MHz	19.5	10.8	
			36 MHz	15.2	8.6	
			24 MHz	10.8	6.45	
			16 MHz	7.93	5.01	
			8 MHz	4.59	3.14	
			4 MHz	3.2	2.48	
			2 MHz	2.51	2.15	
			1 MHz	2.17	1.99	
			500 kHz	1.99	1.91	
			125 kHz	1.86	1.84	
		Running on high speed internal RC (HSI)	180 MHz	57.4	32.8	mA
			144 MHz	46.4	26.7	
			100 MHz	35.4	20.5	
			72 MHz	28.1	15	
			48 MHz	19.4	10.7	
			36 MHz	15.1	8.5	
			24 MHz	10.7	6.34	
			16 MHz	7.82	4.9	
			8 MHz	4.48	3.03	
			4 MHz	3.1	2.37	
			2 MHz	2.4	2.04	
			1 MHz	2.06	1.88	
			500KHz	1.88	1.79	

			125KHz	1.75	1.73	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

(2) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 16 Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(2)	180 MHz	41.9	9.75	mA
			144 MHz	34	8.23	
			100 MHz	26.1	6.7	
			72 MHz	21.9	5.82	
			48 MHz	15.3	4.59	
			36 MHz	12	3.97	
			24 MHz	8.73	3.36	
			16 MHz	6.53	2.95	
			8 MHz	3.89	2.11	
			4 MHz	2.86	1.97	
			2 MHz	2.34	1.89	
			1 MHz	2.08	1.86	
			500 KHz	1.95	1.84	
			125KHz	1.86	1.83	
		Running on high speed internal RC (HSI)	180 MHz	41.8	9.65	mA
			144 MHz	33.9	8.12	
			100 MHz	25.9	6.6	
			72 MHz	21.8	5.72	
			48 MHz	15.2	4.48	
			36 MHz	11.9	3.87	
			24 MHz	8.62	3.26	
			16 MHz	6.42	2.85	
			8 MHz	3.78	2	
			4 MHz	2.75	1.86	
			2 MHz	2.23	1.79	
			1 MHz	1.97	1.75	
			500KHz	1.85	1.73	
			125KHz	1.75	1.72	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

(2) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled except when explicitly mentioned
- prefetching in ON (reminder: this bit must be set before clock setting and bus pre-scaling
- When the peripherals are enabled:

– $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$ if $f_{HCLK} > 90$ MHz

– $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$ if $f_{HCLK} \leq 90$ MHz

The parameters given in *Table 17* and *Table 18* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*.

Table 17 Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	MAX(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Run mode	xternal clock(2), all peripherals enabled	180 MHz	68.2	mA
			144 MHz	57.2	
			100 MHz	46	
			72 MHz	38.8	
			48 MHz	29.9	
			36 MHz	25.5	
			24 MHz	21	
			16 MHz	18.1	
			8 MHz	14.7	
		External clock(2), all peripherals disabled	180 MHz	43.1	mA
			144 MHz	37	
			100 MHz	30.8	
			72 MHz	25.2	
			48 MHz	20.9	
			36 MHz	18.7	
			24 MHz	16.5	
			16 MHz	15	
			8 MHz	13.2	

(1) Guaranteed by characterization results, not tested in production.

(2) External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 18 Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	MAX(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	180 MHz	52.5	mA
			144 MHz	44.5	
			100 MHz	36.5	
			72 MHz	32.3	
			48 MHz	25.6	
			36 MHz	22.2	
			24 MHz	18.8	
			16 MHz	16.6	
			8 MHz	13.8	
		External clock(2), all peripherals disabled	180 MHz	19.8	mA
			144 MHz	18.2	
			100 MHz	16.7	
			72 MHz	15.8	
			48 MHz	14.5	
			36 MHz	13.9	
			24 MHz	13.3	
			16 MHz	12.8	
			8 MHz	12	

(1) Guaranteed by characterization results, not tested in production.

(2) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 19 Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		MAX(2)	Unit
			V_{DD}/V_{BAT} = 2.6 V	V_{DD}/V_{BAT} = 3.3 V	T_A =85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	1.13	1.13	12.27	mA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	1.11	1.11	11.79	
	Supply current	Low-speed oscillator and RTC OFF	4.02	5.82	10.2	

	in Standby mode	Low-speed oscillator and RTC ON	4.55	7.18	11.5	μA

(1) Typical values are measured at T_A = 25 °C.

(2) Guaranteed by characterization results, not tested in production.

Figure 12 Typical current consumption in Stop mode vs. temperature at different V_{DD}

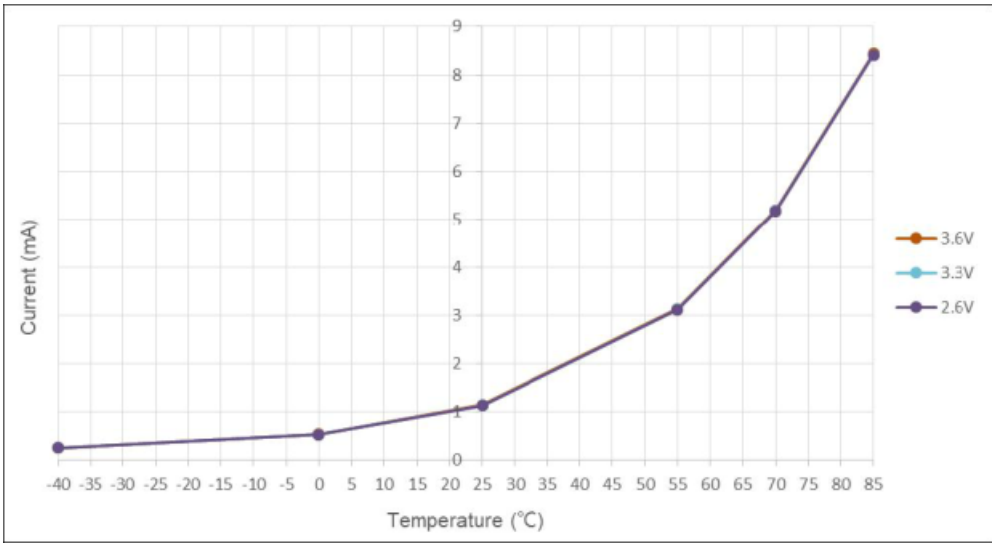


Figure 13 Typical current consumption in Standby mode vs. temperature at different V_{DD}

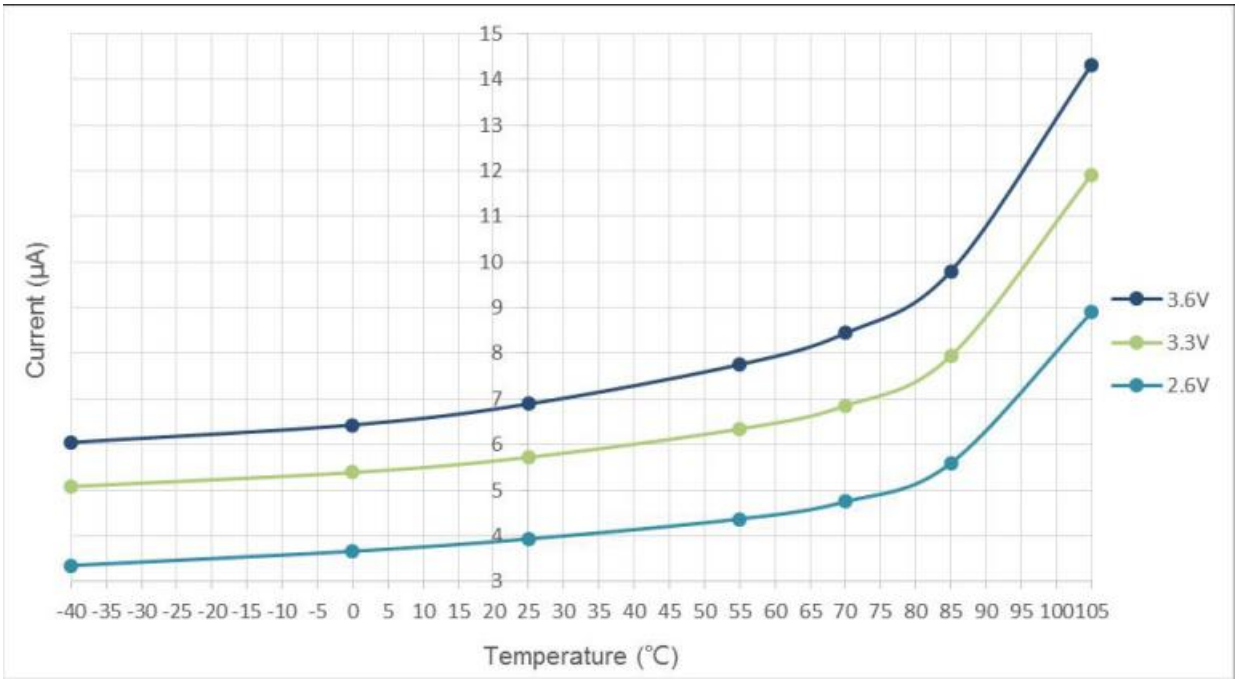


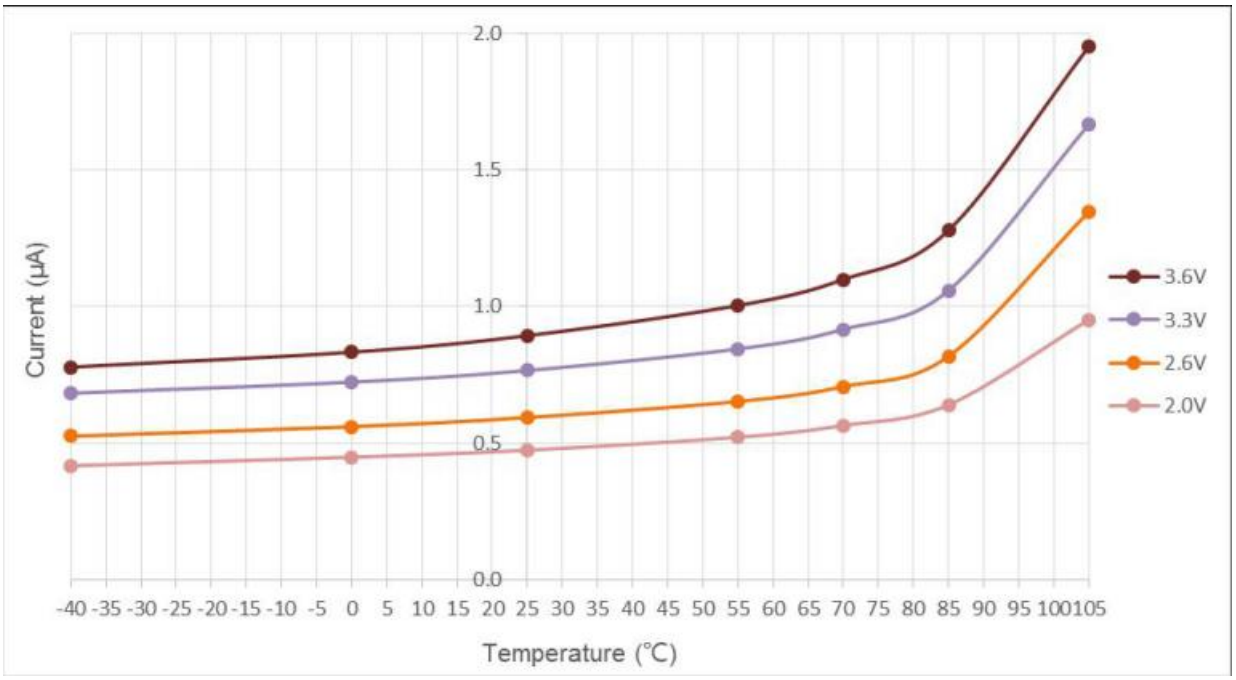
Table 20 Typical and maximum current consumptions on V_{BAT}

Symbol	Parameter	Conditions	Typ(1)			MAX(2)	Unit
			V_{BAT} = 2.0 V	V_{BAT} = 2.6 V	V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD_VBAT}	Supply current of backup domain	Low-speed oscillator and RTC ON, $V_{DD} < V_{PDR}$	0.41	0.50	0.63	1.13	μA

(1) Typical values are measured at T_A = 25 °C.

(2) Guaranteed by characterization results, not tested in production.

Figure 14 Typical current consumption on V_{BAT} with LSE and RTC on vs. temperature at different V_{BAT}



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 21*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled except when explicitly mentioned
- The given value is calculated by measuring the current consumption

– with all peripherals clocked off

– with only one peripheral clocked on

- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*.

Table 21 Peripheral current consumption

Peripheral		Typ	Unit
AHB (up to 180MHZ)	DMA1	3.5	μA/MHz
	DMA2	3.01	
	GPIOA	2.24	
	GPIOB	1.97	
	GPIOC	0.8	
	GPIOD	1.67	
	GPIOE	1.7	
	XMC	9.09	
	CRC	1.6	

APB1 (up to 90 MHz)	TMR2	9.07	
	TMR3	7.16	
	TMR4	7.77	
	TMR5	10.2	
	TMR6	1.19	
	TMR7	1.08	
	TMR12	4.31	
	TMR13	3.03	
	TMR14	2.9	
	SPI2/I2S2	2.96	
	SPI3/I2S3	2.33	
	SPI4/I2S4	2.29	
	USART2	2.22	
	USART3	2.15	
	UART4	2.15	
	UART5	2.15	
	I2C1	2.01	
	I2C2	1.94	
	USB	9.69	
	CAN	5.56	
	WWDG	0.66	
	PWR	0.87	
	BKP	28.1	
APB2 (up to 90 MHz)	AFIO	0.72	
	SPI1/I2S1	3.18	
	USART1	2.29	
	USART6	2.27	
	UART7	2.29	
	UART8	2.43	
	I2C3	1.81	
	TMR1	9.28	
	TMR8	9.06	
	TMR9	3.87	
	TMR10	2.76	
	TMR11	2.71	

	ADC1	5	

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

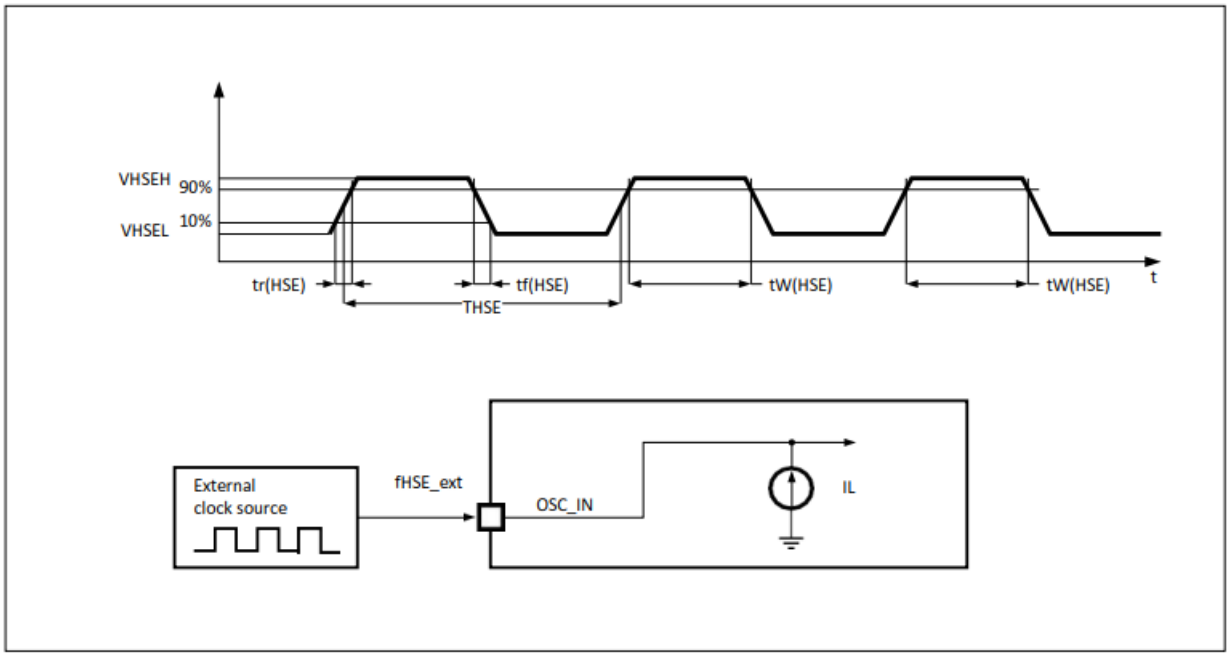
The characteristics given in the table below result from tests performed using a high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 11*.

Table 22 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 15 High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

The characteristics given in the table below result from tests performed using a low-speed external

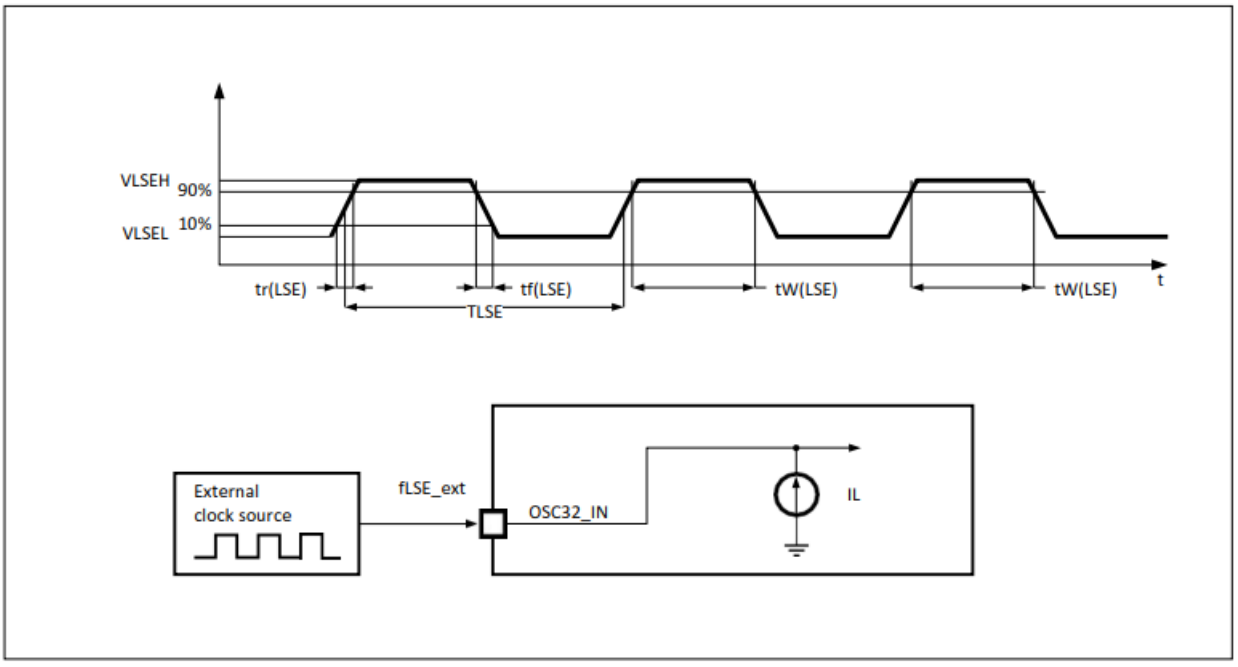
clock source, and under ambient temperature and supply voltage conditions summarized in *Table 11*.

Table 23 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	VDD	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	0.3VDD	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 16 Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details

on the resonator characteristics (frequency, package, accuracy).

Table 24 HSE 4-25 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HSE)}$ (3)	Startup time	V_{DD} is stabilized	-	2	-	ms

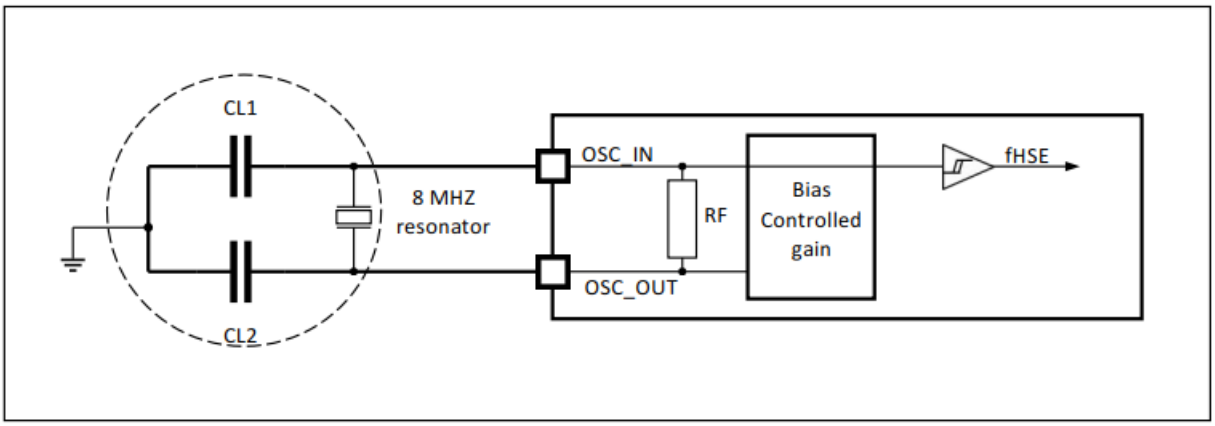
(1) Resonator characteristics given by the crystal/ceramic resonator manufacturer.

(2) Guaranteed by characterization results, not tested in production.

(3) $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 17 Typical application with an 8 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 25 LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LSE)}$	Startup time	V_{DD} is stabilized	-	150	-	ms

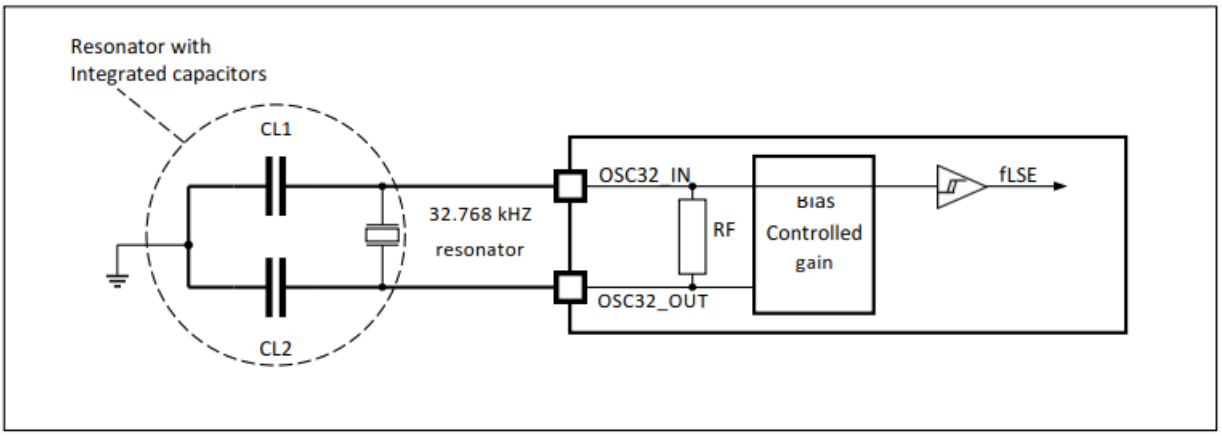
(1) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range

selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 18 Typical application with a 32.768 KHz crystal



5.3.7 Internal clock source characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*.

High-speed internal (HSI) RC oscillator

Table 26 HSI oscillator characteristics(1)

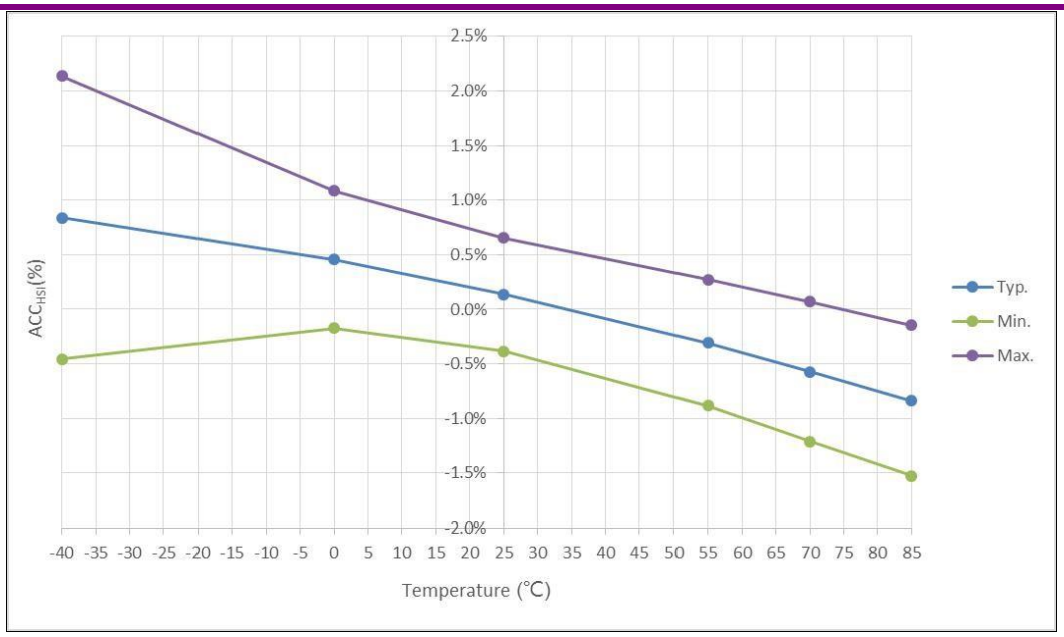
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CTRL register	-	-	1(2)	%
		T_A = -40 ~ 85 °C	-2.5	-	2	
		T_A = 0 ~ 70 °C	-1.5	-	1.5	
		T_A = 25 °C	-1	-	1	
$t_{SU(HSI)}$(3)	HSI oscillator startup time	-	-	-	10	μs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-	240	275	μA

(1) V_{DD} = 3.3 V, T_A = -40~85 °C, unless otherwise specified.

(2) Guaranteed by design, not tested in production.

(3) Guaranteed by characterization results, not tested in production.

Figure 19 HSI oscillator frequency accuracy vs. Temperature



Low-speed internal (LSI) RC oscillator

Table 27 LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	-	30	40	60	kHz

(1) V_{DD} = 3.3 V, T_A = -40 to 105 °C, unless otherwise specified.

(2) Guaranteed by characterization results, not tested in production.

5.3.8 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the HSI RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*.

Table 28 Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	3.3	μs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	280	μs
	Wakeup from Stop mode (regulator in low-power mode)	320	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode（EOPB0 = 1）	70	ms
	Wakeup from Standby mode（EOPB0 = 0）	270	

(1) wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.9 PLL characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*.

Table 29 PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	180	MHz
t_{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by characterization results, not tested in production.

(2) Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.10 Memory characteristics

The characteristics in *Table 30* are given at T_A = 25 °C and V_{DD} = 3.3 V.

Table 30 Internal Flash memory characteristics

Symbol	Parameter	Conditions	Typ					Unit
			f_{HCLK}					
			180	144	72	48	8	MHz
T_{PROG}	Programming time	-	50					μs
t_{ERASE}	Page (2 KB) erase time	-	50					ms
t_{ME}	Mass erase time	V8410N/C	1.4（block 1 or 2）					s
		V8411N	1.4（block 1 or 2）					
			15 （block 3）					
I_{DD}	Supply current	Programming mode	32	27	17	13	4.3	mA
		Erase mode	53	45	27	22	12	

Table 31 Internal Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit

NEND	Endurance	T_A = -40 ~ 85 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 85 °C	20	-	-	years

(1)Guaranteed by design, not tested in production.

5.3.11 XMC characteristics

Asynchronous waveforms and timings

Figure 20 through *Figure 21* represent asynchronous waveforms and *Table 32* through *Table 33* provide the corresponding timings. The results shown in these tables are obtained with the following XMC configuration:

AddressSetupTime = 0

AddressHoldTime = 1

DataSetupTime = 1

Figure 20 Asynchronous multiplexed PSRAM/NOR read waveforms

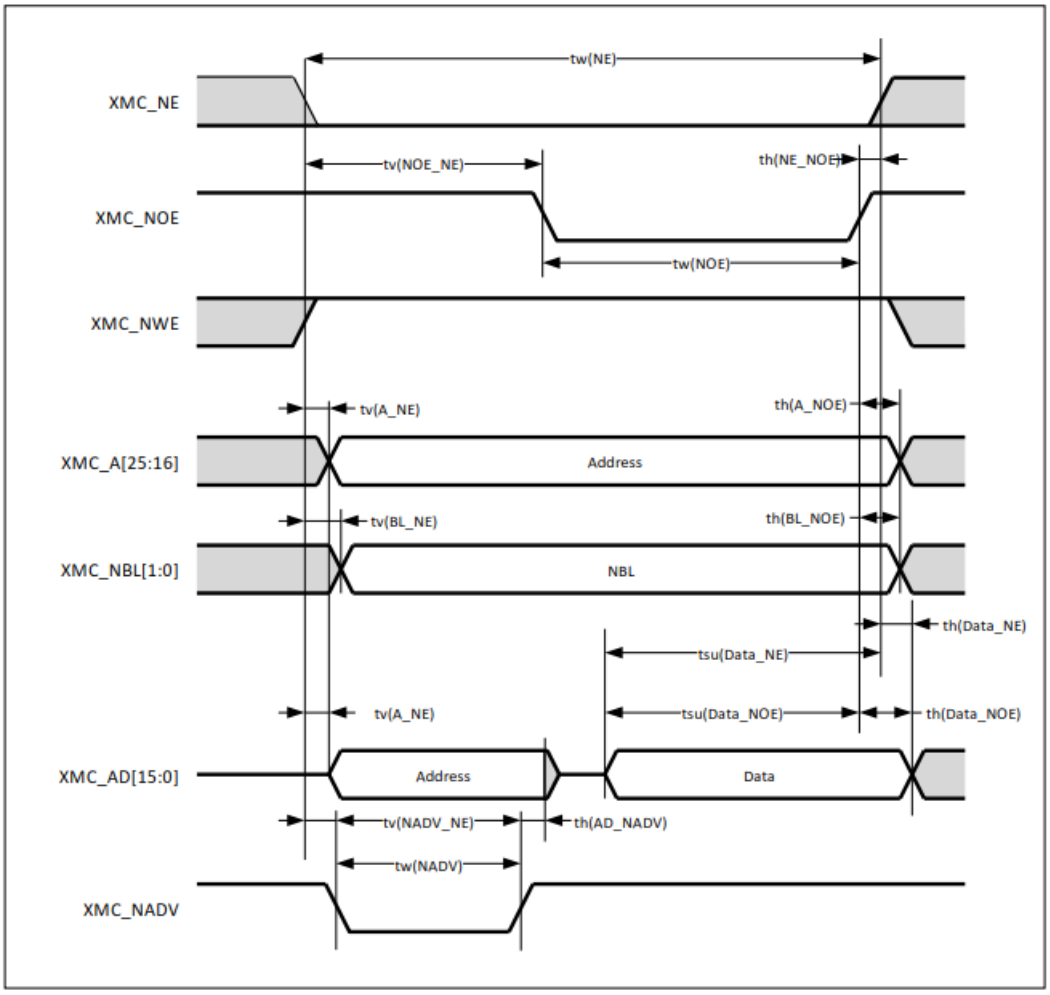


Table 32 Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$7t_{HCLK}$ - 2	$7t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	XMC_NEx low to XMC_NOE low	$3t_{HCLK}$ - 0.5	$3t_{HCLK}$ + 1.5	ns

$t_{w(NOE)}$	XMC_NOE low time	$4t_{HCLK}$ - 1	$4t_{HCLK}$ + 2	ns
$t_{h(NE\_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1	-	ns
$t_{v(A\_NE)}$	XMC_NEx low to XMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	XMC_NEx low to XMC_NADV low	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	XMC_AD (address) valid hold time after XMC_NADV high	t_{HCLK} + 3	-	ns
$t_{h(A\_NOE)}$	Address hold time after XMC_NOE high	t_{HCLK} + 3	-	ns
$t_{h(BL\_NOE)}$	XMC_BL hold time after XMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	XMC_NEx low to XMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to XMC_NEx high setup time	$2t_{HCLK}$ + 24	-	ns
$t_{su(Data\_NOE)}$	Data to XMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NE)}$	Data hold time after XMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after XMC_NOE high	0	-	ns

(1) C_L = 15 pF

(2) Guaranteed by characterization results, not tested in production.

Figure 21 Asynchronous multiplexed PSRAM/NOR write waveforms

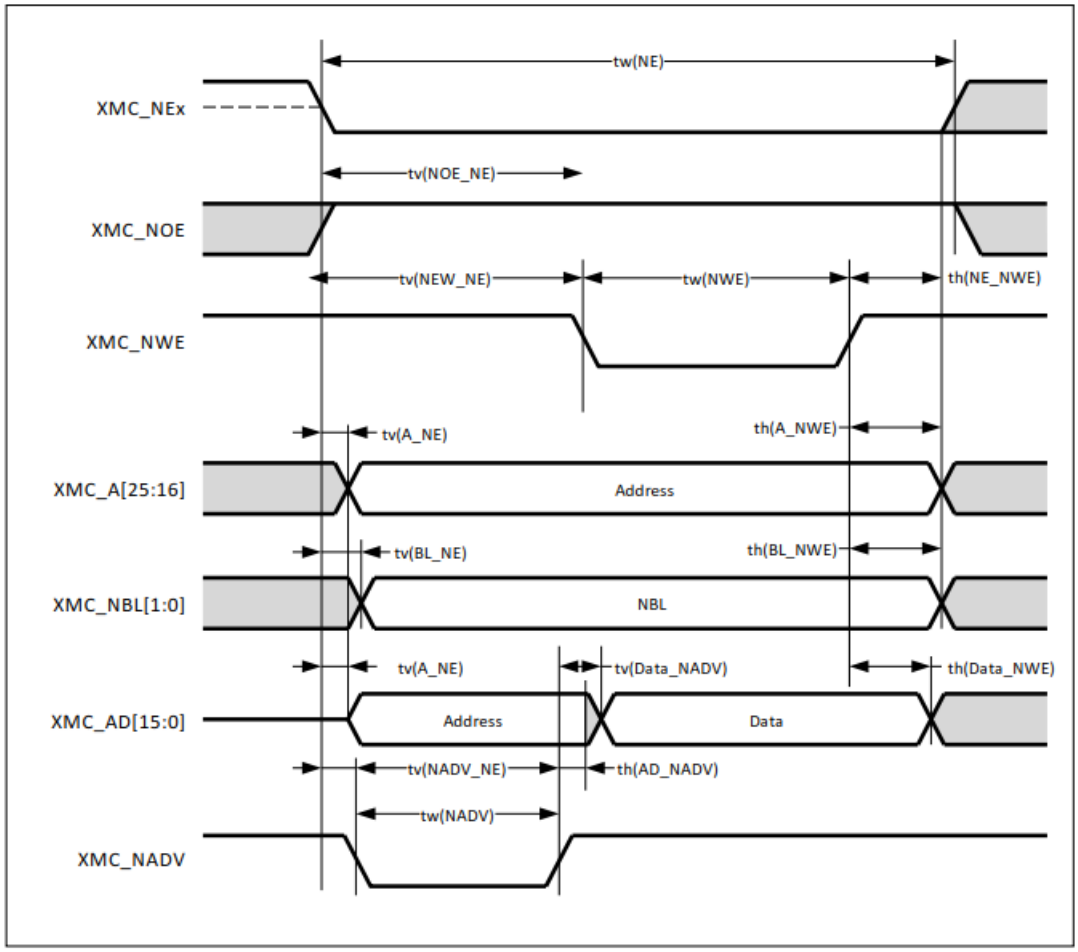


Table 33 Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$5t_{HCLK}$ - 1	$5t_{HCLK}$ + 2	ns
$t_{v(NWE\_NE)}$	XMC_NEx low to XMC_NWE low	$2t_{HCLK}$	$2t_{HCLK}$ + 1	ns
$t_{w(NWE)}$	XMC_NWE low time	$2t_{HCLK}$ - 1	$2t_{HCLK}$ + 2	ns
$t_{h(NE\_NWE)}$	XMC_NWE high to XMC_NE high hold time	t_{HCLK} - 1	-	ns
$t_{v(A\_NE)}$	XMC_NEx low to XMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	XMC_NEx low to XMC_NADV low	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1	t_{HCLK} + 1	ns
$t_{h(AD\_NADV)}$	XMC_AD (address) valid hold time after XMC_NADV high	t_{HCLK} - 3	-	ns
$t_{h(A\_NWE)}$	Address hold time after XMC_NWE high	$4t_{HCLK}$ + 2.5	-	ns
$t_{v(BL\_NE)}$	XMC_NEx low to XMC_BL valid	-	1.6	ns
$t_{h(BL\_NWE)}$	XMC_BL hold time after XMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{v(Data\_NADV)}$	XMC_NADV high to Data valid	-	t_{HCLK} + 1.5	ns
$t_{h(Data\_NWE)}$	Data hold time after XMC_NWE high	t_{HCLK} - 5	-	ns

(1) C_L = 15 pF

(2) Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 22 through *Figure 23* represent synchronous waveforms and *Table 34* through *Table 35* provide the corresponding timings. The results shown in these tables are obtained with the following XMC configuration:

BurstAccessMode = XMC_BurstAccessMode_Enable;

MemoryType = XMC_MemoryType_CRAM;

WriteBurst = XMC_WriteBurst_Enable;

CLKPrescale = 1; (Note: CLKPrescale is CLKPSC bit in XMC_BK1TMGx register. Refer to the V84XXX reference manual.)

DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM (Note: DataLatency is DATLAT bit in XMC_BK1TMGx register. Refer to the V84XXX reference manual.)

Figure 22 Synchronous multiplexed PSRAM/NOR read timings

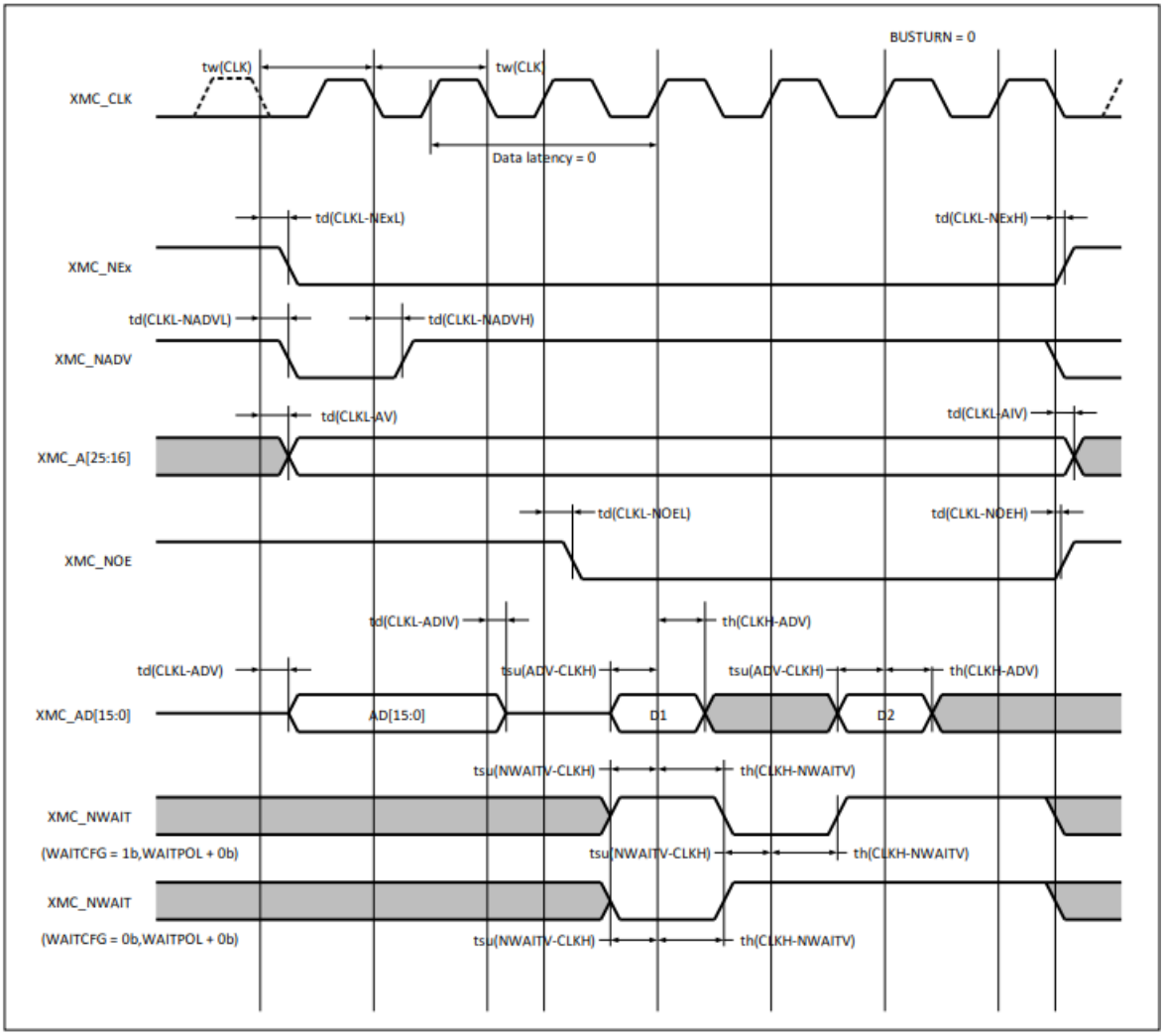


Table 34 Synchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NexL)}$	XMC_CLK low to XMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKH-NexH)}$	XMC_CLK low to XMC_NEx high (x = 0...2)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKH-AIV)}$	XMC_CLK low to XMC_Ax invalid (x = 16...25)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NOEL)}$	XMC_CLK low to XMC_NOE low		t_{HCLK} + 1	ns
$t_{d(CLKH-NOEH)}$	XMC_CLK low to XMC_NOE high	t_{HCLK} + 0.5	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	XMC_A/D[15:0] valid data before XMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	XMC_A/D[15:0] valid data after XMC_CLK high	t_{HCLK} - 10	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	8	-	ns

$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	6	-	ns

(1) C_L = 15 pF

(2) Guaranteed by characterization results, not tested in production.

Figure 23 Synchronous multiplexed PSRAM write timings

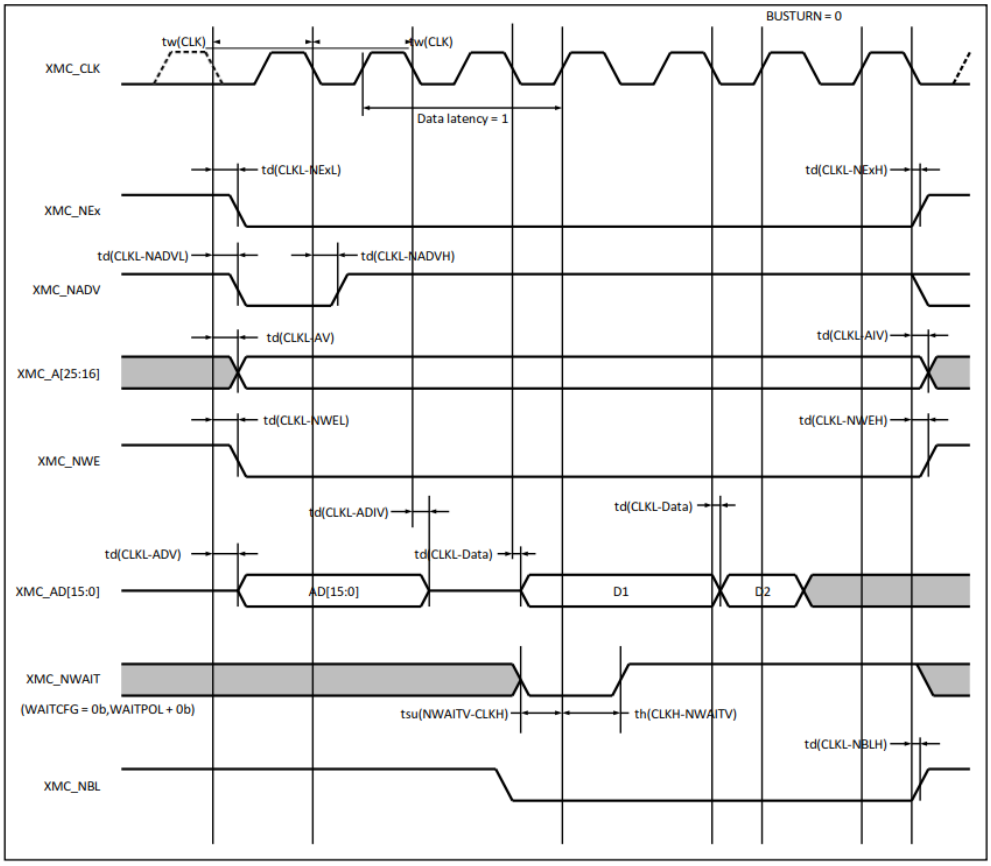


Table 35 Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NexL)}$	XMC_CLK low to XMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKH-NexH)}$	XMC_CLK low to XMC_NEx high (x = 0...2)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKH-AIV)}$	XMC_CLK low to XMC_Ax invalid (x = 16...25)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKH-NWEH)}$	XMC_CLK low to XMC_NWE high	t_{HCLK} + 1	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	XMC_A/D[15:0] valid after XMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	XMC_CLK low to XMC_NBL high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid before XMC_CLK high	2	-	ns

$t_{d(CLKL-NBLH)}$	XMC_NWAIT valid after XMC_CLK high	1	-	ns

(1) C_L = 15 pF

(2) Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 24 through *Figure 27* represent synchronous waveforms and *Table 36* provides the corresponding timings. The results shown in this table are obtained with the following XMC configuration:

COM.XMC_SetupTime = 0x01; (Note: STP in XMC_BKxTMGMEM, x = 2…4)

COM.XMC_WaitSetupTime = 0x03; (Note: OP in XMC_BKxTMGMEM, x = 2…4)

COM.XMC_HoldSetupTime = 0x02; (Note: HLD in XMC_BKxTMGMEM, x = 2…4)

COM.XMC_HiZSetupTime = 0x01; (Note: WRSTP in XMC_BKxTMGMEM, x = 2…4)

ATT.XMC_SetupTime = 0x01; (Note: STP in XMC_BKxTMGATT, x = 2…4)

ATT.XMC_WaitSetupTime = 0x03; (Note: OP in XMC_BKxTMGATT, x = 2…4)

ATT.XMC_HoldSetupTime = 0x02; (Note: HLD in XMC_BKxTMGATT, x = 2…4)

ATT.XMC_HiZSetupTime = 0x01; (Note: WRSTP in XMC_BKxTMGATT, x = 2…4)

Bank = XMC_Bank_NAND;

MemoryDataWidth = XMC_MemoryDataWidth_16b; (Note: Memory data width = 16 bits)

ECC = XMC_ECC_Enable; (Note: enable ECC calculation)

ECCPageSize = XMC_ECCPageSize_512Bytes; (Note: ECC page size = 512 Bytes)

DLYCRSetupTime = 0; (Note: DLYCR in XMC_BKxCTRL)

DLYARSetupTime = 0; (Note: DLYAR in XMC_BKxCTRL)

Figure 24 NAND controller waveforms for read access

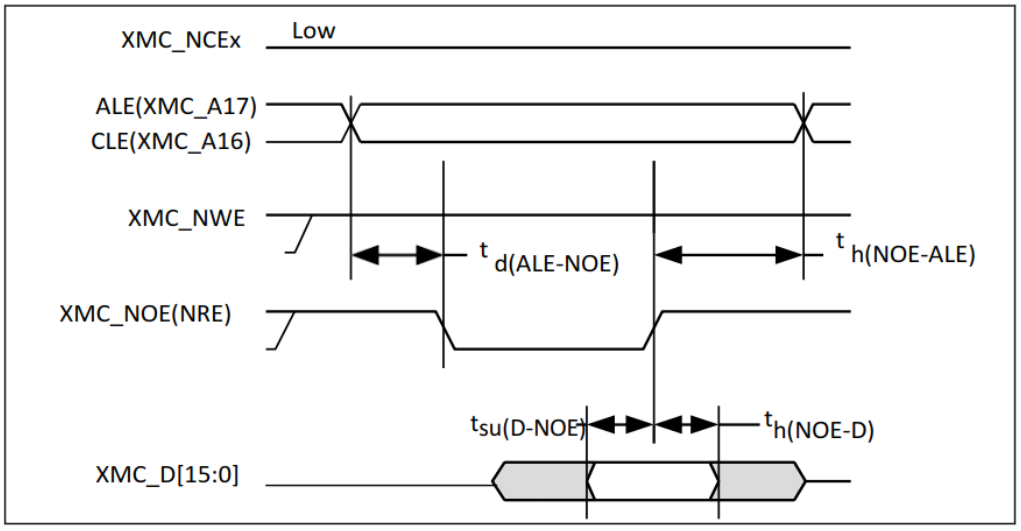


Figure 25 NAND controller waveforms for write access

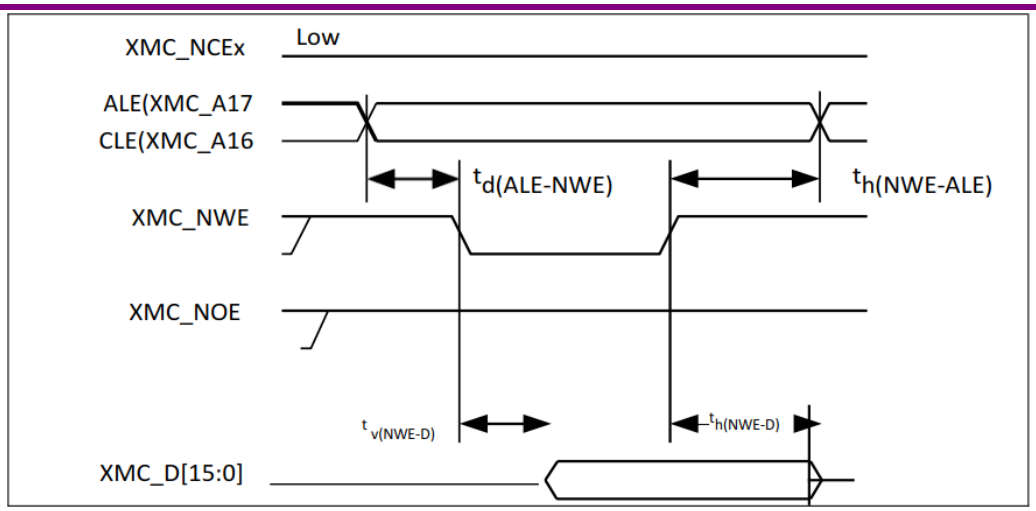


Figure 26 NAND controller waveforms for common memory read access

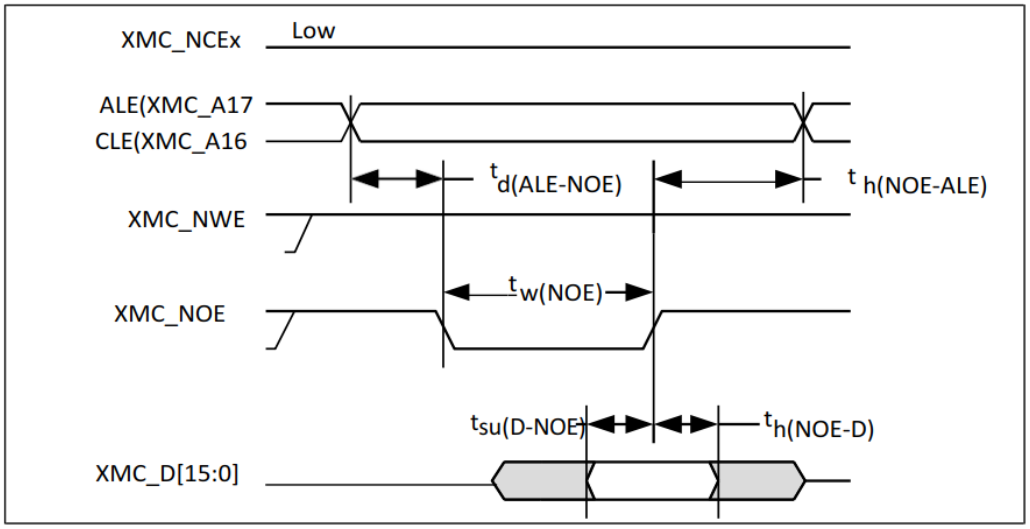


Figure 27 NAND controller waveforms for common memory write access

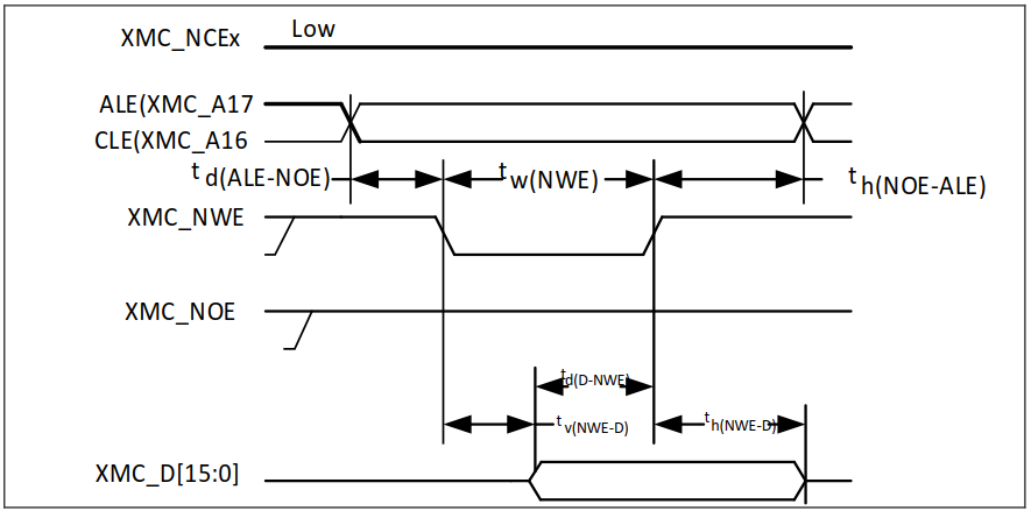


Table 36 Switching characteristics for NAND Flash read and write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$(2)	XMC_D[15:0] valid before XMC_NWE high	$6T_{HCLK}$ + 12	-	ns
$t_{w(NOE)}$(2)	XMC_NWE low width	$4T_{HCLK}$ - 1.5	$4T_{HCLK}$ + 1.5	ns
$t_{su(D-NOE)}$(2)	XMC_D[15:0] valid data before XMC_NOE high	25	-	ns

$t_{h(NOE-D)}$ (2)	XMC_D[15:0] valid data after XMC_NOE high	14	-	ns
$t_{w(NWE)}$ (2)	XMC_NWE low width	$4T_{HCLK}$ - 1	$4T_{HCLK}$ + 2.5	ns
$t_{v(NWE-D)}$ (2)	XMC_NWE low to XMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$ (2)	XMC_NWE high to XMC_D[15:0] invalid	$10T_{HCLK}$ + 4	-	ns
$t_{d(ALE-NWE)}$ (3)	XMC_ALE valid before XMC_NWE low	-	$3T_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$ (3)	XMC_NWE high to XMC_ALE invalid	$3T_{HCLK}$ + 4.5	-	ns
$t_{d(ALE-NOE)}$ (3)	XMC_ALE valid before XMC_NOE low	-	$3T_{HCLK}$ + 2	ns
$t_{h(NOE-ALE)}$ (3)	XMC_NWE high to XMC_ALE invalid	$3T_{HCLK}$ + 4.5	-	ns

(1) C_L = 15 pF

(2) Guaranteed by characterization results, not tested in production.

(3) Guaranteed by design, not tested in production.

5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in *Table 11*. All I/Os are CMOS and TTL compliant.

Table 37 I/O static characteristics

Symb	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	-	–0.3	-	0.28 * V_{DD} + 0.1	V
V_{IH}	TC I/O input high level voltage	-	0.31 * V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FTa I/O input high level voltage	Analog mode				
	FT I/O input high level voltage	-		-	5.5	
	FTa I/O input high level voltage	Input floating, input pull-up, or input pull-down mode				
V_{hys}	TC I/O Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
	FT and FTa I/O Schmitt trigger voltage hysteresis(1)		5% V_{DD}	-	-	-
I_{lkg}	Input leakage current(2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC I/Os	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5V$ FT and FTa I/O	-	-	±1	

R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	60	75	110	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = V_{DD}$	60	75	120	kΩ
C_{IO}	I/O pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

(2) Leakage could be higher than max if negative current is injected on adjacent pins.

(3) The pull-down resistor of BOOT0 exists permanently.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 9*).
- The sum of the currents sunk by all I/Os on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 9*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 11*. All I/Os are CMOS and TTL compliant.

Table 38 Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Maximum sourcing/sinking stregth					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 45 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Large sourcing/sinking stregth					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 20 mA	-	1.3	V

V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Normal sourcing/sinking stregth					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 10 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Unless otherwise specified, the parameters given below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in *Table 11*.

Table 39 Input AC characteristics

Symbol	Parameter	Min	Max	Unit
t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	10	-	ns

5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

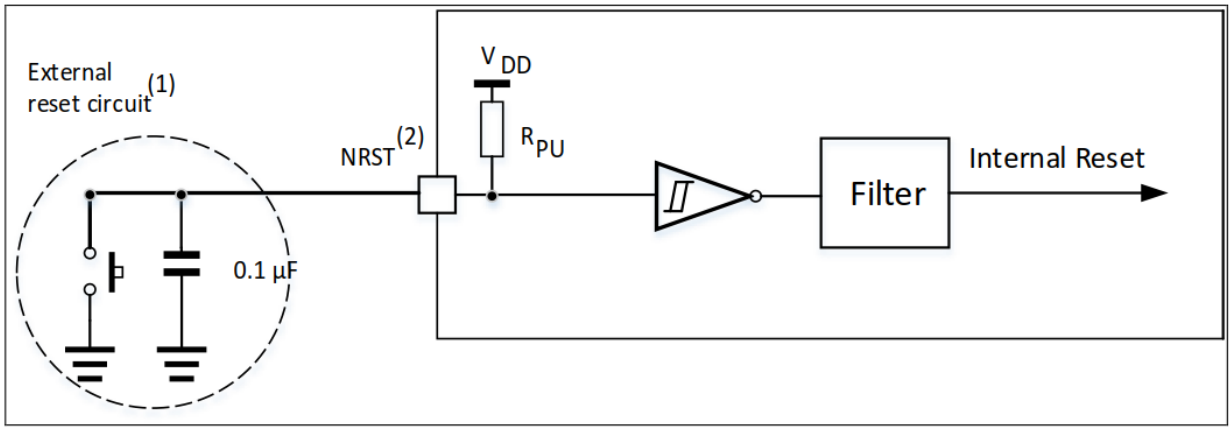
Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 11*.

Table 40 NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	500	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	24	33.3	μs
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	66.7	46	-	μs

(1) Guaranteed by design.

Figure 28 Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.

(2) The user must ensure that the level on the NRST pin can go below the VIL (NRST) max level specified in *Table 40*. Otherwise the reset will not be taken into account by the device.

5.3.14 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to *5.3.12 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 41 TMRx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution tim	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 180MHZ	5.6	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}/2$	MHz
			0	50	MHz

(1) TMRx is used as a general term to refer to the TMR1 to TMR14.

5.3.15 Communications interfaces

I²C interface characteristics

The V84XXX I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL mapped to are not ”true” open-drain.

When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in the table below. Refer also to *5.3.12 I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 42 I²C characteristics

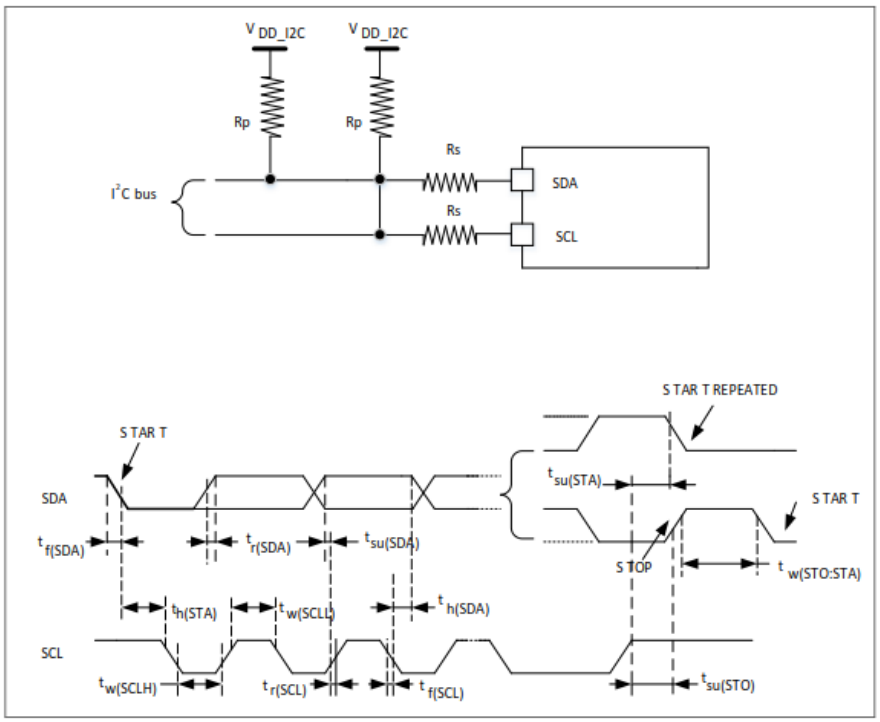
Symbol	Parameter	Standard mode I^2C (1)(2)		Fast mode I^2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

(1) Guaranteed by design, not tested in production.

(2) f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve the fast mode I^2C frequencies.

(3) The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.

Figure 29 I^2C bus AC waveforms and measurement circuit(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 43 SCL frequency (fPCLK1 = 36 MHz, VDD = 3.3 V)(1)(2)

f_{SCL}(kHz)	I2C_CLKCTRL value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

(1) R_P = External pull-up resistance, f_{SCL} = I^2C speed.

(2) For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI-I^2S characteristics

Unless otherwise specified, the parameters given in *Table 44* for SPI or in *Table 45* for I^2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 11*.

Refer to *5.3.12 I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 44 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency(2)(3)	Master mode	-	36	MHz
		Slave mode	-	$f_{PCLK}/2$	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 90 MHz, prescaler = 4	22	32	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{h(SI)}$ (1)		Slave mode	4	-	

$t_{a(SO)}$(1)(4)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(5)	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

(1) Guaranteed by characterization results, not tested in production.

(2) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

(3) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 30 SPI timing diagram - slave mode and CPHA = 0

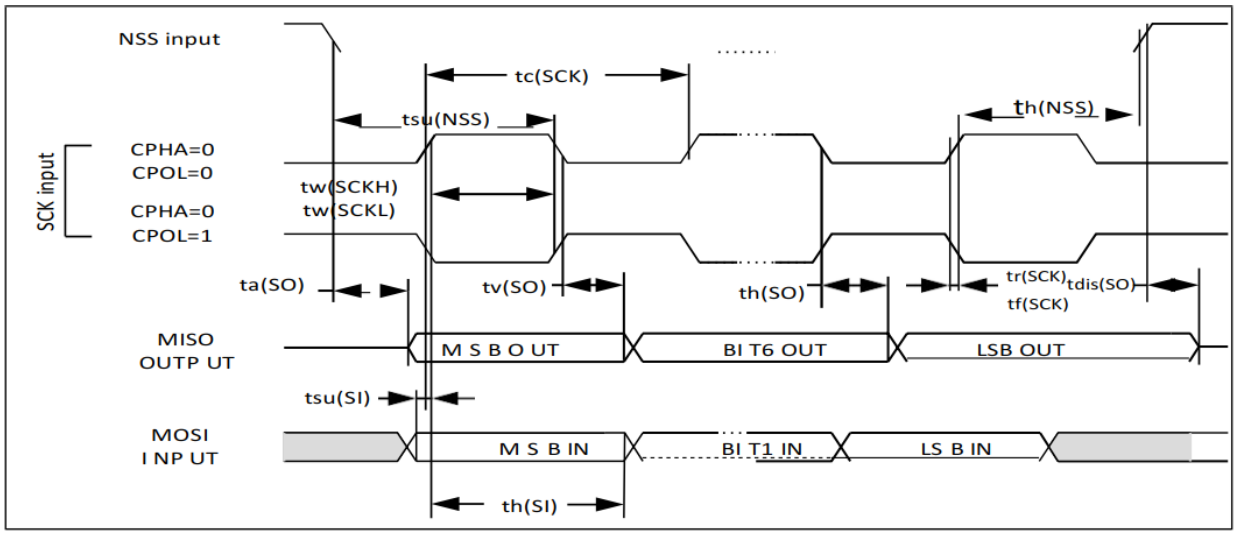
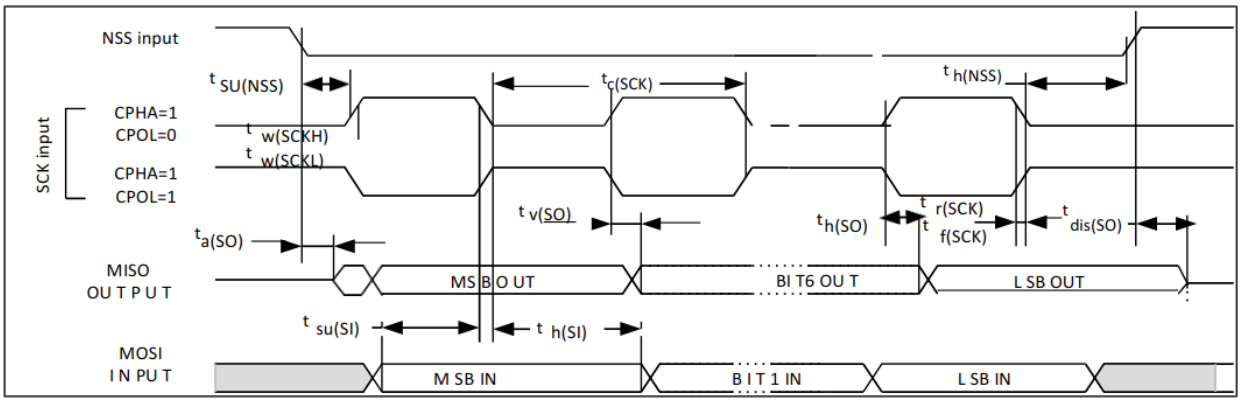
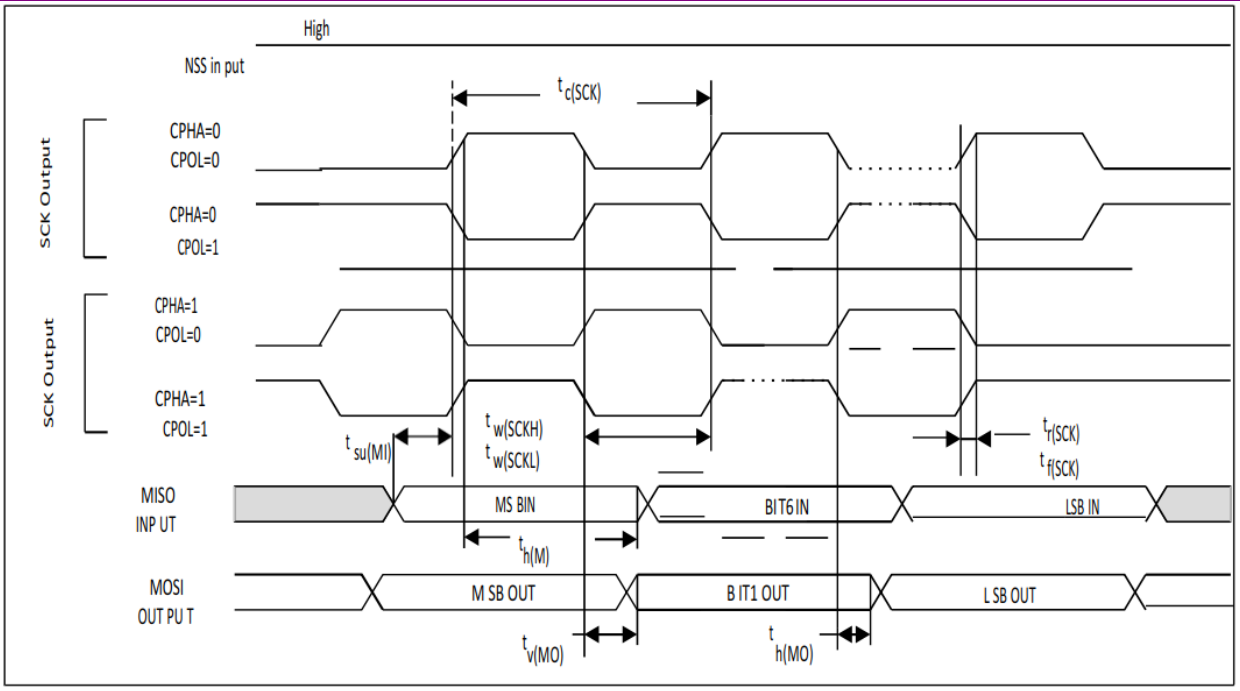


Figure 31 SPI timing diagram - slave mode and CPHA = 1(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 32 SPI timing diagram - master mode(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 45 I²S characteristics

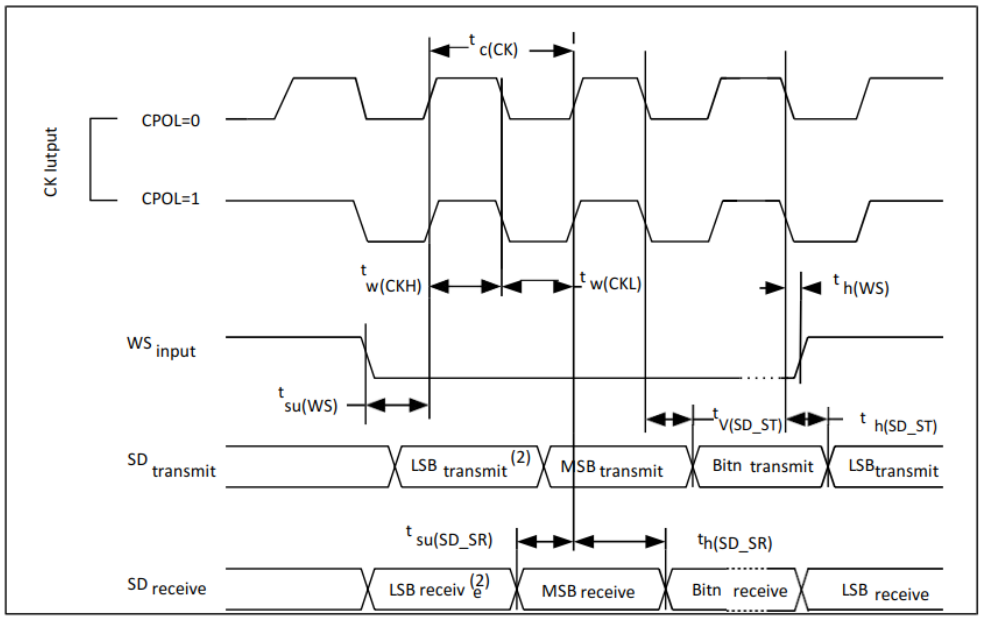
Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I2S clock frequency	Master mode (data: 16 bits, audio frequency = 48 kHz)	1.522	1.525	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I2S clock rise and fall time	Capacitive load: C = 50 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	2	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	4	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode	0	-	
$t_{w(CKH)}$ (1)	CK high and low time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz	312.5	-	
$t_{w(CKL)}$ (1)			345	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6.5	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	18	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	11	-	

$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	

(1) Guaranteed by design and/or characterization results.

(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

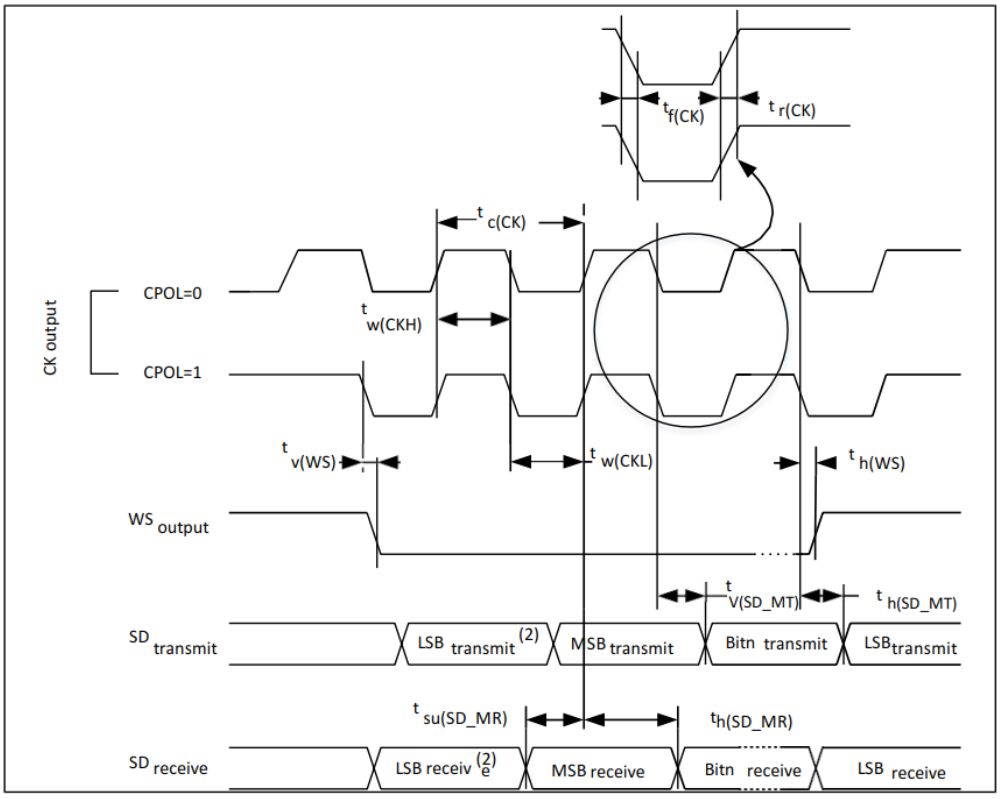
Figure 33 I²S slave timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 34 I²S master timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

Table 46 USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$ (1)	USB transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 47 USB DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	USB operating voltage	-	3.0(2)		3.6	V
	V_{DI}(3)	Differential input sensitivity	I (USB_DP, USB_DM)	0.2		-	V
	V_{CM}(3)	Differential common mode range	Includes VDI range	0.8		2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3		2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS} (4)	2.8		3.6	
R_{PU}		USB_DP internal pull-up	$V_{IN} = V_{SS}$	0.97	1.24	1.58	kΩ

(1) All the voltages are measured from the local groundpotential.

(2) The V84XXX USB functionality is ensured down to 2.6 V but not the full USB electrical characteristics which are degraded in the 2.6 to 3.0 V V_{DD} voltage range.

(3) Guaranteed by characterization results, not tested in production.

(4) RL is the load connected on the USB drivers.

Figure 35 USB timings: definition of data signal rise and fall time

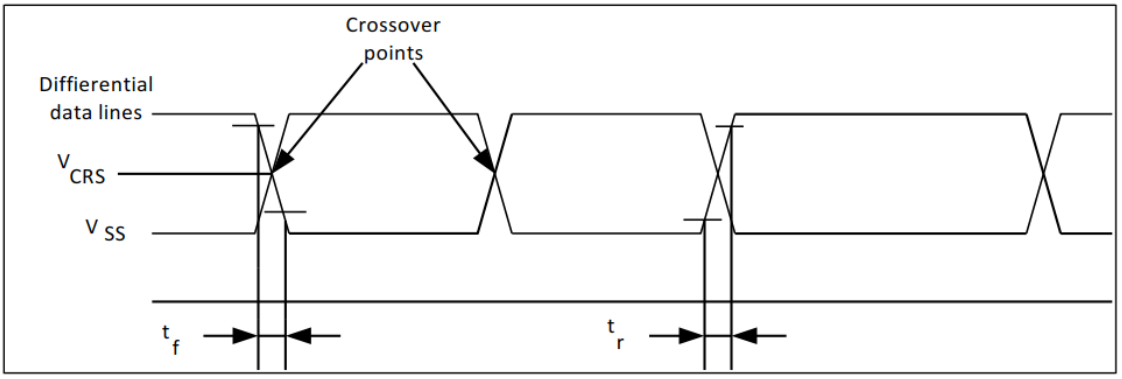


Table 48 USB full-speed electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time (2)	$C_L \leq 50$ pF	4	20	ns
t_f	Fall Time (2)	$C_L \leq 50$ pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.

(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to *5.3.12 I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 11*.

Note: It is recommended to perform a calibration after each power-up.

Table 49 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.6	-	3.6	V
V_{REF+}	Positive reference voltage(3)	-	2.0	-	V_{DDA}	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	380(1)	435	μA
I_{VREF}	Current on the VREF+ input pin(3)	-	-	200(1)	230	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(2)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground))	-	VREF+	V
R_{AIN}(2)	External input impedance	-	See *Table* 50 and *Table* 51 for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	10	-	pF

t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.61			µs
		-	185			1/f_{ADC}
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(3)	1/f_{ADC}
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	µs
		-	-	-	2(3)	1/f_{ADC}
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	µs
		-	1.5	-	239.5	1/f_{ADC}
t_{STAB}(2)	Power-up time	-	42			1/f_{ADC}
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	µs
		-	14 to 252 (tS for sampling + 12.5 for successive approximation)			1/f_{ADC}

(1) Guaranteed by characterization results, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) For external triggers, a delay of 1/f_{PCLK2} must be added to the latency specified in *Table 49*.

Table 50 and *Table 51* are used to determine the maximum external impedance allowed for an error below 1/4 of LSB.

Table 50 R_{AIN} max for f_{ADC} = 14 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.25
7.5	0.54	1.3
13.5	0.96	2.5
28.5	2.04	5.0
41.5	2.96	8.0
55.5	3.96	10.5
71.5	5.11	13.5
239.5	17.11	40

(1) Guaranteed by design.

Table 51 R_{AIN} max for f_{ADC} = 28 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	0.6
13.5	0.48	1.2
28.5	1.02	2.5

41.5	1.48	4.0
55.5	1.98	5.2
71.5	2.55	7.0
239.5	8.55	20

(1) Guaranteed by design.

Table 52 ADC accuracy (V_{DDA} = 3.0 to 3.6 V, V_{REF+} = V_{DDA}, T_A = 25 °C)(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz,	±1.5	±3	
EO	Offset error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ,	+0.5	±1.5	
EG	Gain error	V_{DDA} = 3.0 to 3.6 V, TA = 25 °C	+1	+2/-0.5	LSB
ED	Differential linearity error	Measurements made after ADC calibration	±0.6	±0.9	
EL	Integral linearity error	V_{REF+} = V_{DDA}	±0.8	±1.5	

(1) ADC DC accuracy values are measured after internal calibration.

(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.

(3) Guaranteed by characterization results, not tested in production.

Table 53 ADC accuracy (V_{DDA} = 2.6 to 3.6 V, T_A = -40 to +85 °C)(1)(2)

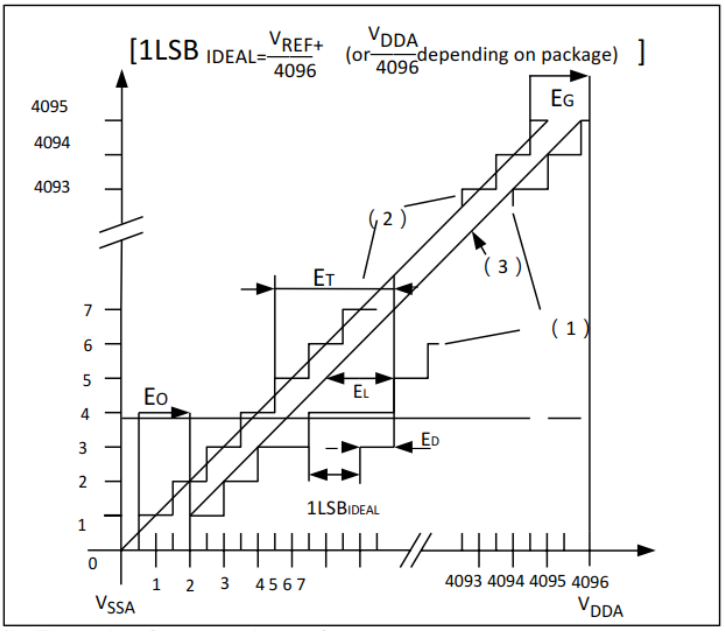
Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.6 to 3.6 V Measurements made after ADC calibration	±2	±4	
EO	Offset error		+0.5	±2	
EG	Gain error		+1	+3/-1	LSB
ED	Differential linearity error		±0.6	±1	
EL	Integral linearity error		±1	±1.8	

(1) ADC DC accuracy values are measured after internal calibration.

(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.

(3) Guaranteed by characterization results, not tested in production.

Figure 36 ADC accuracy characteristics



(1) Example of an actual transfer curve.

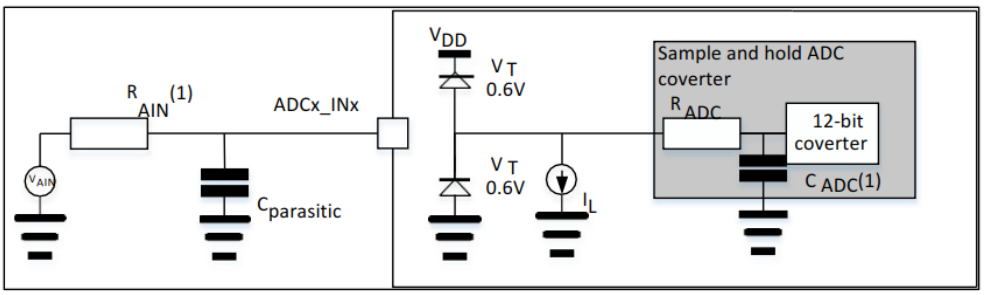
(2) Ideal transfer curve.

(3) End point correlation line.

(4) ET = Maximum deviation between the actual and the ideal transfer curves. EO = Deviation between the first actual transition and the first ideal one. EG = Deviation between the last ideal transition and the last actual one. ED = Maximum deviation between actual steps and the ideal one.

EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 37 Typical connection diagram using the ADC



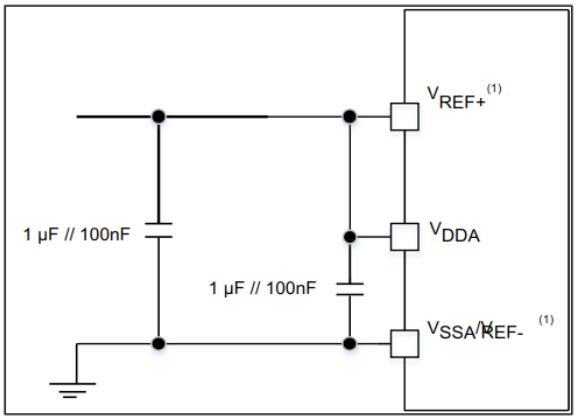
(1) Refer to *Table 49* for the values of R_{AIN} and C_{ADC}.

(2) Cparasitic represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high Cparasitic value will downgrade conversion accuracy. To remedy this, fADC should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 38*. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 38 Power supply and reference decoupling (V_{REF+} not connected to VDDA)



5.3.17 Temperature sensor characteristics

Table 54 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	VSENSE linearity with temperature	-	±1	±2	ºC
Avg_Slope(1) (2)	Average slope	-4.14	-4.26	-4.37	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	1.17	1.27	1.37	V
t_{START}(3)	Startup time	-	-	100	µs
T_{S_temp}(3)(4)	ADC sampling time when reading the temperature	-	8.6	17.1	µs

(1) Guaranteed by characterization results, not tested in production.

(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

(3) Guaranteed by design, not tested in production.

(4) Shortest sampling time can be determined in the application by multiple iterations.

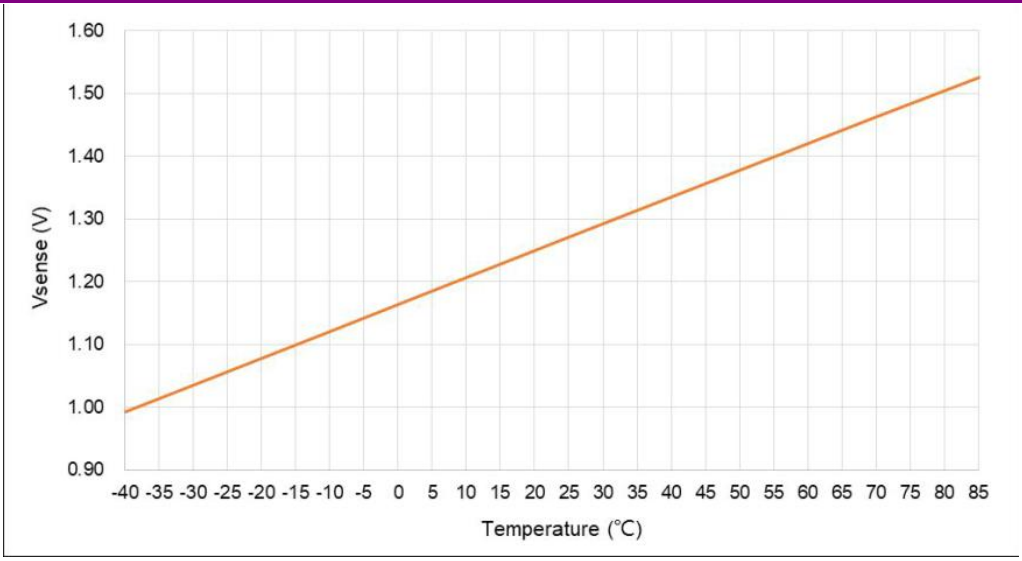
Obtain the temperature using the following formula:

Temperature (in °C) = {(V_{25} - V_{SENSE}) / Avg_Slope} + 25. Where,

V_{25} = V_{SENSE} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{SENSE} (given in mV/° C).

Figure 39 V_{SENSE} vs. temperature



5.4 ESD electricial character

Table 55 ESD electricial parameter

V_{ESD}	Human Body Model(HBM)	-4000	4000	V
	Charged Device Model(CDM)	-1000	1000	V

6 stroage

6.1 Hmidity sensitivity

Table 56 MSL summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

Note: The moisture sensitivity level of V84XXX is MSL3.

6.2 Storage conditions

Table 57 Bagged storage conditions

Packaging method	method Vacuum
Storage temperature	-55°C ~150°C

7 Reflow soldering process

All Wangao chips provided to customers are lead-free RoHS compliant products.

The reflow soldering process recommended in this article is a lead-free reflow soldering process, which is suitable for the pure lead-free process of lead-free solder paste. If customers need to use lead solder paste, please contact the smart chip FAE connect.

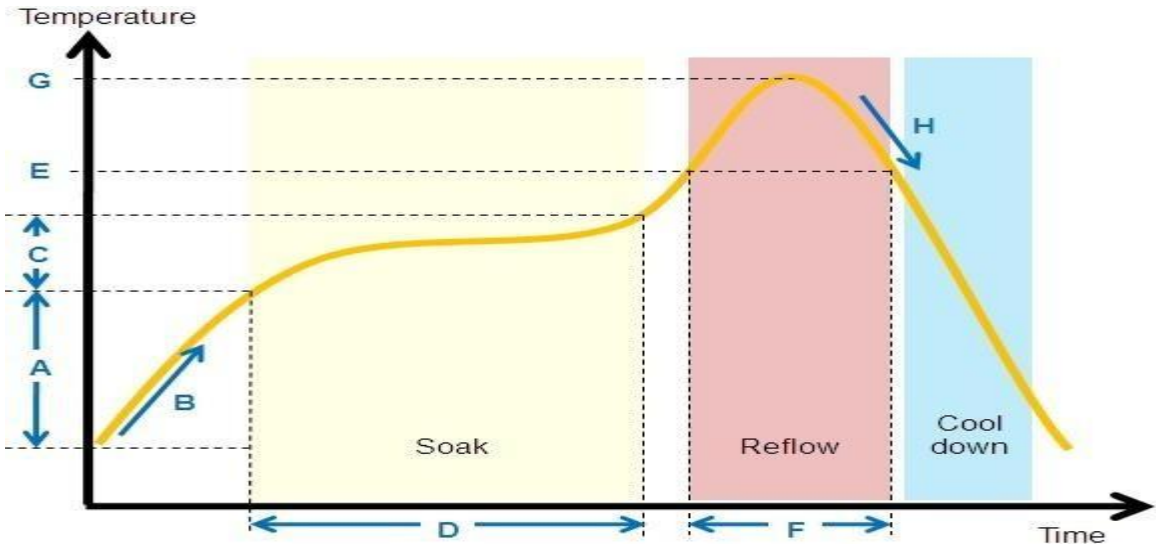
See Table 58 for lead-free reflow profile conditions. This table is for reference only.

Table 58 Reflow profile conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

The figure below shows a typical lead-free reflow mode.

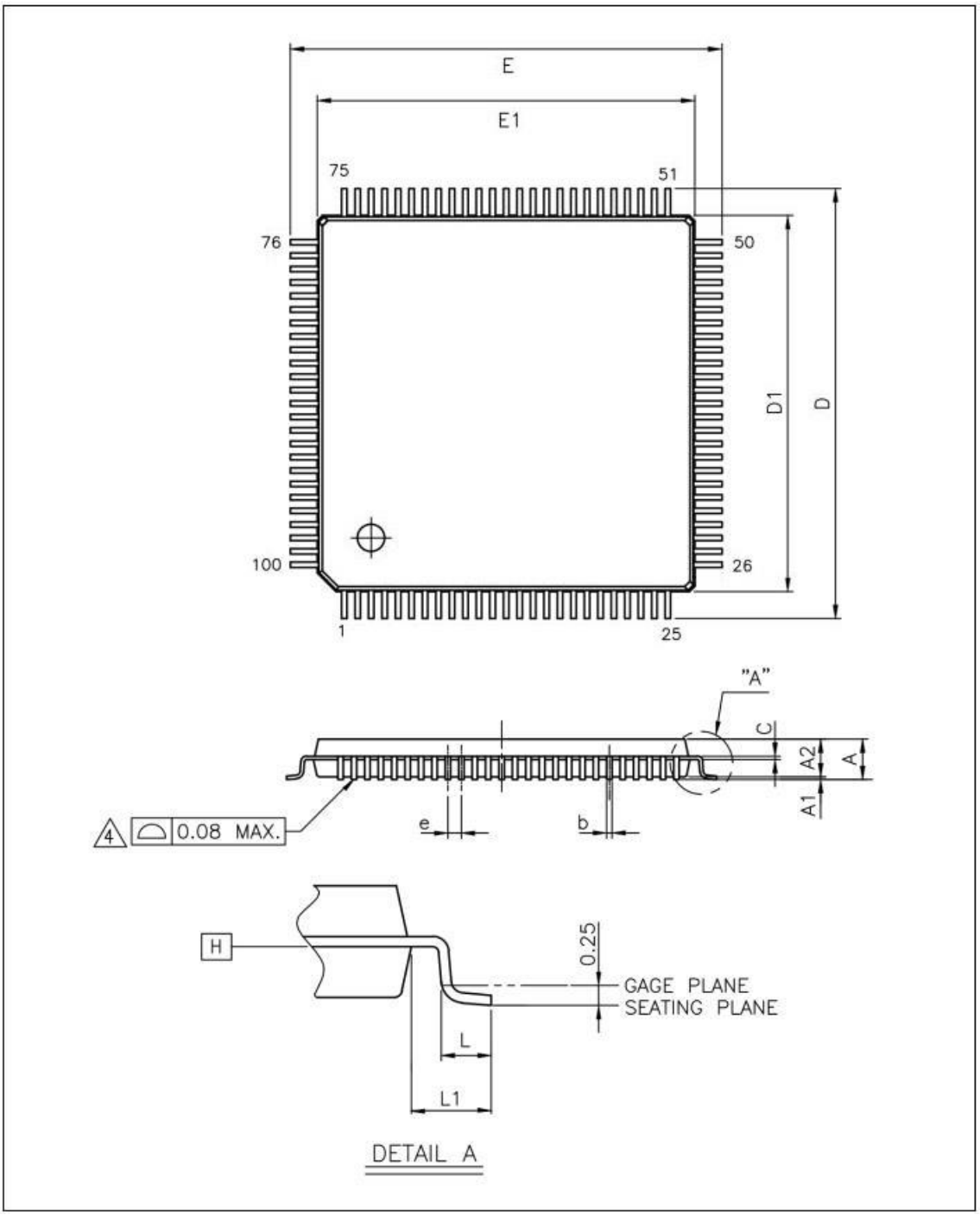
Figure 40 A typical lead-free reflow mode



8 Package information

8.1 LQFP100 package information

Figure 41 LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



(1) Drawing is not in scale.

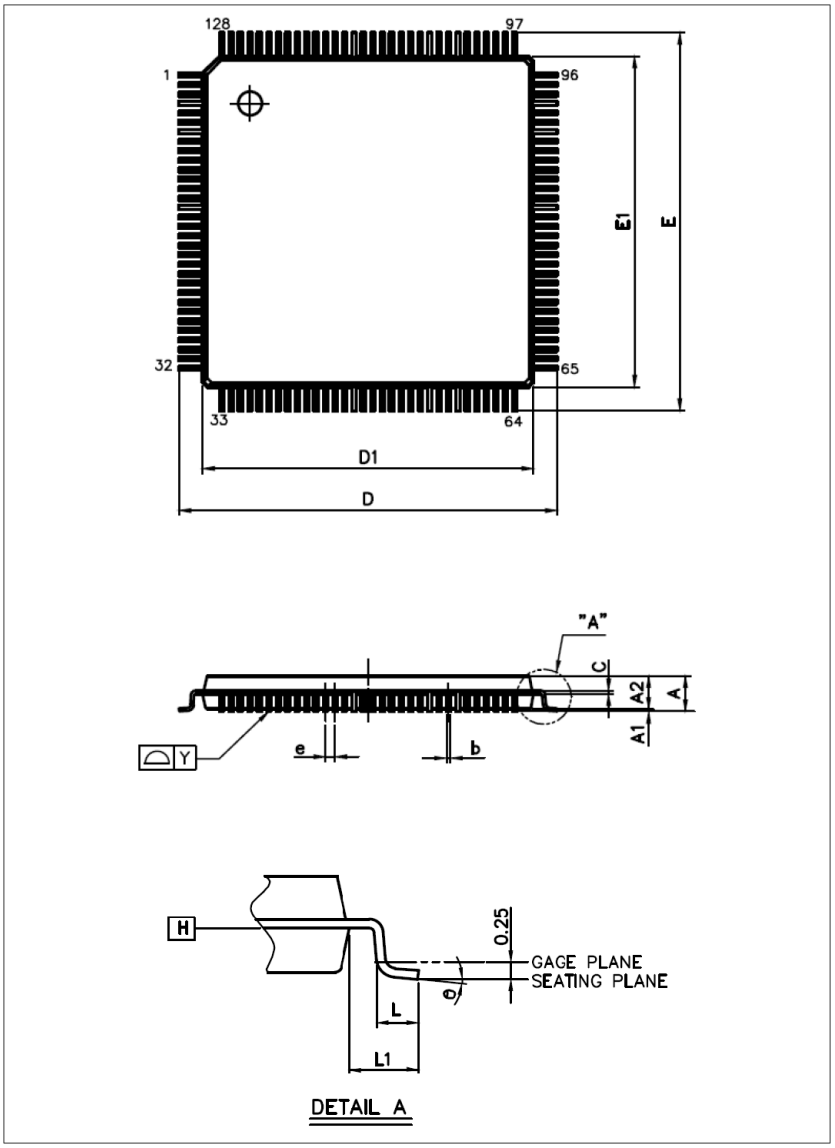
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063

A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.26	0.007	0.008	0.010
c	0.10	0.127	0.20	0.004	0.005	0.008
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
e	0.50 BSC.			0.020 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

8.2 LQFP128 package information

Figure 42 LQFP128 – 14 x 14 mm 128 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	-	0.23	0.005	-	0.009
c	0.09	-	0.20	0.004	-	0.008
D	16.00BSC			0.630BSC		
D1	14.00BSC			0.551BSC		
E	16.00BSC			0.630BSC		
E1	14.00BSC			0.551BSC		

e	0.40BSC			0.016BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
θ	0◦	3.5◦	7◦	0◦	3.5◦	7◦
Y	0.08			0.003		

8.3 QFN48 package information

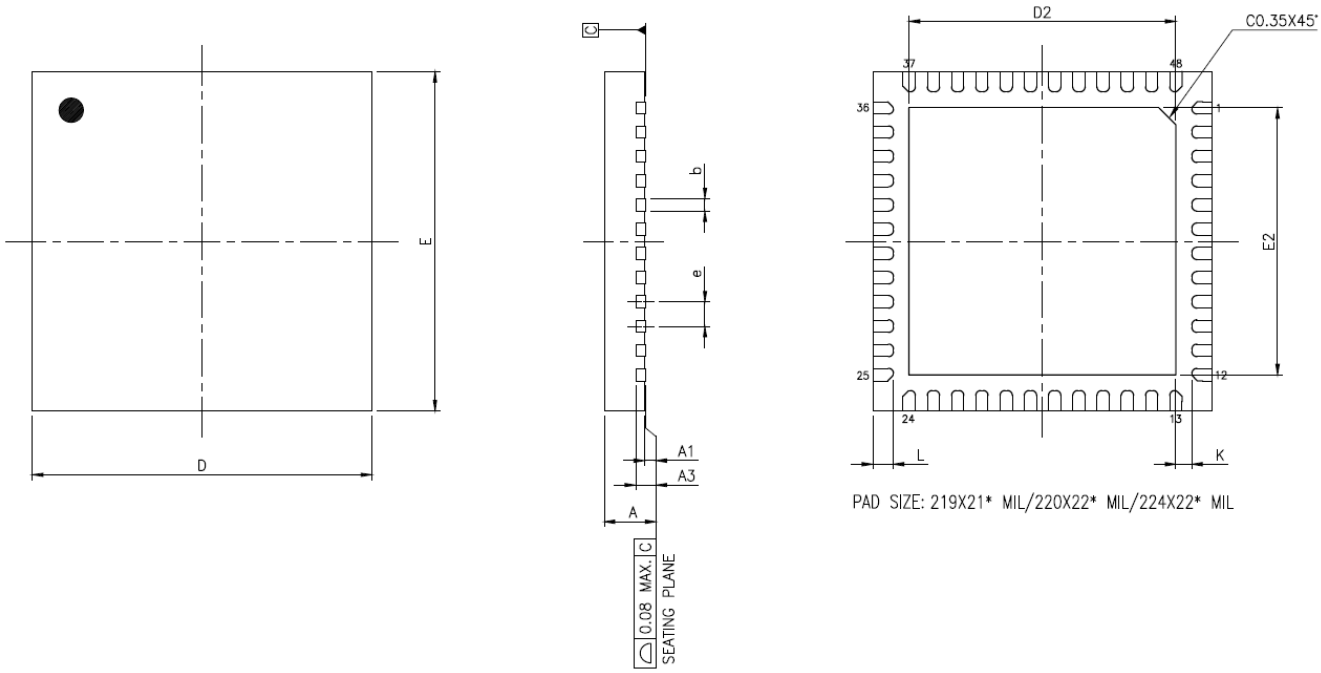


Figure 43 QFN48 – 7 x 7 mm 48 pin low-profile quad flat package outline

(1) Drawing is not in scale.

JEDEC	PACKAGE TYPE		
	MO-220		
PKG CODE	VQFN（Y748）		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		

PAD SIZE	D2			E2			L			K			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure	PPF	

													Tin		
224X22* MIL	5.25	5.30	5.35	5.25	5.30	5.35	0.35	0.40	0.45	0.20	-	-	V	X	N/A

8.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 11*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{jmax} = T_{amax} + (P_{dmax} \times \Theta_{JA})$

Where:

- T_{amax} is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_{dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins where:

$$P_{I/Omax} = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 59 Package thermal characteristics

symbol	Parameter	value	unit
Θ_{JA}	Thermal impedance from junction to environment	53.6	°C/W