V9260S Datasheet

Specifications are subject to change without notice.

Revision History

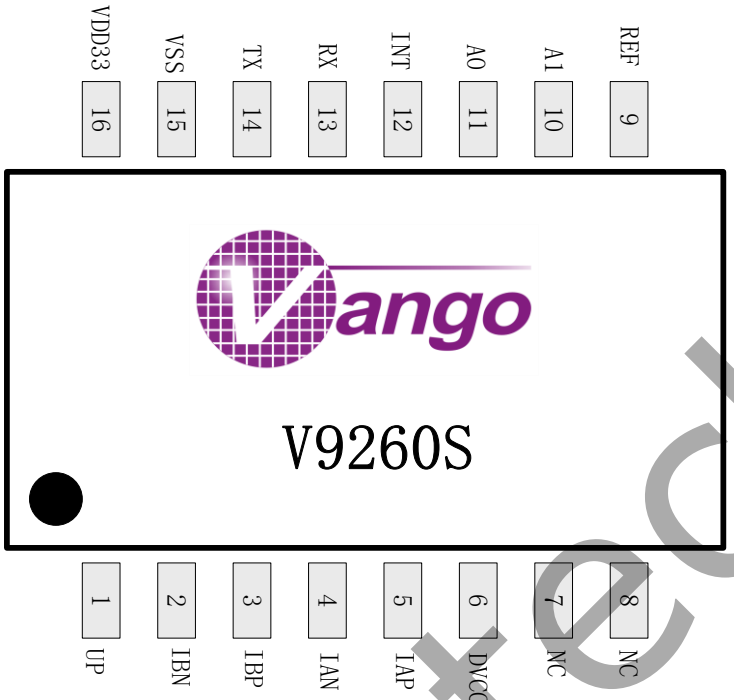
Date	Version	Description
2017.11.18	0.1	Initial release
2018.03.12	3.0	Modify reference voltage to 1.210V. In order to obtain the best metering performance and temperature performance during normal metering, Bandgap Circuit must be configured according to the calculated result. The calculation method, please refer to Bandgap Circuit chapter. Modify figure of Power, Clock and so on.
2018.03.27	3.1	Modify the formula of offset Calibration of RMS.
2018.05.31	3.2	Modify the formula of Phase Compensation.
2018.09.01	3.3	Modify the typical power consumption to 1.7mA, and the range is +-10%. Modify 3.3V power supply to 2.9~3.6V Modify the typical value of the power down threshold to 2.7V, range 2.5V~2.9V Modify the storage temperature to -55~150°C Add register AnaCtrl0 (0x182) and AnaCtrl1 (0x183).
2019.01.17	3.4	Remove the threshold for energy.
2019.11.29	3.5	Add chip mark description. Modify the maximum baud rate to 19200bps.
2020.08.10	3.7	Add PN Junction Temperature.
2021.04.15	3.8	Update IEC Standard

V9260S is a multifunction, ultralow power, single-phase power measurement IC with automatic baud rate adaption UART serial interface.

Features

- 3.3V power supply: 2.9V to 3.6V.
- Reference: 1.210V (typical drift 10ppm/°C).
- Power dissipation in full operation: 1.7mA (+-10%).
- Supporting two current channels for active energy metering and one current channel reactive energy metering simultaneously
- Highly metering accurate:
  - ✓ Supporting Supports the requirements of IEC 62053-21:2020/ IEC 62053-22:2020 and IEC 62053-23:2020;
  - ✓ Less than 0.1% error for active/reactive energy metering over a dynamic range of 5000:1;
- 3 independent oversampling Σ/Δ ADCs: one for voltage and two for currents.
- Various measurements:
  - ✓ DC components of voltage and current signals;
  - ✓ Instantaneous /average current and voltage RMS;
  - ✓ Instantaneous /average active/reactive power;
  - ✓ Line frequency;
  - ✓ Phase
- Automatic baud rate adaption UART interface, supporting baud rate: 1200bps~19200bps
- No input crystal required.
- Current input: Shunt resistor or CT
- Operating temperature: -40~+85°C.
- Storage temperature: -55~+150°C.
- Package: 16-SOP.

Pin Description



No.	Mnemonic	Type	Description
1	UP	Input	Positive input for Voltage Channel.
2	IBN	Input	Negative input for Current Channel B.
3	IBP	Input	Positive input for Current Channel B.
4	IAN	Input	Negative input for Current Channel A.
5	IAP	Input	Positive input for Current Channel A.
6	DVCC	Output	Digital power output. Should be connected to a parallel circuit combined by a ⩾4.7uF capacitor and a 0.1uF decoupling capacitor, and then connected to analog ground.
7	NC	-	Floating pin.
8	NC	-	Floating pin.
9	REF	Input /Output	On-chip reference. This pin must be connected to a 1μF capacitor, and then grounded.
10	A1	Input	Both pins are used to set the chip address for the master MCU to

No.	Mnemonic	Type	Description
11	A0	Input	select the slave for communication when more than one chips are used.
12	INT	Output	Interrupt output, high active. This pin outputs system control register self-check interrupt and configuration verification interrupt all the time. This pin can output zero-crossing interrupt and power-down interrupt when interrupt output is enabled.
13	RX	Input	Receiver data input. Hold low logic for at least 70ms to reset the chip.
14	TX	Output	Transmitter data output
15	VSS	Ground	Analog/digital ground.
16	VDD33	Input	3.3V power supply. This pin must be connected to a ⩾0.1μF decoupling capacitor.

Specifications

All maximum/minimum specifications apply over the entire recommended operation range (T=-40°C ~+85°C, VDD33=3.3V±10%) unless otherwise noted. All typical specifications are at TA=25°C, VDD33=3.3V unless otherwise noted.

Parameter	Min.	Typ.	Max.	Unit	Remark
Phase Error Between Channels					
PF=0.8 Capacitive		±0.05		Degree	
PF=0.5 Inductive		±0.05		Degree	
Active Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Active Energy Metering Bandwidth		1.6		kHz	
Reactive Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Reactive Energy Metering Bandwidth		1.6		kHz	

Parameter	Min.	Typ.	Max.	Unit	Remark
VRMS Metering Error		1		%	Dynamic Range 2000:1 @ 25°C Fundamental frequency deviation within ± 25%
VRMS Metering Bandwidth		1.6		kHz	
IRMS Metering Error		1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
IRMS Metering Bandwidth		1.6		kHz	
Frequency Measurement					
Range	40		70	Hz	
Error		0.01		Hz	
Analog Input					
Maximum Signal Level			±200	mV	Peak value
ADC					
DC Offset			10	mV	
Resolution		23		Bit	Sign bit is included.
Bandwidth (-3dB)		1.6		kHz	
On-chip Reference					
Reference Error	-18		18	mV	@ 25°C
Power Supply Rejection Ratio		80		dB	
Temperature Coefficient		10	30	ppm/°C	
Output Voltage		1.210		V	
Power Supply					
VDD33	2.9	3.3	3.6	V	
POR Detection Threshold		1.45		V	Error: ±10%
Power-Down Detection Threshold	2.5	2.7	2.9	V	
Digital Power Supply (DVCC)					
Voltage		1.8		V	Programmable. Error: ±10%
Current			35	mA	

Parameter	Min.	Typ.	Max.	Unit	Remark
Internal High Frequency RC Clock Frequency		3.2768		MHz	Error: ±20%
Logic Output	TX/INT				
Output High Voltage, V_{OH}	1.7			V	Load of 8-mA current in a short time may not damage the chip, but load of 8-mA for a long time may damage the chip.
I_{SOURCE}			8	mA	
Output Low Voltage, V_{OL}			0.7	V	
I_{SINK}			8	mA	
Logic Input	RX/A0/A1				
Input High Voltage, V_{INH}	2.0		3.6	V	
Input Low Voltage, V_{INL}	-0.3		0.7	V	
Input Current, I_{IN}			1	μA	
Input Capacitance, C_{IN}			20	pF	
Baud Rate	1200		19200	bps	Automatic baud rate adaption

Absolute Maximum Ratings

Operating circumstance exceeding Absolute Maximum Ratings may cause permanent damage to the device.

Parameters	Min.	Typ.	Max.	Unit	Description
Digital Power Supply	-0.3		+3.6	V	To ground.
Analog Power Supply	-0.3		+3.6	V	To ground.
Analog Input Voltage (IN/IP/UN/UP)	-0.3		+3.3	V	To ground.
Operating Temperature	-40		+85	°C	
Storage Temperature	-55		+150	°C	
PN Junction Temperature	-40		+125	°C	

Functional Block Diagram

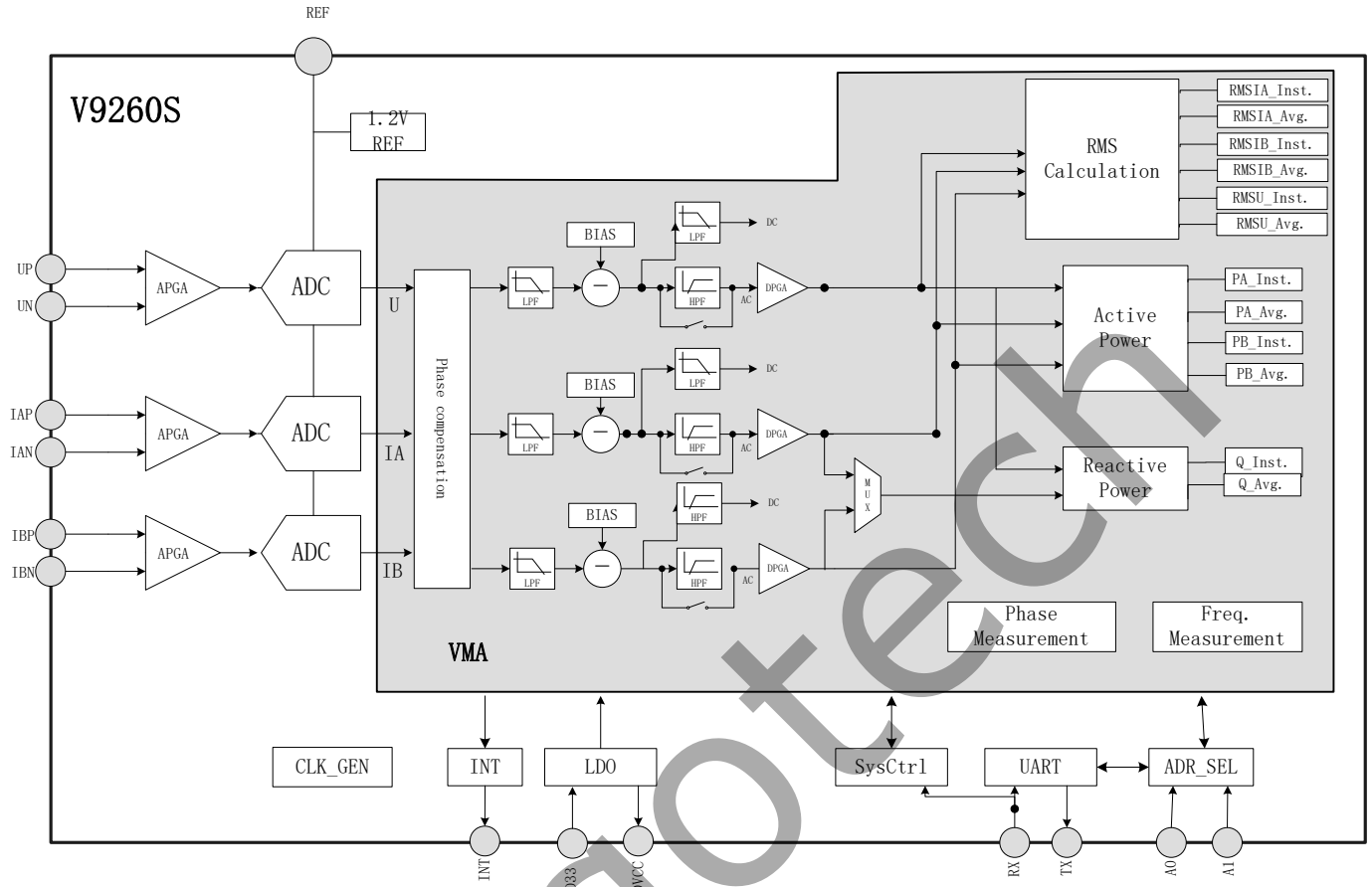


Table of Contents

Revision History **1**

Features **2**

Pin Description **3**

Specifications **4**

Absolute Maximum Ratings **6**

Functional Block Diagram **7**

Table of Contents **0**

Figure List **2**

Table List **3**

1. Reset **5**
1.1. Power-On Reset (POR) 5
1.2. RX Reset 5
1.3. Global Software Reset 6
1.4. Registers 7

2. Clock **8**
2.1. 3.2768-MHz RC Oscillator 8
2.2. 32.768-kHz RC Oscillator 8
2.3. Registers 9

3. Operation Mode **11**
3.1. Metering Mode 11

4. Power Supply **12**
4.1. Power Supply Monitoring Circuit 12
4.2. Power on Reset Circuit 13

5. Bandgap Circuit **14**

6. UART Interface **15**
6.1. Data Byte 15
6.2. Communication Protocol 15
6.2.1. Write Operation 17
6.2.2. Read Operation 17
6.2.3. Broadcast Communication 19

7. Signal Processing **21**
7.1. Analog Input 21
7.2. Analog-to-Digital Conversion 23
7.3. Phase Compensation 24
7.4. Digital Input and DC Removal 25

7.5. RMS Calculation 27
7.5.1. RMS Calculation Equation 28
7.5.2. Gain Calibration of RMS 28
7.5.3. Offset Calibration of RMS 29
7.6. Power Calculation 29
7.6.1. Gain Calibration of Power 31
7.6.2. Offset Calibration of Power 31
7.7. Line Frequency and Phase Measurement 31
7.7.1. Line Frequency Measurement 31
7.7.2. Voltage Phase Measurement 32
7.8. Calibration 33
7.8.1. Registers for Meter Calibration 33
7.8.2. Equations for Calibration 36
7.8.3. Calibration Steps 38

8. Interrupt 40
8.1. Configuration Verification Interrupt 41
8.2. Zero-Crossing Interrupt 43
8.3. Registers 44

9. Registers 45
9.1. System Control Register 45
9.2. Calibration Parameter Registers 49
9.3. Checksum Register 52
9.4. Software Reset Control Register 52
9.5. System Status Registers 53
9.6. Metering Control Registers 55

10. Outline Dimensions 60

Figure List

Figure 1-1 Timing of POR 5
Figure 1-2 Timing of RX Reset 6
Figure 1-3 Timing of Global Software Reset 7
Figure 2-1 Clock Generation 8
Figure 4-1 Power Supply Architecture 12
Figure 4-2 Power-Down Interrupt 13
Figure 6-1 Structure of an 11-Bit Data Byte 15
Figure 6-2 Command Frame for Read/Write/Broadcast Operation 15
Figure 6-3 Timing of UART Communication 16
Figure 7-1 Analog Input of Current Channel 21
Figure 7-2 Analog Input of Voltage Channel 22
Figure 7-3 Phase Compensation 24
Figure 7-4 Digital Input and DC Removal (Current Signal is taken as an Example) 25
Figure 7-5 RMS Signal Processing 27
Figure 7-6 Active Power Calculation 29
Figure 7-7 Line Frequency Measurement Schematic Diagram 31
Figure 8-1 Zero-Crossing Interrupt 43

Table List

Table 1-1 Reset Related Registers 7
Table 2-1 Clock Generation Related Registers 9
Table 3-1 States of Functional Units in Default State 11
Table 4-1 System Control Register (0x0180, SysCtrl, R/W) 12
Table 5-1 Configuration for Bandgap Circuit 14
Table 6-1 UART Communication Timing Parameters 16
Table 6-2 Structure of Data Byte (B7:B0) From Master MCU to V9260S on Write Operation 17
Table 6-3 Structure of Data Byte (B7:B0) From V9260S to Master MCU on Write Operation 17
Table 6-4 Structure of Data Byte (B7:B0) From Master MCU to V9260S on Read Operation 18
Table 6-5 Structure of Data Byte (B7:B0) From V9260S to Master MCU on Read Operation 18
Table 6-6 Structure of Data Byte (B7:B0) From Master MCU to V9260S on Broadcast Operation 19
Table 7-1 Analog PGA Configuration 22
Table 7-2 Analog Control Register 0 (0x0182, AnaCtrl0, R/W) 23
Table 7-3 Analog Control Register 1 (0x0183, AnaCtrl1, R/W) 23
Table 7-4 Enable/Disable ADCs of Each Channel 23
Table 7-5 Registers for phase compensation 24
Table 7-6 f_{smpl} Determines Phase Compensation Resolution and Correction Range 25
Table 7-7 DC Component Calculation Related Register 26
Table 7-8 Digital Gain Configuration of Voltage Signal 26
Table 7-9 RMS Related Registers 27
Table 7-10 Power Related Registers 29
Table 7-11 Bandpass Filter Parameters Address 32
Table 7-12 Voltage Frequency Data Register 32
Table 7-13 Phase Measurement Related Register (R) 33
Table 7-14 Meter Calibration Related Registers 33
Table 8-1 Interrupt Output Enable Bits 40

Table 8-2 Interrupt Flag Bits 40

Table 8-3 Registers for Configuration Verification 42

Table 8-4 System Status Register (0x019D, SysStsClr, R/W) 44

Table 9-1 System Control Register (0x0180, SysCtrl, R/W) 45

Table 9-2 Analog Control Register 0 (0x0182, AnaCtrl0, R/W) 48

Table 9-3 Analog Control Register 1 (0x0183, AnaCtrl1, R/W) 49

Table 9-4 Power/RMS/Low-Current Signal Gain Calibration/Phase Calibration Register (R/W) 50

Table 9-5 Checksum Register (0x0109, CKSUM, R/W) 52

Table 9-6 Software Reset Control Register (0x01BF, SFTRST, W) 52

Table 9-7 System Status Register (0x00CA, SysSts, R) 53

Table 9-8 System Status Register (0x019D, SysStsClr, R/W) 55

1.Reset

In the V9260S, the chip will be reset to Default State when POR, RX reset or global software reset occurs.

1.1. Power-On Reset (POR)

In the V9260S, the internal power-on reset circuit supervises the output voltage on pin DVCC all the time. When the output voltage is lower than 1.45V, the reset signal is generated and forces the chip into reset state. When the output voltage is higher than 1.45V, the reset signal is released and the chip will get to Default State in 500μs.

When POR event occurs, bit RSTSRC (bit[5:3] of SysSts, 0x00CA) is reset to 0b001.

In the reset state, the master MCU and the specific metering architecture cannot access the RAM. When the chip exits from the reset state, the RAM will implement self-check in about 1.25ms. If no error occurs, the RAM can be accessed.

In the reset state, the UART serial interface is idle. The interface starts to run immediately once the chip exits from the reset state.

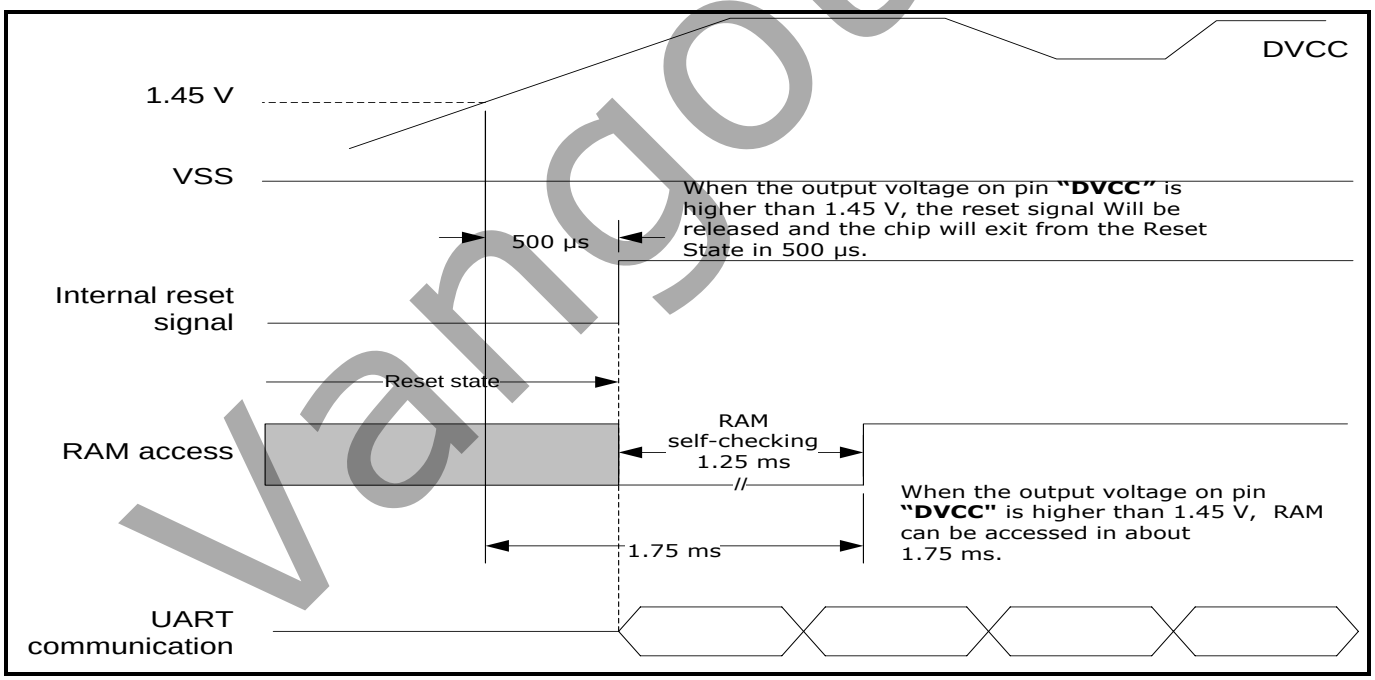


Figure 1-1 Timing of POR

1.2. RX Reset

The input on pin RX must be driven low for at least 70ms to force the chip into the reset state. Pull the logic high, and 900μs later the chip exits from the reset state and gets back to Default State.

When RX reset occurs, bit RSTSRC (bit[5:3] of SysSts, 0x00CA) is reset to 0b011.

In the reset state, the master MCU and the specific metering architecture cannot access the RAM. When the chip exits from the reset state, the RAM will implement self-check in about 1.25ms. If no error occurs, the RAM can be accessed in 30.9ms later after RX reset.

In the reset state, the UART serial interface is idle. The interface starts to run immediately once the chip exits from the reset state.

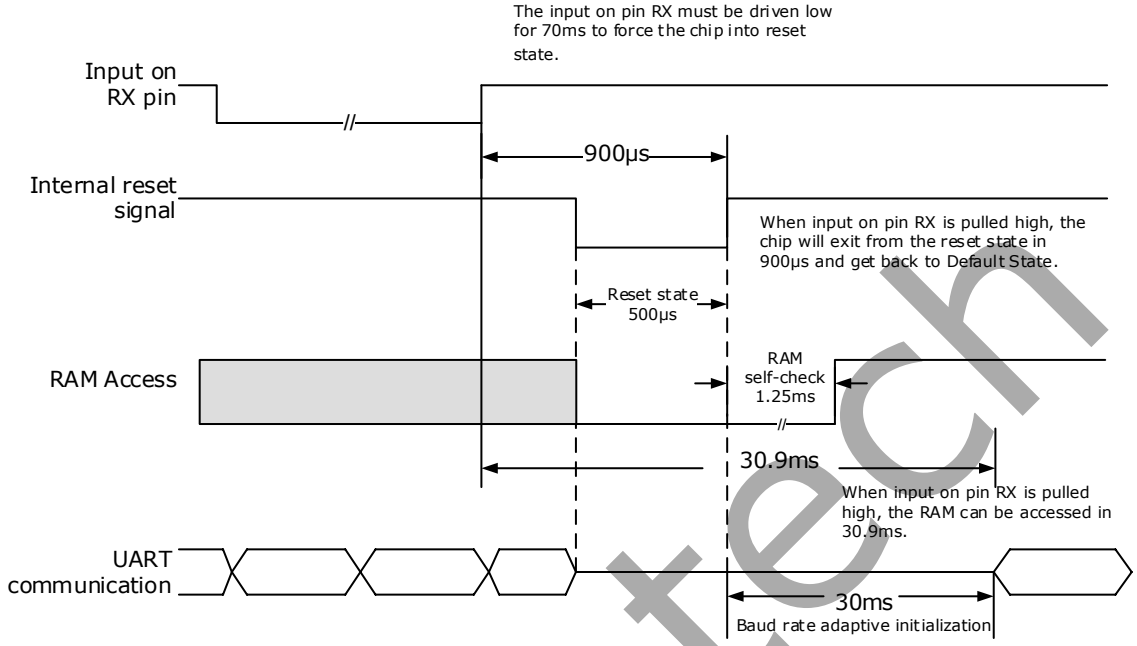


Figure 1-2 Timing of RX Reset

1.3. Global Software Reset

In the V9260S, writing of 0x4572BEAF in the register SFTRST (0x01BF) can force the chip into the reset state, and the chip will exit and get back to Default State in 650μs.

When global software reset occurs, bit RSTSRC (bit[5:3]of SysSts, 0x00CA) is reset to 0b100.

In the reset state, the master MCU and the specific metering architecture cannot access the RAM. When the chip exits from the reset state, the RAM will implement self-check in about 1.25ms. If no error occurs, the RAM can be accessed.

In the reset state, the UART serial interface is idle. The interface starts to run immediately once the chip exits from the reset state.

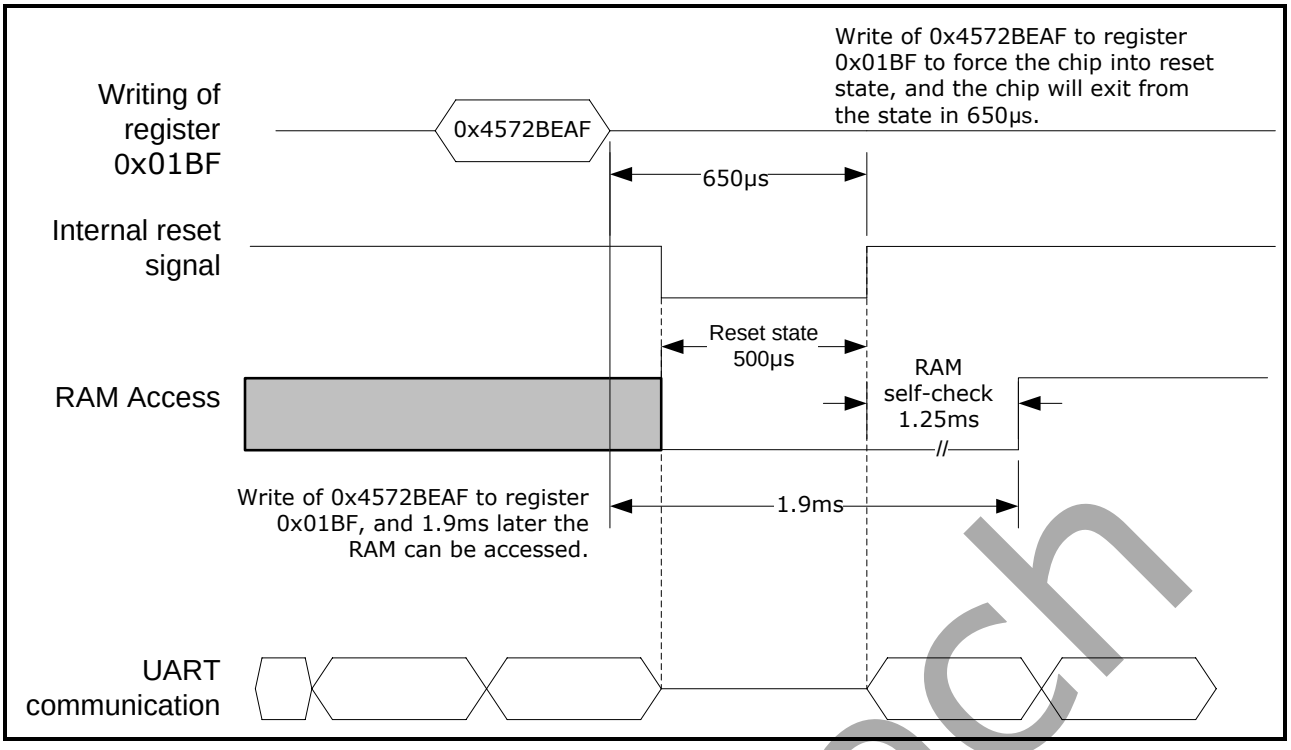


Figure 1-3 Timing of Global Software Reset

1.4. Registers

Table 1-1 Reset Related Registers

Register	Bit	Description
0x00CA SysSts	Bit[5:3] RSTSRC	Flag bits to indicate the reset source. Bit5 Bit4 Bit3 Description 0 0 1 A POR event occurred. 0 0 0 Reserved. 0 1 1 An RX reset event occurred. 0 1 0 Reserved. 1 0 0 A global software reset occurred.
0x01BF, SFTRST Software Reset Control Register		Readable and writable, in the form of 32-bit 2's complement. Write 0x4572BEAF to the register to reset the system.

2.Clock

There are 2 on-chip RC oscillation circuits (3.2MHz/32KHz) provide clocks for the V9260S:

- On-chip 3.2768MHz RC oscillator generates the clock (CLK1) that works as a clock source for the specific metering architecture (VMA), ADCs and UART serial interface. This circuit can be disabled. After POR, RX reset or global software reset, this circuit will be enabled automatically.
- On-chip 32.768kHz RC oscillator generates the clock (CLK2) that works as the clock source for the filters for some key IO ports. This circuit keeps on working until the system is powered off.

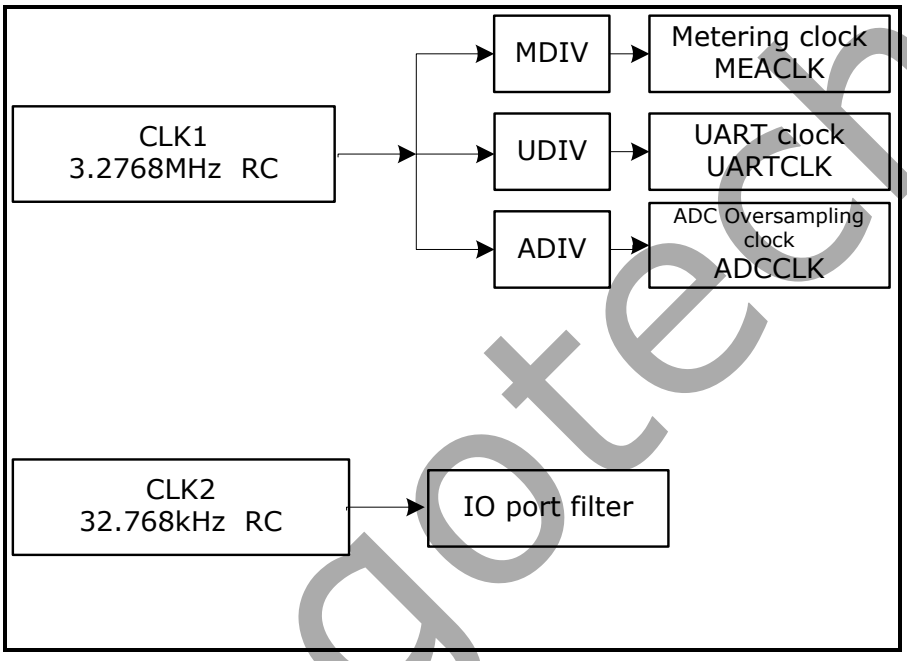


Figure 2-1 Clock Generation

2.1. 3.2768-MHz RC Oscillator

In the V9260S, an on-chip 3.2768MHz RC oscillator is designed to generate a 3.2768-MHz (The deviation is within ± 20% from chip to chip for mass production. The temperature deviation from -40~85 degree for each specific chip is less than 3%.) clock (CLK1) to work as a clock source for the specific metering architecture, ADCs and UART serial interface.

2.2. 32.768-kHz RC Oscillator

The on-chip 32.768-kHz RC oscillator can generate a 32.768kHz RC clock (CLK2) for the filters for some key IO ports. This oscillator cannot be disabled until the system is powered off.

2.3. Registers

Table 2-1 Clock Generation Related Registers

Register	Bit	Default	Description
0x0180 SysCtrl	Bit[21:20] ADCCLKSEL<1:0>	2'b00	To select the sampling frequency of the oversampling ADC (ADC clock, ADCCLK). The sampling frequency of the ADCs must be a quarter or one eighth of the metering clock (MEACLK) frequency when the chip operates with full functions in Metering Mode. 00: 819.2kHz; 01: 409.6kHz; 10: 204.8kHz; 11: 102.4kHz. When the chip operates with full functions in Metering Mode, their default values are recommended to be used for the best performance.
	Bit19 MEACLKSEL	0	To select the clock frequency for the specific metering architecture (MEACLK). 0: 3.2768MHz; 1: 819.2kHz.
	Bit[11:7] RCTRIM<4:0>	0	Adjust the internal high frequency RC clock frequency (Default value is 3.2768MHz.). The default 0b00000 is not adjusted. For the normal metering, it is recommended to write default values for best performance. From **"0b00001"** to **"0b01111"**, the RC clock frequency is decreased by 2% per LSB. From **"0b11111"** to **"0b10000"**, the RC clock frequency is increased by 2% per LSB.
	Bit6 RCX12	0	RC frequency adjustment. The default frequency of the metering chip is 50Hz. When the 60Hz system is applied, users can increase the high frequency RC clock default frequency of 3.2MHZ to 1.2 times of the original. 0: No adjustment 1: X1.2

3.Operation Mode

When the chip is working, it can be reset to Default State when POR, RX reset, or global software reset occurs. Table 3-1 lists the states of functional units in the V9260S in Default State.

In Default State, the typical load current is 500μA. Some easy configuration can drive the chip to work in Metering Mode.

Table 3-1 States of Functional Units in Default State

Functional Unit	Default State
3.2MHz RC oscillator	Enabled.
32kHz RC oscillator	Enabled.
Bandgap circuit	Enabled.
Biasing circuit	Enabled.
Power supply monitoring circuit	Enabled.
POR circuit	Enabled.
LDO	Enabled.
ADC	Disabled.
Specific metering architecture	Enabled, but for configuration verification only.
Interrupt management circuits	Enabled. The parameter configuration self-checking error interrupt is always output high. The other interrupt output can be masked.
UART serial interface	Enabled.

3.1. Metering Mode

In Default State, the V9260S will enter Metering Mode via some easy configuration:

- to enable or disable the ADCs, to configure the sampling frequency to 819.2kHz or 204.8kHz;
- to configure MEACLK frequency to 3.2768MHz or 819.2kHz; the operating mode can be configured to enable only the parameter configuration self-checking or to achieve all functions.

4.Power Supply

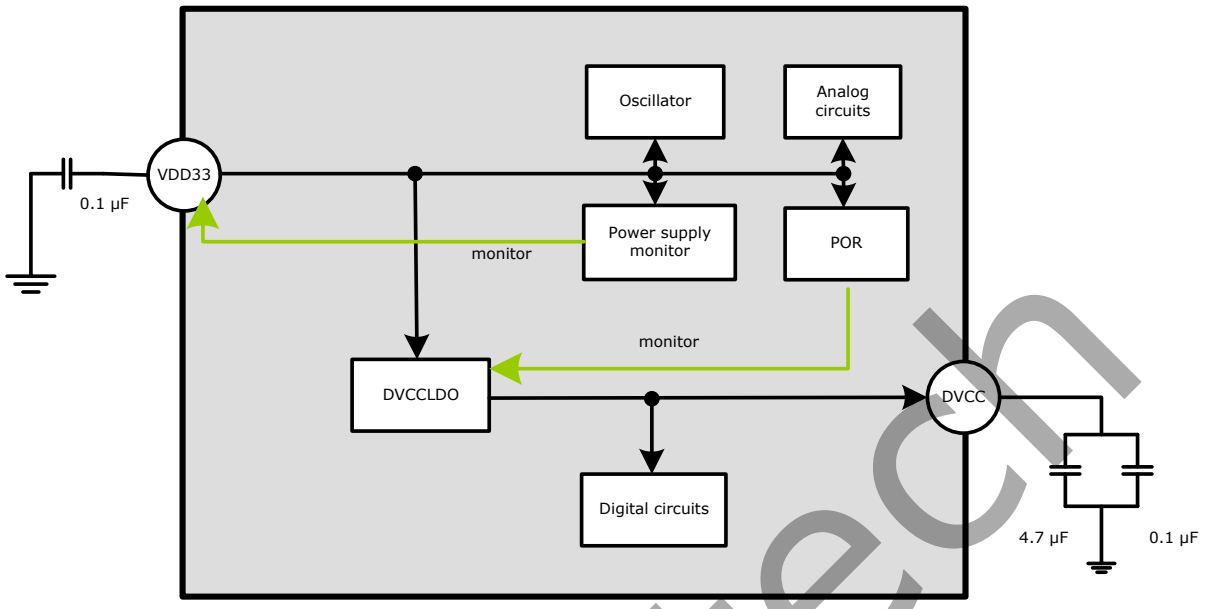


Figure 4-1 Power Supply Architecture

The V9260S supports a power input 3.3V.

The VDD33 is for the digital circuit power supply, and for the analog circuit power supply, oscillator, power-on reset, and power-down detection circuit are integrated. The connection among the modules as shown above.

Table 4-1 System Control Register (0x0180, SysCtrl, R/W)

0x0180, R/W, System Control Register, SysCtrl			
Bit		Default	Description
Bit4	IEPDN	0	Enable power-down interrupt output. Disabled by default. 0: Disable; 1: Enable.

4.1. Power Supply Monitoring Circuit

In the V9260S, an internal power supply monitoring circuit is designed to supervise the power input on pin VDD33. When the input on pin VDD33 is less than Power-Down detection threshold, a power-down interrupt signal is triggered, and the flag bit PDN (bit7 of SysSts) and PDN_R(bit6 of SysSts) are set to 1. When the power down event disappears, the flag bit PDN will be cleared automatically and PDN_R(bit6 of SysSts) should be cleared manually

When the interrupt output is enabled (IEPDN = 1, bit4 of SysSts), the pin **"INT"** will output the high

logic signaling the master MCU that V9260S has been powered down until the power supply is higher than Power-Down detection threshold.

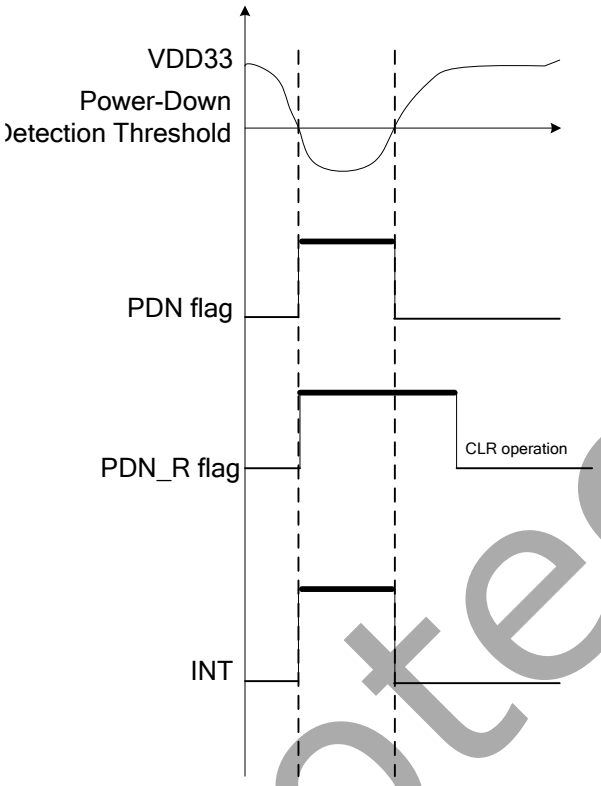


Figure 4-2 Power-Down Interrupt

4.2. Power on Reset Circuit

In the V9260S, the internal power-on reset circuit supervises the output voltage on pin DVCC all the time. When the output voltage is lower than 1.45V, the reset signal is generated and forces the chip into reset state. When the output voltage is higher than 1.45V, the reset signal is released. Please refer to 1.1 Power-On Reset (POR).

5.Bandgap Circuit

In the V9260S, the Bandgap circuit outputs a reference voltage and bias voltage, about 1.210V with a typical temperature coefficient of 10ppm/°C, for ADCs and the 3.2MHz RC oscillator.

By default the Bandgap circuit is enabled.

Users can configure bit[18:16](REST<2:0>) and bit[15:14](RESTL<1:0>) of SysCtrl (0x0180) to adjust the temperature coefficient to compensate the temperature coefficient error introduced by the external components with the following steps:

1) Assume the current settings of relative bits are REST<2:0>='010' and RESTL<1:0>='00', which means an additional +20ppm for temperature coefficient of Bandgap.

2) Measure meter errors in high and low temperature conditions. Assume user has calibrated the meter error to 0 at 20℃, and the measuring errors are 0.6% at 80℃ and -0.4% at -40℃ separately. Then a -(0.6%-(-0.4%))/2=-0.5% measuring error needs to be compensated relative to high temperature working condition, equivalent to -0.5%/(80-20)=-5000/60=-83ppm, rounding to -80ppm.

3) As measuring error is minus two times of REF temperature coefficient error, to compensate a -80ppm error, an additional +40ppm of Bandgap REF temperature coefficient adjustment is needed. Taking the initial +20ppm setting into consideration, the actual adjustment should be +60ppm. According to the lookup table of RESTL<1:0> and REST<2:0>, user should set register RESTL<1:0> to '01' and REST<2:0> to '111', whose combination equals to a +60ppm temperature coefficient adjustment.

A temperature coefficient drift of x in the Bandgap circuit results in a drift of -2x in the measurement error.

Table 5-1 Configuration for Bandgap Circuit

Register	bit	Description
SysCtrl 0x0180	Bit[18:16] REST<2:0>	To finely adjust the temperature coefficient of the Bandgap circuit. In order to obtain the best metering performance and temperature performance during normal metering, it must be configured according to the calculated result. The calculation method, please refer to Bandgap Circuit chapter. 000: no adjustment; 001: +10ppm (recommended); 010: +20ppm; 011: +30ppm; 100: -40ppm; 101: -30ppm; 110: -20ppm; 111: -10ppm.
	Bit[15:14] RESTL<1:0>	To roughly adjust the temperature coefficient of the Bandgap circuit. In order to obtain the best metering performance and temperature performance during normal metering, it must be configured according to the calculated result. The calculation method, please refer to Bandgap Circuit chapter. 00: 0; 01: +70ppm; 10: -140ppm; 11: -70ppm (recommended).

6.UART Interface

The V9260S supports communication with the master MCU as a slave via UART serial interface. The UART serial interface has features:

- Asynchronous, half-duplex communication;
- A 11-bit data byte, composed of 1-bit Start bit, 8-bit Data bits, 1-bit Parity bit (odd), and 1-bit Stop bit;
- Least significant bit (LSB) shifted in or out firstly when the chip receives or transmits a byte;
- Automatic baud rate adaption: support 1200bps~19200bps.

When a reset event, such as POR, RX reset or global software reset, occurs, the UART serial interface is reset.

6.1. Data Byte

The data byte received and transmitted via the UART serial interface of the V9260S is composed of 11 bits, including 1-bit Start bit (logic low), 8-bit Data bits, 1-bit odd Parity bit and 1-bit Stop bit (logic high), as shown in the following figure. When the V9260S receives or sends a data byte, the least significant bit always is shifted in or out firstly.

Figure 6-1 Structure of an 11-Bit Data Byte

6.2. Communication Protocol

In read, write or broadcast communication, the master MCU needs a command frame that is composed of 8 data bytes to operate a 32-bit data in the V9260S.

Head Byte	Control Byte	Address Byte	Data Byte 0	Data Byte 1	Data Byte 2	Data Byte 3	Check Byte

Figure 6-2 Command Frame for Read/Write/Broadcast Operation

In read or write operation, when the V9260S receives the command frame from the master MCU, it will reply to the master MCU with a respond frame of different structures. In broadcast communication, the V9260S will not reply to the master MCU to avoid communication conflict.

The following figure depicts the timing of UART communication.

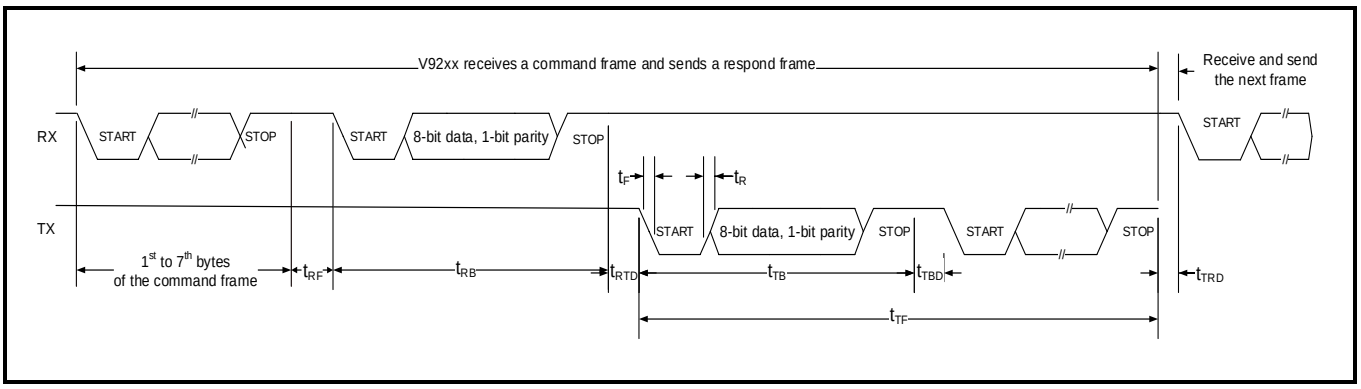


Figure 6-3 Timing of UART Communication

Table 6-1 UART Communication Timing Parameters

Parameter	Description
t_{RB}	Time to receive a data byte on pin RX. $t_{RB}=\frac{11}{baudrate}$ Where, *baudrate* is the actual baud rate.
t_{RF}	The maximum time between two bytes when receiving a command frame on pin **"RX"** t_{RF}=20ms After a timeout event, the UART interface is idle and waits for the next command frame.
t_{RTD}	The delay between command frame reception on pin RX and respond frame transmission on pin TX. 1ms≤t_{RTD}≤20ms Please note no respond frame will be transmitted in broadcast communication, and at least 1ms delay is recommended between two continuous command frames for broadcast communications.
t_{TF}	Time to transmit a respond frame in read or write operation, depending on the structure of the frame.
t_{TB}	Time to transmit a data byte. $t_{TB}=\frac{11}{baudrate}$ Where *baudrate* is the actual baud rate.
T_{TBD}	Delay between two continuous data bytes in a respond frame. 0ms≤t_{TBD}≤20ms
t_{TRD}	The delay between respond frame transmission on pin TX and the next command frame reception on pin RX. More than 1ms is recommended.
t_R	Rise time of RX and TX, about 300ns.

Parameter	Description
t_F	Fall time of RX and TX, about 300ns.

6.2.1. Write Operation

The master MCU needs a command frame, composed of 8 data bytes, to write of a 32-bit data to the register of the V9260S. When it receives the command frame, the V9260S will transmit a respond frame, composed of 4 data bytes, to reply to the master MCU. On both transmission and reception, the LSB is shifted in or out firstly.

In Control Byte, B3 and B2, determined by input on pins A1 and A0, are used to select the slave chip when more than one chip are used.

Table 6-2 Structure of Data Byte (B7:B0) From Master MCU to V9260S on Write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Head Byte	0	1	1	1	1	1	0	1
2	Control Byte	The higher 4 bits of the target register address.				A1	A0	1	0
3	Address Byte	The lower 8 bits of the target register address.							
4	Data Byte 0	Bit[7:0] of the target data.							
5	Data Byte 1	Bit[15:8] of the target data.							
6	Data Byte 2	Bit[23:16] of the target data.							
7	Data Byte 3	Bit[31:24] of the target data.							
8	Check Byte	The checksum. Add the above 7 data bytes, invert the sum, and then add it to 0x33 to obtain the checksum.							

Table 6-3 Structure of Data Byte (B7:B0) From V9260S to Master MCU on Write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Head Byte	0	1	1	1	1	1	0	1
2	Control Byte	The higher 4 bits of the target register address.				A1	A0	1	0
3	Address Byte	The lower 8 bits of the target register address.							
4	Check Byte	The checksum. Add the above 3 data bytes, invert the sum, and then add it to 0x33 to obtain the checksum.							

6.2.2. Read Operation

The master MCU needs a command frame, composed of 8 data bytes, to read of a 32-bit data of a register of the V9260S. When it receives the command frame, the V9260S will transmit a respond frame,

composed of 4×N+4 (1≤N≤255) data bytes, to reply to the master MCU. On both transmission and reception, the LSB is shifted in or out firstly.

In Control Byte, B3 and B2, determined by input on pins A1 and A0, are used to select the slave chip when more than one chip are used.

Table 6-4 Structure of Data Byte (B7:B0) From Master MCU to V9260S on Read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Head Byte	0	1	1	1	1	1	0	1
2	Control Byte	The higher 4 bits of the target register address (D_1).				A1	A0	0	1
3	Address Byte	The lower 8 bits of the target register address (D_1).							
4	Data Byte 0	The length (N, in unit of Word) of the data to be read from the registers located at the addresses beginning with the target address (D_1) given by the Control Byte and Address Byte. When Data Byte 0 is 0, it means 1 data word (4 bytes) is read out. When the master MCU reads of the target address only, N is 1. When more than one registers located at continuous addresses beginning with the target address (D_1), N is equal to the number of the address. The maximum value of N is 255, which means no more than 255 continuous registers can be read at a time.							
5	Data Byte 1	No actual function.							
6	Data Byte 2								
7	Data Byte 3								
8	Check Byte	The checksum. Add the above 7 data bytes, invert the sum, and then add it to 0x33 to obtain the checksum.							

Table 6-5 Structure of Data Byte (B7:B0) From V9260S to Master MCU on Read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Head Byte	0	1	1	1	1	1	0	1
2	Control Byte	The higher 4 bits of the target register address (D_1).				A1	A0	0	1
3	Length Byte	N, equal to Data Byte 0 sent from master MCU to V9260S on read operation. When Data Byte 0 is 0, N is equal to 1.							
4	Data Byte 10	Bit[7:0] of the register located at target address (D_1).							
5	Data Byte 11	Bit[15:8] of the register located at target address (D_1).							
6	Data Byte 12	Bit[23:16] of the register located at target address (D_1).							
7	Data Byte 13	Bit[31:24] of the register located at target address (D_1).							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
8	Data Byte 20	Bit[7:0] of the register located at address D_2 (D_2=D_1+1).							
9	Data Byte 21	Bit[15:8] of the register located at address D_2 (D_2=D_1+1).							
…	…	…							
4×N+0	Data Byte N0	Bit[7:0] of the register located at address D_N (D_N=D_1+N-1).							
4×N+1	Data Byte N1	Bit[15:8] of the register located at address D_N (D_N=D_1+N-1).							
4×N+2	Data Byte N2	Bit[23:16] of the register located at address D_N (D_N=D_1+N-1).							
4×N+3	Data Byte N3	Bit[31:24] of the register located at address D_N (D_N=D_1+N-1).							
4×N+4	Check Byte	The checksum. Add the above 4×N+3 data bytes, invert the sum, and then add it to 0x33 to obtain the checksum.							

6.2.3. Broadcast Communication

The master MCU needs a command frame, composed of 8 data bytes, to write a 32-bit data to the registers of more than one V9260S in broadcast communication. When receiving a command frame, the V9260S should not transmit a respond frame to reply to the master MCU to avoid communication error. On receiving a data frame, the LSB is shifted in or out firstly.

When the external MCU processes two consecutive broadcast write operations to the metering chip, it is recommended to wait for at least 1ms.

Table 6-6 Structure of Data Byte (B7:B0) From Master MCU to V9260S on Broadcast Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Head Byte	0	1	1	1	1	1	0	1
2	Control Byte	The higher 4 bits of the target register address.				X*	X*	0	0
3	Address Byte	The lower 8 bits of the target register address.							
4	Data Byte 0	Bit[7:0] of the target data.							
5	Data Byte 1	Bit[15:8] of the target data.							
6	Data Byte 2	Bit[23:16] of the target data.							
7	Data Byte 3	Bit[31:24] of the target data.							
8	Check Byte	The checksum. Add the above 7 data bytes, invert the sum, and then add it to 0x33 to obtain the checksum.							
*X can be 0 or 1.									

7.Signal Processing

The metering clock (MEACLK) is sourced by CLK1, generated by the 3.2MHz RC oscillator.

7.1. Analog Input

The V9260S supports 2 analog input of current channels.

For the current channel, a current transformer (CT) or shunt resistor can be used for analog inputs. The double-ended full differential input is adopted. The wiring is shown as below. The shunt resistor can also be used for the current input with AGND grounded.

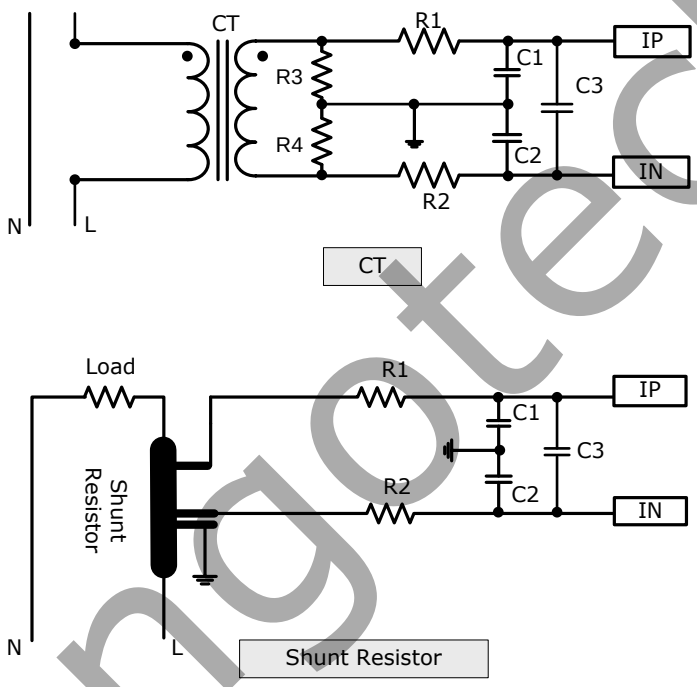


Figure 7-1 Analog Input of Current Channel

For voltage channel, a potential transformer (PT) or a resistor-divider network can be used for analog inputs. The current channel consists of 2 fully differential voltage inputs. And the voltage channel consists of 2 pseudo differential voltage inputs: UP is positive input for voltage channel, and UN (inside the chip), connected to ground, is negative input for voltage channel.

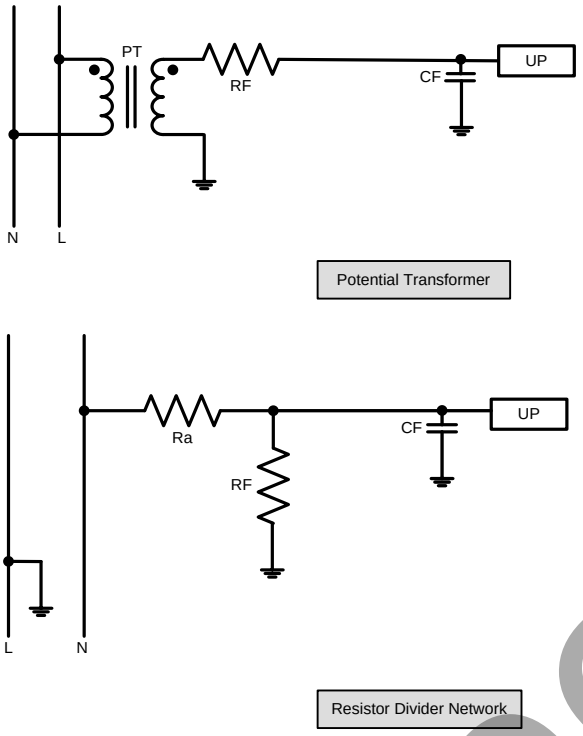


Figure 7-2 Analog Input of Voltage Channel

Each input has a maximum voltage of ±200mV, and each pair of a maximum differential voltage of ±400mV. To match the output signal of the transformers to the measurement scale of the ADCs, analog programmable gain amplifiers (APGA) with possible gain selection of 1, 4, 16, and 32 for current input, and of 1 and 4 for voltage input, are set. The analog PGA gain is determined by the output signal of the transformer. The product of the output signal and PGA gain (including digital and analog PGA) must be no higher than voltage reference. Equation 7-1 depicts the signal processing of current and voltage:

$$U' = PGAu \times (Au \times \sin\omega t + DCu)$$
$$I' = PGAi \times [Ai \times \sin(\omega t + \psi) + DCi]$$

Equation 7-1

Where *PGAu* and *PGAi* is the analog PGA gain for voltage and current; *Au* and *Ai* are the amplitude of the input signals (V); *DCu* and *DCi* are the DC components of the raw voltage and current.

Table 7-1 Analog PGA Configuration

Register	Bit	Default	Description
0x0180 SysCtrl	Bit26 GU	0	To set analog PGA gain of analog input of Voltage Channel. 0, ×4 (recommended); 1, ×1.
	Bit[25:24] GIB<1:0>	0	To set analog PGA gain of analog input of Current Channel (IB). The analog PGA gain is determined by the output signal of the sensor. The product of the output signal and PGA gain (both analog and digital) must be no more than voltage reference. 00: ×32; 01: ×16; 10: ×4; 11: ×1.
	Bit[23:22]	0	To set analog PGA gain of analog input of Current Channel (IA).

Register	Bit	Default	Description
	GIA<1:0>		The analog PGA gain is determined by the output signal of the sensor. The product of the output signal and PGA gain (both analog and digital) must be no more than voltage reference. 00: ×32; 01: ×16; 10: ×4; 11: ×1.

Table 7-2 Analog Control Register 0 (0x0182, AnaCtrl0, R/W)

Register	Bit	Default	Description
0x0182 AnaCtrl0	Bit[9:8]	IT<1:0>	Adjust the global bias current. 00: -33%; 01: 1; 10: -66%; 11: -75%. Under the normal metering condition, this bit must hold the default value for proper operation.

Table 7-3 Analog Control Register 1 (0x0183, AnaCtrl1, R/W)

Register	Bit	Default	Description
0x0183 AnaCtrl1	Bit[29:28]	CSEL<1:0>	Adjust the Miller capacitance of I channel ADC. 00: No adjustment; 01: Increase 33%; 10: Increase 66%; 11: Increase 100%. For normal metering, the recommended configuration is 0b01.

7.2. Analog-to-Digital Conversion

Second-order Σ-ΔADCs are applied in the voltage and current channels in the V9260S. In the default state, all ADCs are disabled.

Table 7-4 Enable/Disable ADCs of Each Channel

Register	Bit	Default	Description
0x0180 SysCtrl	Bit29 ADCUPDN	0	Set this bit to 1 to enable U Channel ADC. This bit is cleared by default.
	Bit28 ADCIBPDN	0	Set this bit to 1 to enable IB Channel ADC. This bit is set to 0 by default.

Register	Bit	Default	Description
	Bit27 ADCIAPDN	0	Set this bit to 1 to enable IA Channel ADC. This bit is set to 0 by default.

7.3. Phase Compensation

After the analog signal is converted to a digital signal by an ADC, it is subjected to the phase compensation by the input phase compensation module to eliminate the phase error between the voltage and current signals due to the mismatch of the sampling circuit and the ADC.

A phase compensation circuit composed of a chain of time-delay units is applied to correct the phase error between the current and voltage signals. According to the phase lead or lag relationship between the voltage and current, select one of the signals into the delay circuit for phase compensation. In register 0x00F7, users can configure the phases of IA and IB.

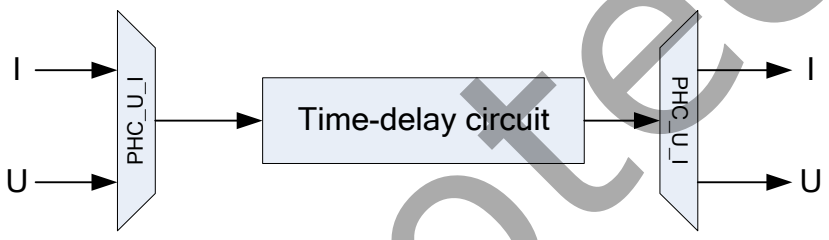


Figure 7-3 Phase Compensation

Table 7-5 Registers for phase compensation

Register	Bit	Default	Description
0x00F7 PHC	Bit[24:16] PHCIB	0	Where Bit24 is the sign bit of IB channel phase compensation value. 1: Delay voltage signal; 0: Delay current signal. Bit [24:16]: 9-bit 2's complement. When the operating clock (f_{smpl}) of metering chip is 3.2768MHz, the phase compensation resolution is 0.005°/bit, and the maximum phase error correction range is ±1.4°.
	Bit[8:0] PHCIA	0	Where Bit8 is the sign bit of IA channel phase compensation value. 1: Delay voltage signal; 0: Delay current signal. Bit [8:0]: 9-bit 2's complement. When the operating clock (f_{smpl}) of metering chip is 3.2768MHz, the phase compensation resolution is 0.005°/bit, and the maximum phase error correction range is ±1.4°.

The sampling frequency (f_{smpl}) of the phase compensation circuit is 3.2768 MHz by default. The phase compensation resolution is 0.005°/lsb, and the maximum phase error correction range is ±1.4°. The

sampling frequency (f_{smpl}) of the phase compensation circuit is determined by the configuration of the MEACLKSEL bit (bit 19, SysCtrl, 0x0180).

Compensate the phase error at power factor of 0.5L. The value (N) of the phase compensation control register can be calculated by the following formula (rounded up to the result of the calculation):

$$N = \mathrm{Round}\left(\frac{3011}{2} \times E \times \frac{fsmpl}{819200}\right) \qquad \text{Equation 7-2}$$

Where

N is the value to be set in bit[8:0] and bit[24:16] of register PHC (0x00F7);

E is the error displayed in LCD screen of the calibration equipment.

f_{smpl} is determined by the configuration of MEACLKSEL bits (Bit19, SysCtrl, 0x0180).

Table 7-6 f_{smpl} Determines Phase Compensation Resolution and Correction Range

N	Configuration		f_{smpl} (Hz)	Resolution (°/lsb)	Correction Range (°)
[-255, +255]	MEACLKSEL bit19, 0x0180	0	3276800	0.005	1.4
		1	819200	0.022	5.6

7.4. Digital Input and DC Removal

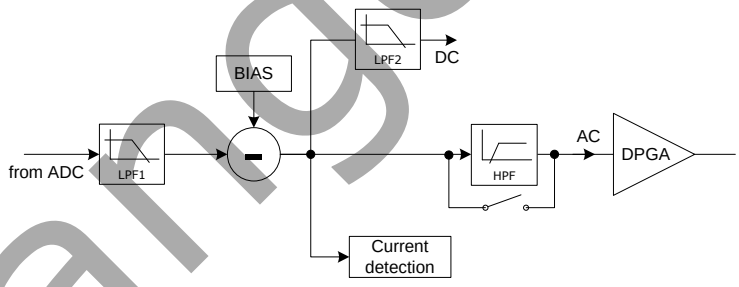


Figure 7-4 Digital Input and DC Removal (Current Signal is taken as an Example)

The 1-bit code stream output from the oversampling Σ/ΔADC can be enabled to be sent to the decimation filter to suppress the high-frequency noise and to lower the sampling frequency to get the raw waveform of each signal. And finally the original waveform of the 29-bit (bit[28:27] sign bit) is received.

The signal input to the decimation filter is enabled or disabled via configuring bit[29:27] of SysCtrl, 0x0180. When this function is enabled, the code stream is accumulated to the filter; when this function is disabled, a constant "0" is input for digital signal processing.

The raw waveform is transferred to a subtractor to remove the direct drift introduced by the external components and ADCs, with the help of the DC bias preset in registers IAADCC (0x0104), IBADCC (0x0105)and UADCC (0x0106). Then, the signals are processed as follows:

- The signals are transferred to low-pass filter LPF2 to obtain the DC components of the signals that can be read out from registers for DC components;

- By default the signals are transferred to a high-pass filter (HPF) to remove the DC components of the raw waveforms and obtain the AC components to calculate power and RMS;

The method of obtaining the DC bias value of the oversampling ADC in the IA, IB and U channels is:

- (1)Set Bit[13:12] of SysCtrl (0x0180), SHORTU, and SHORTI;
- (2)Read the values of DC measurement register IADCINST (0x00DA), IBDCINST (0x00DB), UDCINST (0x00D9) and write into the register IAADCC (0x0104), IBADCC (0x0105) and UADCC (0x0106).
- (3)Clear Bit[13:12] of SysCtrl (0x0180), SHORTU, and SHORTI;

In the DC metering application scenario, the users can disable the DC removal high-pass filter by configuring the BPHPF bit (bit2, SysCtrl, 0x0180) and configure DC bias values in register IAADCC (0x0104), IBADCC (0x0105) and UADCC (0x0106) to eliminate the DC drift introduced by external devices and ADCs, so that DC power can be calculated.

The data format of the DC component register of the voltage / current signal is 32-bit complement. The read operation is valid and the write operation is meaningless.

When the energy metering clock frequency is 3.2768MHz, the DC component register data update time is 160ms and the settling time is 320ms.

When the energy metering clock frequency is 819.2kHz, the DC component register data update time is 640ms and the settling time is 1280ms.

Table 7-7 DC Component Calculation Related Register

Register			Description
Configuration Register	0x0104	IAADCC	A channel ADC bias current calibration
	0x0105	IBADCC	B channel ADC bias current calibration
	0x0106	UADCC	Voltage ADC bias DC calibration
Data Output Register	0x00D9	UDCINST	Instantaneous voltage DC component
	0x00DA	IADCINST	A channel instantaneous DC component
	0x00DB	IBDCINST	B channel instantaneous DC component

The users can configure the digital gain of the voltage signal through the system control register (SysCtrl, 0x0180) to amplify the AC component of the signal. It can be configured up to 4 times, but the product of the maximum input signal and the total gain should be guaranteed to be less than the reference voltage. It is recommended to use the analog gain for gain adjustment.

Table 7-8 Digital Gain Configuration of Voltage Signal

Register	Bit	Default	Description
0x0180 SysCtrl	Bit1 PGAU	0	Configure voltage (U) channel digital gain. 0: ×1; 1: ×4.

7.5. RMS Calculation

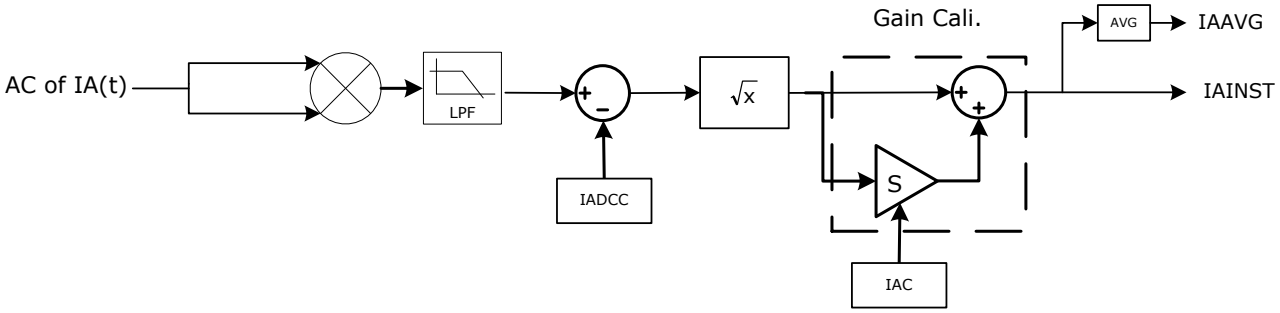


Figure 7-5 RMS Signal Processing

Table 7-9 RMS Related Registers

Address	Register	Description	R/W	Data Format
0x00CE	IAINST	A channel instantaneous current RMS	R	32-bit 2's complement
0x00CF	UINST	Instantaneous voltage RMS	R	32-bit 2's complement
0x00D3	IAAVG	A channel average current RMS	R	32-bit 2's complement
0x00D4	UAVG	Average voltage RMS	R	32-bit 2's complement
0x00D6	IBINST	B channel instantaneous current RMS	R	32-bit 2's complement
0x00D8	IBAVG	B channel average current RMS	R	32-bit 2's complement
0x00FD	IAC	A channel current RMS gain calibration	R/W	32-bit 2's complement
0x00FE	IADCC	A channel current RMS low-current calibration	R/W	32-bit2's complement
0x00FF	UC	Voltage RMS gain calibration	R/W	32-bit 2's complement
0x0102	IBC	B channel current RMS gain calibration	R/W	32-bit 2's complement
0x0103	IBDCC	B channel current RMS low-current calibration	R/W	32-bit2's complement
0x0108	UDCC	Voltage RMS value low-current signal	R/W	32-bit 2's complement

Address	Register	Description	R/W	Data Format
		calibration		

7.5.1. RMS Calculation Equation

In the metering chip design, the voltage/current RMS calculation equation (Take current IA as an example):

$$Irms = \frac{\sqrt{2}}{2} \times 0.99992 \times PGAdi \times \frac{PGAi \times Ai}{1.210}$$ Equation 7-3

Where,

PGAdi is the digital PGA gains of current;

PGAi is the analog PGA gains of current;

Ai is the amplitude of current input;

1.210V is the reference voltage;

0.99992 is the gain introduced by the filters.

According to the above method, the raw RMS of each channel signal is obtained. After the gain calibration, the instantaneous RMS (U / I) is obtained, and then the average RMS (U / I) is obtained. All of the above values are stored in the corresponding data registers.

When MEACLK frequency is 3.2768MHz, the data are updated in 10ms and settled in 160ms; the update time for all voltage / current RMS values is 320ms and the settling time is 960ms.

When MEACLK frequency is 819.2kHz, the data are updated in 40ms and settled in 640ms; the update time for all voltage / current RMS values is 1.28s and the settling time is 3.84s.

7.5.2. Gain Calibration of RMS

The current or voltage RMS calculated via the above equations must be gain calibrated, as depicted in the following equation:

$$RMS = RMS' \times (1 + S)$$ Equation 7-4

Where,

RMS' is the raw current or voltage RMS, calculated via the above equations;

RMS is the current or voltage RMS after calibration;

S is the gain calibration, set in registers (IAC, IBC, UC).

7.5.3. Offset Calibration of RMS

In order to eliminate the crosstalk noise, the metering chip supports the offset calibration of RMS, the users can eliminate the noise power by setting the IADCC, IBDCC and UDCC.

Take IA channel as an example, the implementation method is as follows:

Set the current input on the calibration equipment to 0. The average RMS IAAVG is read, and IAAVG ^ 2 is calculated. In the 64bit data, bit[39:8] is taken as the empirical value of the offset calibrated RMS to write into register IADCC.

When the current is re-applied, the accuracy of the current RMS will be effectively improved.

7.6. Power Calculation

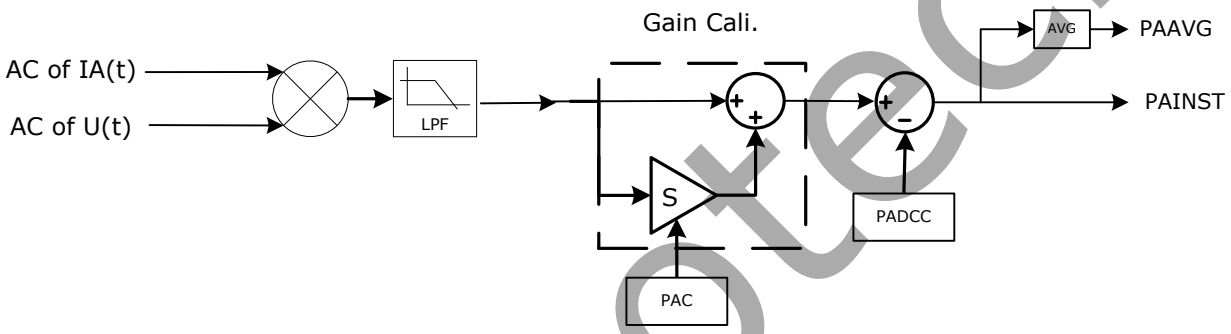


Figure 7-6 Active Power Calculation

The active power is acquired via the following equation:

$$P = \frac{1}{2} \times \frac{Ai \times PGAi \times PGAdi}{1.210} \times \frac{Au \times PGAu \times PGAdu}{1.210} \times \cos\theta \times 0.99985$$ Equation 7-5

Where, *PGAdi* and *PGAdu* are digital PGA gains of current and voltage; *PGAi* and *PGAu* are analog PGA gains of current and voltage; *Ai* and *Au* are the amplitude of current and voltage inputs; *θ* is the phase difference between voltage and current signals; 0.99985 is the gain introduced by the filters.

When MEACLK frequency is 3.2768MHz, registers for instantaneous active power are updated in 160ms and settled in 480ms; and registers for average active power are updated in 640ms and settled in 1.28s.

When MEACLK frequency is 819.2kHz, registers for instantaneous active power are updated in 640ms and settled in 1920ms; and registers for average active power are updated in 2.56s and settled in 5.12s.

The reactive power calculation principle is the same as the active power'.

Table 7-10 Power Related Registers

Address	Register	Description	R/W	Data Format
0x00CC	PAINST	A channel instantaneous active power value	R	32-bit 2's complement

Address	Register	Description	R/W	Data Format
0x00CD	QINST	instantaneous reactive power value	R	32-bit 2's complement
0x00D0	PAAVG	A channel average active power value	R	32-bit 2's complement
0x00D1	QAVG	Average reactive power value	R	32-bit 2's complement
0x00D7	PBAVG	B channel average active power value	R	32-bit 2's complement
0x00D8	IBAVG	B channel average current RMS	R	32-bit 2's complement
0x00F6	PAC	To set gain calibration of active power for A channel	R/W	32-bit 2's complement
0x00F8	PADCC	Low-current signal calibration of active power for A channel	R/W	32-bit 2's complement
0x00F9	QAC	To set gain calibration of reactive power for A channel	R/W	32-bit 2's complement
0x00FA	QBC	To set gain calibration of reactive power for B channel	R/W	32-bit 2's complement
0x00FB	QADCC	A reactive power low-current signal calibration	R/W	32-bit 2's complement
0x00FC	QBDCC	B reactive power low-current signal calibration	R/W	32-bit 2's complement
0x0100	PBC	To set gain calibration of active power for A channel	R/W	32-bit 2's complement
0x0101	PBDCC	Low-current signal calibration of active power for B channel	R/W	32-bit 2's complement

7.6.1. Gain Calibration of Power

In the metering chip design, in order to correct the system deviation between the various channels, the calculated active power and reactive power are required to be processed with the gain calibration first and then be stored into the corresponding data registers.

Assuming the raw active power is P', the RMS after calibration is P, and the gain calibration value is S, the relationship among the three is as follows:

$$P = P' \times (1 + S)$$ Equation 7-6

The users can set the corresponding gain calibration values in the power gain registers (PAC, PBC, QC).

7.6.2. Offset Calibration of Power

In order to eliminate the crosstalk noise, the metering chip supports the offset calibration of power. The users can eliminate the noise power by setting the PADCC, PBDCC and QDCC.

7.7. Line Frequency and Phase Measurement

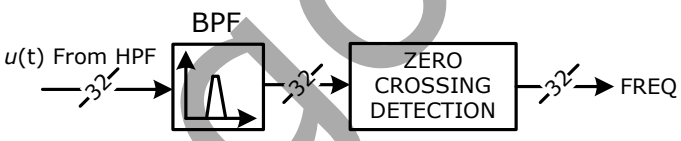


Figure 7-7 Line Frequency Measurement Schematic Diagram

7.7.1. Line Frequency Measurement

The V9260S supports line frequency measurement. In the line frequency measurement circuit, the fundamental voltage signal is sampled at a frequency of 6400Hz for negative-to-positive zero-crossing detection. Each cycle (20ms) outputs a frequency measurement (ie, the number of samples between two positive zero-crossing values), stored in the frequency instantaneous value register (FREQ, 0x00CB, read only). In order to improve the frequency measurement accuracy, the average 16 cycles operation is proceeded toward the instantaneous frequency to get the average frequency (FREQAVG, 0x00D2 readable and writable).

In the V9260S, a band-pass filter is applied to remove the direct component, the noise and the harmonic wave of the voltage signal to obtain the fundamental voltage for line frequency measurement. The performance of the band-pass filter is affected by the number of bits to be shifted and the filter coefficient. When fewer bits are shifted, the filter needs less time to respond, is less sensitive to the frequency deviation, and has less capability to depress the noise and harmonics.

The voltage frequency value can be calculated as follows:

$$f = 0.00390625 \times \mathrm{K}' \times \frac{\mathrm{T8BAUD}}{\mathrm{FREQAVG}}$$ Equation 7-7

Where:

F: Actual voltage frequency

T8BAUD: Value of the register (0x00E0)

FRQAVG: Value of the average frequency register (0x00D2)

K ': Actual baud rate, known by master MCU

When a POR reset, software reset, or RX reset occurs, the voltage frequency register will be reset.

Table 7-11 Bandpass Filter Parameters Address

	Register		R/W	Description	Default
0x0107	BPFPARA	Bandpass filter coefficient	R/W	The filter is used to separate the fundamental signal to allow for more accurate frequency measurement and phase measurement. At 3.2M clock, the users need to write into 0x806764B6.	0

Table 7-12 Voltage Frequency Data Register

Register		Description
0x00CB	FREQINST	Instantaneous frequency value register. Read only. When the energy metering clock frequency is 3.2768MHz, it will be updated every 20ms.
0x00D2	FREQAVG	Frequency average value per second register. Readable and writable. When the energy metering clock frequency is 3.2768MHz, it will be updated every 320ms.

7.7.2. Voltage Phase Measurement

The metering chip supports the voltage phase measurement function. The signal processing is shown in Figure 7-7. The working principle is that the master MCU broadcasts command via UART to write 1 to the register PHS_STT (0x0198). When it is analyzed as the phase measurement command by the chip, 6.4kHz sampling frequency will be used (At normal operating frequency, the voltage signal sampling points per cycle is 128 points, that is, 6.4kHz sampling frequency) for counting until the positive zero-crossing event occurs. The counting value will be written into the phase register PHDAT (0x00DE), and the positive two voltage sampling values before and after zero-crossing, ZXDATREG (0x00DC), ZXDAT (0x00DD), will be recorded to facilitate the users to do interpolation operations for more accurate phase values.

In the multi-metering chip system, according to the values of this register, the phase relationship and the phase difference among each metering chips can be determined.

Table 7-13 Phase Measurement Related Register (R)

Address	Register	R/W	Data format	Default	Description
0x00DC	ZXDATREG	R	32-bit 2's complement	0	The previous sampling value of zero-crossing
0x00DD	ZXDAT	R	32-bit 2's complement	0x80000000	The sampling value of zero-crossing
0x00DE	PHDAT	R	32-bit 2's complement	1	Voltage phase data

7.8. Calibration

7.8.1. Registers for Meter Calibration

Table 7-14 Meter Calibration Related Registers

Address	Register	Description	R/W	Data Format
0x00CB	FREQINST	Instantaneous frequency value	R	32-bit 2's complement
0x00CC	PAINST	A channel instantaneous active power value	R	32-bit 2's complement
0x00CD	QINST	instantaneous reactive power value	R	32-bit 2's complement
0x00CE	IAINST	A channel instantaneous current RMS	R	32-bit 2's complement
0x00CF	UINST	Instantaneous voltage RMS	R	32-bit 2's complement
0x00D0	PAAVG	A channel average active power value	R	32-bit 2's complement
0x00D1	QAVG	Average reactive power value	R	32-bit 2's complement
0x00D2	FREQAVG	Average frequency value	R	32-bit 2's complement
0x00D3	IAAVG	A channel average current RMS	R	32-bit 2's complement
0x00D4	UAVG	Average voltage RMS	R	32-bit 2's complement

Address	Register	Description	R/W	Data Format
0x00D5	PBINST	B channel instantaneous active power value	R	32-bit 2's complement
0x00D6	IBINST	B channel instantaneous current RMS	R	32-bit 2's complement
0x00D7	PBAVG	B channel average active power value	R	32-bit 2's complement
0x00D8	IBAVG	B channel average current RMS	R	32-bit 2's complement
0x00F6	PAC	To set gain calibration of active power for A channel	R/W	32-bit 2's complement
0x00F7	PHC	To set phase calibration of active power	R/W	32-bit 2's complement Where Bit24 is the sign bit of IB channel phase compensation value. 1: Delay voltage signal; 0: Delay current signal. Bit [24:16]: 9-bit 2's complement. Where Bit8 is the sign bit of IA channel phase compensation value. 1: Delay voltage signal; 0: Delay current signal. Bit [8:0]: 9-bit 2's complement. When the operating clock (f_{smpl}) of metering chip is 3.2768MHz, the phase compensation resolution is 0.005°/bit, and the maximum phase error correction range is ±1.4°.
0x00F8	PADCC	Low-current signal calibration of active power for A channel	R/W	32-bit 2's complement
0x00F9	QAC	To set gain calibration of reactive power for A channel	R/W	32-bit 2's complement
0x00FA	QBC	To set gain calibration of reactive power for B channel	R/W	32-bit 2's complement

Address	Register	Description	R/W	Data Format
0x00FB	QADCC	A reactive power low-current signal calibration	R/W	32-bit 2's complement
0x00FC	QBDCC	B reactive power low-current signal calibration	R/W	32-bit 2's complement
0x00FD	IAC	A channel current RMS gain calibration	R/W	32-bit 2's complement
0x00FE	IADCC	A channel current RMS low-current calibration	R/W	32-bit2's complement
0x00FF	UC	Voltage RMS gain calibration	R/W	32-bit 2's complement
0x0100	PBC	To set gain calibration of active power for A channel	R/W	32-bit 2's complement
0x0101	PBDCC	Low-current signal calibration of active power for B channel	R/W	32-bit 2's complement
0x0102	IBC	B channel current RMS gain calibration	R/W	32-bit 2's complement
0x0103	IBDCC	B channel current RMS low-current calibration	R/W	32-bit2's complement
0x0104	IAADCC	A channel ADC bias current calibration	R/W	32-bit 2's complement
0x0105	IBADCC	B channel ADC bias current calibration	R/W	32-bit 2's complement
0x0106	UADCC	Voltage ADC bias DC calibration	R/W	32-bit 2's complement
0x0107	BPFPARA	Bandpass filter coefficient	R/W	The filter is used to separate the fundamental signal to allow for more accurate frequency measurement and phase measurement. At 3.2M clock, the users need to write into 0x806764B6.
0x0108	UDCC	Voltage RMS value low-current signal calibration	R/W	32-bit 2's complement

7.8.2. Equations for Calibration

1. Equation for current/voltage RMS registers

$$RMS = V \times G \times K \qquad \text{Equation 7-8}$$

Where, *V* is the RMS value of the input signal; *G* is the gain; and *K* is a coefficient, K=9.19495302×10^8.

Example 1: When the sampling signal of the voltage channel is 36.7mV and the gain is 4, the value of the average voltage RMS register (0x00D4) should be

RMS=0.0367×4×9.19495302×10^8=0x80BA916

2. Equation for active/reactive power registers

Including: Average active power register (PAAVG, 0x00D0) and average reactive power register (QAVG, 0x00D1). The value of the active power register can be calculated according to the following equation:

$$P = Vi \times Gi \times Vv \times Gv \times B_p \times \cos\theta \qquad \text{Equation 7-9}$$

$$Q = Vi \times Gi \times Vv \times Gv \times Bp \times \sin\theta \qquad \text{Equation 7-10}$$

Where, *Vi* and *Vv* are RMS of the input current and voltage; *Gi* and *Gv* are the analog PGA gains for current and voltage respectively; *cosθ* is the power factor; *θ* is the phase difference between the current signal and the voltage signal ; B_p is a coefficient, B_p=7.09441×10^8.

Example: When Vv is 36.7mV; Gv is 4; Vi is 0.875mV; Gi is 32; cosθ is 1, the value of average active power register (PAAVG, 0x00D0) should be:

$$P_{value} = 0.000875 \times 32 \times 0.0367 \times 4 \times 7.09441 \times 10^8 = 0x2C7EF6$$

3. Equation for ratio of RMS and power

The value acquired by Equation 7-8, Equation 7-9 and Equation 7-10 is the theoretical value of the register of RMS or power. It must be multiplied by a ratio to get the actual value as shown on the LCD screen (Accurate to the second decimal place).

The data of the current/voltage RMS/power register can be calculated according to Equation 7-8, Equation 7-9 and Equation 7-10 (there is a difference between the calculated data and the direct reading of the corresponding register data, but not much different). This data is only ADC sampling data, if users want to convert it into intuitive RMS/power data, the users need to calculate a fixed ratio by the following equation, and multiply the actual reading of the register and the ratio to get the correct voltage/current RMS/power, that is, RMS and power data shown on the LCD screen.

$$D = \frac{V_n}{Value} \qquad \text{Equation 7-11}$$

Where, *Value* is the value of voltage/current RMS/power registers acquired by Equation 7-8, Equation 7-9 and Equation 7-10; *D* is the ratio; and V_n is the rated voltage/current/power.

4. Equation for registers for phase compensation

Phase compensation is to ensure that the low power factor can also maintain certain measurement accuracy. Users must first complete the gain calibration, and then the phase compensation.

The values corresponding to the 9-bit 2's complement of bit [8: 0] of the phase compensation register (PHC, 0x00F7) are used to set the phase compensation values.

Compensate the phase error at power factor of 0.5L . The value (N) of the phase compensation control register can be calculated by the following formula (rounded up to the result of the calculation):

$$N = \text{Round}\left(\frac{3011}{2} \times E \times \frac{fsmpl}{819200}\right) \qquad \text{Equation 7-12}$$

Where

N is the value to be set in bit[8:0] of register PHC (0x00F7);

E is the error displayed in LCD screen of the calibration equipment.

f_{smpl} is determined by the configuration of MEACLKSEL bits (Bit19, SysCtrl, 0x0180).

5. Equation for gain calibration registers

Including all gain registers of power and RMS.

The values of the gain registers can be calculated according to the following equation:

$$S = 2^{31}\left(\frac{1}{1+e} - 1\right) + S_1\left(\frac{1}{1+e}\right) \qquad \text{Equation 7-13}$$

Where,

S is the content to be set in the registers for gain calibration of power or RMS, in the form of 2's complement;

S_1 is the original gain value of the registers; ie the uncalibrated RMS values/the original values of power gain calibration registers, in the form of 2's complement;

e is the error: When this equation is used for the power gain calibration, *e* is the error displayed on the LCD screen of the calibration equipment (*E*); when this equation is used for the current/voltage RMS gain calibration, *e* is the error (E_u/E_i) calculated by Equation 7-16 or Equation 7-17.

6. Equation for power offset calibration registers

Including: Active/Reactive power offset calibration value register.

The value of the power offset calibration value register (C) can be calculated from the following equation:

$$C = -E \times P \times a\% \qquad \text{Equation 7-14}$$

Where,

E is the error displayed on the LCD screen when a% Ib are applied at power factor of 1.0;

P is value of power register, calculated via Equation 7-9 or Equation 7-10.

7.8.3. Calibration Steps

7.8.3.1. Parameters Configuration

Users must configure the following parameters when designing an energy meter:

- Parameters for a meter, including rated current, rated voltage, pulse constant, and accuracy class, etc.
- Parameters for design, including the current and voltage RMS when rated current and rated voltage are applied.
- The analog PGA gains of the current and voltage channels.
- The ratio (D) of RMS and power calculated via Equation 7-11.

When the above parameters are set, no changes should be done to them.

7.8.3.2. Calibrating Power

The step of getting the gain calibration value of the power data (*E*):

1. Read the P_n displayed on the LCD screen of the calibration equipment.
2. Read the power data P_1 from the meter LCD (P_1 is the product of the value of the average power data register and the power data scale coefficient D).
3. Calculate the gain calibration value of the power data according to the following method

$$E_P = \frac{P_1 - P_n}{P_n}$$ Equation 7-15.

1. Gain calibration (Take active power for example)

For example, at power fact of 1.0, apply 100% Ib and 100% Un to the calibration equipment.

Get the gain calibration value of the power data (*E*), and read the value of the gain calibration register (PAC, 0x00F6), (the raw value for gain calibration, S_1) and then calculate the value for gain calibration via Equation 7-13 and write it to the register PAC (0x00F6).

2. Phase compensation

After completing the power gain calibration, in the case of PF = 0.5L, apply 100% Ib and 100% Un to the calibration equipment for the phase calibration.

During the gain calibration, the register PHC (0x00F7) must be cleared first. Get the gain calibration value of the power data (*E*), calibrate the values of phase compensation according to Equation 7-12, and write to the corresponding bit of the register.

3. Power offset calibration (optional)

PF = 1.0, 5% Ib (usually, 2% Ib) and 100% Un are applied to the calibration equipment. Get the gain calibration value of the power data (*E*). The offset calibration values calculated according to Equation 7-14 must be written into the corresponding power offset calibration register.

7.8.3.3. Calibrating Current RMS

1. Write 0 to the current RMS gain calibration register;

2. When the power factor is 1.0, apply 100% Ib current to the calibration equipment;

3. Read the current RMS I1 from the LCD of meter (I1 is the product of the value of average current RMS register and the current RMS scale coefficient D);

4. Calculate the value of gain calibration of current RMS according to the following equation:

Calculate error first: $E_i = \frac{I_1 - Ib}{I_b}$ Equation 7-16, the unit of current is mA;

Calculate the value of gain calibration according to Equation 7-16, and then write to the current RMS gain calibration register.

7.8.3.4. Offset Calibrating of Current RMS (optional)

Take IA channel as an example, the implementation method is as follows:

Set the current input on the calibration equipment to 0. The average RMS IAAVG is read, and IAAVG ^ 2 is calculated. In the 64bit data, bit[39:8] is taken as the empirical value of the offset calibrated RMS to write into register IADCC.

When the current is re-applied, the accuracy of the current RMS will be effectively improved.

7.8.3.5. Calibrating Voltage RMS

1. Write 0 to the voltage RMS gain calibration register;

2. Apply 100% Un voltage to the calibration equipment;

3. Read the voltage RMS U1 from the meter LCD (U1 is the product of the value of the average voltage RMS register and the voltage RMS scale coefficient D)

4. Calculate the gain calibration value of the voltage RMS according to the following method

Calculate error first: $E_u = \frac{U_1 - U_n}{U_n}$ Equation 7-17, the unit of voltage is mV.

Then, calculate the gain calibration value according to Equation 7-17 and write to voltage RMS gain calibration register.

8.Interrupt

In the V9260S, 3 events can trigger interrupt signals that will set the flag bits to 1s. When the interrupt output is enabled, the pin INT will output the interrupt pulse according to the configuration to warn the master MCU.

- Configuration verification interrupt: interrupt output cannot be masked;
- Zero-crossing interrupt: the voltage sign bit is output as the zero-crossing interrupt; interrupt output can be masked;
- Power down interrupt: interrupt output can be masked;

The interrupt management circuit keeps on working until it is powered off.

Table 8-1 Interrupt Output Enable Bits

Register	Bit	Default	Description
0x0180 SysCtrl	Bit5, IEHSE	0	This bit must hold its default value for proper operation.
	Bit4, IEPDN	0	To enable power-down interrupt output. 1: enable; 0: mask.
	Bit3, IESUL	0	To enable voltage sign output. 1: enable; 0: mask.

Table 8-2 Interrupt Flag Bits

Register	Bit	Default	Description
0x00CA SysSts	Bit11 USIGN	0	Voltage sign bit. 1: negative; 0: positive. Read this bit to detect the sign of the voltage. The flag cannot be cleared. This bit toggles following the sign of the voltage.
	Bit7 PDN	0	Power-down interrupt flag bit. When input voltage on pin VDD33 is lower than Power-Down detection threshold, this bit will be set to 1. When the input is higher than Power-Down detection threshold, this bit will be cleared.
	Bit6 PDN_R	0	Power-down interrupt flag latch value. This bit is read as 1 when the system is powered down, ie when the level on the VDD33 pin is below Power-Down detection threshold. When the power-down event disappears, the flag bit will remain 1 and needs to be cleared manually. The flag bit can be cleared by

<table>
<tr><th>Register</th><th>Bit</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="3"></td><td></td><td></td><td>writing zero to the 0x019D Register to the PDN_CLR bit.</td></tr>
<tr><td>Bit[5:3]
RSTSRC</td><td>0</td><td>Bit[5:4] is read only, and bit3 is readable and writable.
Read the Bit [5: 3] to determine the cause of the reset.
Bit5 Bit4 Bit3 Description
0 0 1 A POR occurs.
0 0 0 Reserved.
0 1 1 A RX reset occurs.
0 1 0 Reserved.
1 0 0 A software reset occurs.</td></tr>
<tr><td>Bit2
CHKERR</td><td>0</td><td>Read this bit for the state of configuration verification. The read value is refreshed every 5ms.
Read this bit to determine whether a parameter configuration self-checking error occurs.
Add the content of the registers for calibration, metering control registers, analog control registers, and 3 reserved internal registers to the content of the checksum register to ensure that all the important configurations are in their desired states. If the sum is 0xFFFFFFFF, the verification passes, and this bit is read out as 0; otherwise, the verification fails, and this bit is read out as 1.</td></tr>
</table>

8.1. Configuration Verification Interrupt

The metering chip accumulates all the values of all the registers shown in the following table every 5ms.

The configuration verification measure: add the content of the register CKSUM (0x0109) and that of the other 21 registers listed in the following table. If the sum is 0xFFFFFFFF, it indicates all the configurations are right; otherwise, it indicates some change has occurred to the registers, an interrupt signal will be triggered, the flag bit CHKERR (bit2 of SysSts) will be set to 1. This interrupt output cannot be masked. The configuration verification is executed all the time, and the sum is calculated once every 5ms. The flag bit will hold its state until the sum of the content of 25 registers is 0xFFFFFFFF.

The register CKSUM should be written of the difference between 0xFFFFFFFF and the sum of the content of the other 21 registers.

Table 8-3 Registers for Configuration Verification

No	Register			R/W	Default value
1	0x00F6	PAC	To set gain calibration of active power for A channel	R/W	0
2	0x00F7	PHC	To set phase calibration of active power	R/W	0
3	0x00F8	PADCC	Low-current signal calibration of active power for A channel	R/W	0
4	0x00F9	QAC	To set gain calibration of reactive power for A channel	R/W	0
5	0x00FA	QBC	To set gain calibration of reactive power for B channel	R/W	0
6	0x00FB	QADCC	A reactive power low-current signal calibration	R/W	0
7	0x00FC	QBDCC	B reactive power low-current signal calibration	R/W	0
8	0x00FD	IAC	A channel current RMS gain calibration	R/W	0
9	0x00FE	IADCC	A channel current RMS low-current calibration	R/W	0
10	0x00FF	UC	Voltage RMS gain calibration	R/W	0
11	0x0100	PBC	To set gain calibration of active power for A channel	R/W	0
12	0x0101	PBDCC	Low-current signal calibration of active power for B channel	R/W	0
13	0x0102	IBC	B channel current RMS gain calibration	R/W	0
14	0x0103	IBDCC	B channel current RMS low-current calibration	R/W	0
15	0x0104	IAADCC	A channel ADC bias current calibration	R/W	0
16	0x0105	IBADCC	B channel ADC bias current calibration	R/W	0
17	0x0106	UADCC	Voltage ADC bias DC calibration	R/W	0

No	Register			R/W	Default value
18	0x0107	BPFPARA	Bandpass filter coefficients	R/W	0
19	0x0108	UDCC	Voltage RMS low-voltage signal calibration	R.W	0
20	0x0109	CKSUM	checksum	R/W	0
21	0x0180	SysCtrl	System configuration register	R/W	0
22	0x0182	AnaCtrl0	Analog control register 0	R/W	0
23	0x0183	AnaCtrl1	Analog control register 1	R/W	0

8.2. Zero-Crossing Interrupt

The V9260S supports voltage zero-crossing interrupt.

When the voltage signal crosses the zero point, a zero-crossing interrupt is triggered, the sign bit USIGN (bit11, SysSts) toggles following the voltage signal.

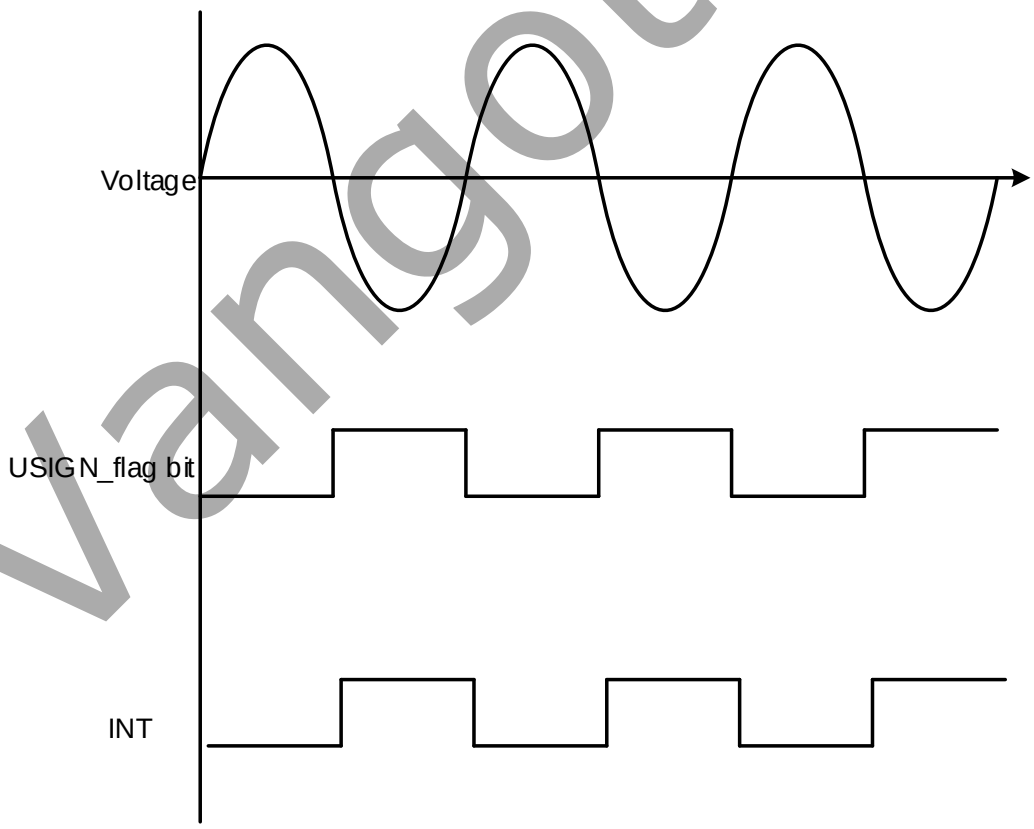


Figure 8-1 Zero-Crossing Interrupt

8.3. Registers

Table 8-4 System Status Register (0x019D, SysStsClr, R/W)

0x019D, System Status Register, SysStsClr				
bit		R/W	Default	Description
Bit[31:10]	Reserved	R/W	N/A	The read value is indeterminate and meaningless.
Bit9	PHSDONE_CLR	R/W	0	The flag bit for whether the phase measurement ends or not. 0: Not finished; 1: Finished. It can be cleared by writing 0 to this bit.
Bit[8:7]	Reserved	R/W	N/A	The read value is indeterminate and meaningless.
Bit6	PDN_CLR	R/W	0	Power down interrupt flag. This bit is read as 1 when the system is powered down, ie when the level on the VDD33 pin is below Power-Down detection threshold. When the power-down event disappears, the flag is read as a value of 1. It can be cleared by writing 0 to this bit.
Bit[5:0]	Reserved	R/W	N/A	The read value is indeterminate and meaningless.

9.Registers

9.1. System Control Register

When power-on reset (POR), RX reset or global software reset occurs, the system control register will be reset to its default state. If not specifically noted, the default values in the tables of this section are in format of hexadecimal. The system control register participates in the parameter configuration self-checking.

Table 9-1 System Control Register (0x0180, SysCtrl, R/W)

0x0180, R/W, System Control Register, SysCtrl			
bit		Default	Description
Bit[31:30]	Reserved	0	These bits must hold their default values for proper operation.
Bit29	ADCUPDN	0	Set this bit to 1 to enable the voltage (U) channel ADC. U channel ADC is disabled by default.
Bit28	ADCIBPDN	0	Set this bit to 1 to enable the current (IB) channel ADC. IB channel ADC is disabled by default.
Bit27	ADCIAPDN	0	Set this bit to 1 to enable the current (IA) channel ADC. IA channel ADC is disabled by default.
Bit26	GU	0	U channel ADC analog gain control. 0: ×4; 1: ×1. For normal metering, it is recommended to write default values for optimum metering performance.
Bit[25:24]	GIB<1:0>	00	IB channel ADC analog gain control. The users should determine the PGA according to the sensor's output signal size. It should ensure that the product of maximum signal and PGA is less than the reference voltage. 00: ×32; 01: ×16; 10: ×4; 11: ×1.

0x0180, R/W, System Control Register, SysCtrl			
bit		Default	Description
Bit[23:22]	GIA<1:0>	00	IA channel ADC analog gain control. The users should determine the PGA according to the sensor's output signal size. It should ensure that the product of maximum signal and PGA is less than the reference voltage. 00: ×32; 01: ×16; 10: ×4; 11: ×1.
Bit[21:20]	ADCCLKSEL<1:0>	00	Configure the oversampling ADC clock frequency (sampling frequency). In the normal metering, it is necessary to ensure that the ADC sampling frequency is one quarter or one eighth of the energy metering clock frequency 00: 819.2kHz; 01: 409.6kHz; 10: 204.8kHz; 11: 102.4kHz. In the normal metering, in order to obtain the best metering performance, it is recommended to write the default values.
Bit19	MEACLKSEL	0	Select the energy metering clock frequency. 0: 3.2768MHz; 1: 819.2kHz. In the normal metering, it is necessary to ensure that the ADC sampling frequency is one quarter or one eighth of the energy metering clock frequency
Bit[18:16]	REST<2:0>	0	The temperature coefficient of the voltage reference (Bandgap) circuit is slightly adjusted. In order to obtain the best metering performance and temperature performance during normal metering, it must be configured according to the calculated result. The calculation method, please refer to Bandgap Circuit chapter. 000: 0ppm; 001: +10ppm; 010: +20ppm; 011: +30ppm; 100: -40ppm; 101: -30ppm; 110: -20ppm; 111: -10ppm.

0x0180, R/W, System Control Register, SysCtrl			
bit		Default	Description
Bit[15:14]	RESTL<1:0>	0	The temperature coefficient of the voltage reference (Bandgap) circuit is roughly adjusted. In order to obtain the best metering performance and temperature performance during normal metering, it must be configured according to the calculated result. The calculation method, please refer to Bandgap Circuit chapter. 00: 0ppm; 01: +70ppm; 10: -140ppm; 11: -70ppm.
Bit13	SHORTU	0	When the U channel is input with a DC signal, this bit can be set to 1 to short the U channel amplifier to obtain the offset value of the ADC itself. This function is disabled by default. For normal metering, user must write default values.
Bit12	SHORTI	0	When I channel is input with the DC signal, this bit can be set to 1 to short I channel amplifier to obtain the offset value of the ADC itself. This function is disabled by default. For normal metering, user must write default values.
Bit[11:7]	RCTRIM<4:0>	0	To adjust the internal high-frequency RC clock frequency. (The ideal value is 3.2768MHz.) Default:0b000000, no adjustment is applied. When the chip operates with full functions in Metering Mode, it is recommended to hold their default values for the best performance. From **"0b00001"** to **"0b01111"**, the RC clock frequency is decreased by 2% per LSB. From **"0b11111"** to **"0b10000"**, the RC clock frequency is increased by 2% per LSB.
Bit6	RCX12	0	RC frequency adjustment. The default frequency of the metering chip is 50Hz. When it is necessary to apply to the 60Hz system, users can increase the high frequency RC clock default frequency of 3.2768MHZ to 1.2 times of the original. 0: No adjustment 1: X1.2

0x0180, R/W, System Control Register, SysCtrl			
bit		Default	Description
Bit5	IEHSE	0	This bit must hold the default value for proper operation.
Bit4	IEPDN	0	Enable power-down interrupt output. It is disabled by default. 0: Disable; 1: Enable.
Bit3	IESUL	0	Enable voltage sign bit output. It is disabled by default. 0: Disable; 1: Enable.
Bit2	BPHPF	0	Bypass high-pass filter. During the default signal processing, the high-pass filter is enabled. It is necessary to enable this bit for the DC metering. 0: Enable high-pass filter. Only the voltage / current signal AC component is involved in RMS / power calculation; 1: Bypass high-pass filter. The voltage / current signal DC and AC components are involved in RMS / power calculation.
Bit1	PGAU	0	Configure the voltage (U) channel digital gain. 0: ×1; 1: ×4.
Bit0	CHSEL	0	Reactive power/energy metering channel selection. There is only one reactive power/energy metering signal path. 0: IA; 1:IB.

Table 9-2 Analog Control Register 0 (0x0182, AnaCtrl0, R/W)

0x0182，R/W，Analog Control Register 0，AnaCtrl0			
Bit		Default	Description
Bit[31:10]	Reserved	0	This bit must hold the default value for proper operation.
Bit[9:8]	IT<1:0>	0	Adjust the global bias current. 00: -33%; 01: 1; 10: -66%; 11: -75%. Under the normal metering condition, this bit must hold the default value for proper operation.
Bit[7:0]	Reserved	0	This bit must hold the default value for proper operation.

Table 9-3 Analog Control Register 1 (0x0183, AnaCtrl1, R/W)

0x0183，R/W，Analog Control Register 1，AnaCtrl1			
Bit		Default	Description
Bit[31:30]	Reserved	0	This bit must hold the default value for proper operation.
Bit[29:28]	CSEL<1:0>	0	Adjust the Miller capacitance of I channel ADC. 00: No adjustment; 01: Increase 33%; 10: Increase 66%; 11: Increase 100%. For normal metering, the recommended configuration is 0b01.
Bit[27:0]	Reserved	0	This bit must hold the default value for proper operation.

9.2. Calibration Parameter Registers

When power-on reset (POR), RX reset or global software reset occurs, the calibration parameter registers will be reset to the default state. If not specifically noted, the default values in the tables of this section are in format of hexadecimal.

The calibration parameter registers participate in the parameter configuration self-checking.

Table 9-4 Power/RMS/Low-Current Signal Gain Calibration/Phase Calibration Register (R/W)

Address	Register		R/W	Description	Default
0x00F6	PAC	To set gain calibration of active power for A channel	R/W	32-bit 2's complement	0
0x00F7	PHC	To set phase calibration of active power	R/W	32-bit 2's complement Where Bit24 is the sign bit of IB channel phase compensation value. 1: Delay voltage signal; 0: Delay current signal. Bit [24:16]: 9-bit 2's complement. Where Bit8 is the sign bit of IA channel phase compensation value. 1: Delay voltage signal; 0: Delay current signal. Bit [8:0]: 9-bit 2's complement. When the operating clock (f_{smpl}) of metering chip is 3.2768MHz, the phase compensation resolution is 0.005°/bit, and the maximum phase error correction range is ±1.4°.	0
0x00F8	PADCC	Low-current signal calibration of active power for A channel	R/W	32-bit 2's complement	0
0x00F9	QAC	To set gain calibration of reactive power for A channel	R/W	32-bit 2's complement	0
0x00FA	QBC	To set gain calibration of reactive power for B channel	R/W	32-bit 2's complement	0

Address	Register		R/W	Description	Default
0x00FB	QADCC	A reactive power low-current signal calibration	R/W	32-bit 2's complement	0
0x00FC	QBDCC	B reactive power low-current signal calibration	R/W	32-bit 2's complement	0
0x00FD	IAC	A channel current RMS gain calibration	R/W	32-bit 2's complement	0
0x00FE	IADCC	A channel current RMS low-current calibration	R/W	32-bit2's complement	0
0x00FF	UC	Voltage RMS gain calibration	R/W	32-bit 2's complement	0
0x0100	PBC	To set gain calibration of active power for A channel	R/W	32-bit 2's complement	0
0x0101	PBDCC	Low-current signal calibration of active power for B channel	R/W	32-bit 2's complement	0
0x0102	IBC	B channel current RMS gain calibration	R/W	32-bit 2's complement	0
0x0103	IBDCC	B channel current RMS low-current calibration	R/W	32-bit2's complement	0
0x0104	IAADCC	A channel ADC bias current calibration	R/W	32-bit 2's complement	0
0x0105	IBADCC	B channel ADC bias current calibration	R/W	32-bit 2's complement	0

Address	Register		R/W	Description	Default
0x0106	UADCC	Voltage ADC bias DC calibration	R/W	32-bit 2's complement	0
0x0107	BPFPARA	Bandpass filter coefficient	R/W	The filter is used to separate the fundamental signal to allow for more accurate frequency measurement and phase measurement. At 3.2M clock, the users need to write into 0x806764B6.	0
0x0108	UDCC	Voltage RMS value low-current signal calibration	R/W	32-bit 2's complement	0

9.3. Checksum Register

Table 9-5 Checksum Register (0x0109, CKSUM, R/W)

Register		Default	R/W	Format	Description
0x0109	CKSUM	0	R/W	32-bit 2's complement	Add the value of this register and other related registers (including metering control registers, analog control registers, registers for calibration) to compute the checksum for configuration verification to ensure the configuration of all the registers are in the desired states. If the sum is 0xFFFFFFFF, the verification passes. This register should be set to the difference of 0xFFFFFFFF and the sum of the other 23 registers.

9.4. Software Reset Control Register

Table 9-6 Software Reset Control Register (0x01BF, SFTRST, W)

Register		Default	R/W	Format	Description
0x01BF	SFTRST	0	R/W	32-bit 2's complement	Readable and writable, in the form of 32-bit 2's complement. Write 0x4572BEAF to the register to reset the system.

9.5. System Status Registers

Table 9-7 System Status Register (0x00CA, SysSts, R)

0x00CA, System Status Register, SysSts				
Bit		R/W	Default	Description
Bit[31:12]	Reserved	R	N/A	These values are indeterminate and meaningless.
Bit11	USIGN	R	0	Voltage sign bit. 1: negative; 0: positive. Read this bit to detect the sign of the voltage. The flag cannot be cleared. This bit toggles following the sign of the voltage.
Bit10	Reserved	R	N/A	These values are indeterminate and meaningless.
Bit9	PHSDONE_R	R	0	The latch value of flag bit for whether the phase measurement ends or not. 0: Not finished; 1: Finished.
Bit8	BISTERR	R	0	The internal RAM will be self-checked immediately after a global reset event occurs. The self-checking will be finished in 1.25 ms. After the self-checking, if this bit is read out as **'1',** it indicates that the self-checking of the internal RAM fails. If this bit is read out as **'0',** it indicates that the internal RAM is ready to be accessed; but if this bit is read out as **'1'** again after another reset event, it indicates that there is something wrong with RAM.

0x00CA, System Status Register, SysSts

Bit		R/W	Default	Description
Bit7	PDN	R	0	Power-down interrupt flag bit. When input voltage on pin VDD33 is lower than Power-Down detection threshold, this bit is read out as 1. When the input is higher than Power-Down detection threshold, this bit is read out as 0.
Bit6	PDN_R	R	0	Power-down interrupt flag latch value. This bit is read as 1 when the system is powered down, ie when the level on the VDD33 pin is below Power-Down detection threshold. When the power-down event disappears, the flag bit will be read out as 1.
Bit[5:3]	RSTSRC	R	0	Read the Bit [5: 3] to determine the cause of the reset. Bit5 Bit4 Bit3 Description 0 0 1 A POR occurs. 0 1 1 A RX reset occurs. 0 1 0 Reserved. 1 0 0 A software reset occurs.
Bit2	CHKERR	R	0	Read this bit for the state of configuration verification. The read value is refreshed every 5ms. Read this bit to determine whether a parameter configuration self-checking error occurs. Add the content of the registers for calibration, metering control registers, analog control registers, and 1 reserved internal registers to the content of the checksum register to ensure that all the important configurations are in their desired states. If the sum is 0xFFFFFFFF, the verification passes, and this bit is read out as 0; otherwise, the verification fails, and this bit is read out as 1.
Bit1	PHSDONE	R	0	The flag bit for whether the phase measurement ends or not. 0: Not finished; 1: Finished.

0x00CA, System Status Register, SysSts				
Bit		R/W	Default	Description
Bit0	REF	R	0	Set this bit to high when the REF external capacitor starts to leak. Otherwise this bit is low. The read and write operations do not change the level of this bit.

Table 9-8 System Status Register (0x019D, SysStsClr, R/W)

0x019D, System Status Register, SysStsClr				
Bit		R/W	Default	Description
Bit[31:10]	Reserved	R/W	N/A	These values are indeterminate and meaningless.
Bit9	PHSDONE_CLR	R/W	0	The flag bit for whether the phase measurement ends or not. 0: Not finished; 1: Finished. It can be cleared.
Bit[8:7]	Reserved	R/W	N/A	These values are indeterminate and meaningless.
Bit6	PDN_CLR	R/W	0	Power-down interrupt flag bit. When input voltage on pin VDD33 is lower than Power-Down detection threshold, this bit is read out as 1. When the input is higher than Power-Down detection threshold, this bit is read out as 1. It can be cleared.
Bit[5:0]	Reserved	R/W	N/A	These values are indeterminate and meaningless.

9.6. Metering Control Registers

When power-on reset, RX reset or global software reset occurs, all metering control registers will be reset.

Table 9-9 Data Register (R/W)

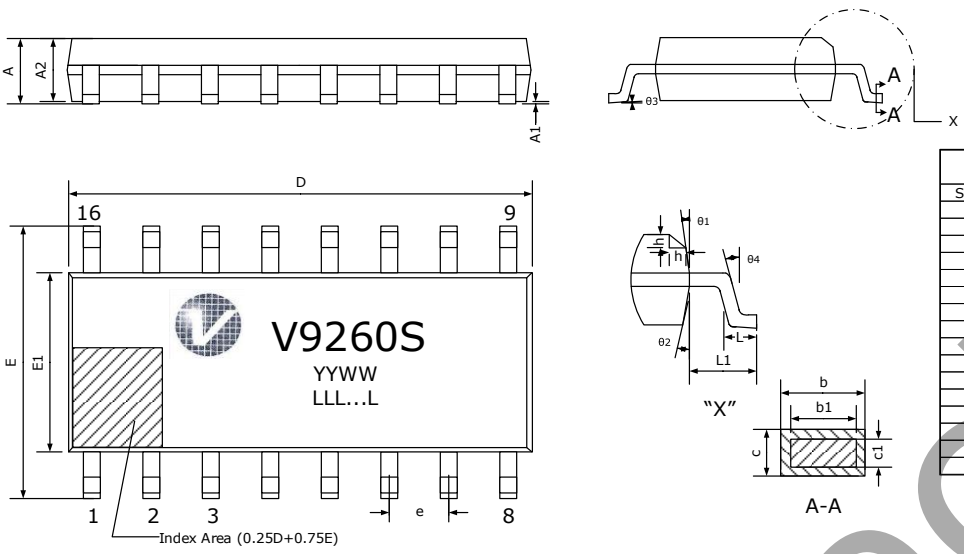
Address	Register		R/W	Data format	Default	Description
0x00CB	FREQINST	Instantaneous frequency value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, it will be updated every 20ms.
0x00CC	PAINST	A channel instantaneous active power value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 160ms and the settling time is 480ms.
0x00CD	QINST	instantaneous reactive power value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 160ms and the settling time is 480ms.
0x00CE	IAINST	A channel instantaneous current RMS	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 10ms and the settling time is 160ms.
0x00CF	UINST	Instantaneous voltage RMS	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 10ms and the settling time is 160ms.
0x00D0	PAAVG	A channel average active power value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 640ms and the settling time is 1280ms.
0x00D1	QAVG	Average reactive power value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 640ms and the settling time is 1280ms.
0x00D2	FREQAVG	Average frequency value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, it will be updated every 320ms.
0x00D3	IAAVG	A channel average current RMS	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value

Address	Register		R/W	Data format	Default	Description
						is 320ms and the settling time is 960ms.
0x00D4	UAVG	Average voltage RMS	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 320ms and the settling time is 960ms.
0x00D5	PBINST	B channel instantaneous active power value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 160ms and the settling time is 480ms.
0x00D6	IBINST	B channel instantaneous current RMS	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 10ms and the settling time is 160ms.
0x00D7	PBAVG	B channel average active power value	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 640ms and the settling time is 1280ms.
0x00D8	IBAVG	B channel average current RMS	R	32-bit 2's complement	0	When the energy metering clock frequency is 3.2768MHz, the update time for the register value is 320ms and the settling time is 960ms.
0x00D9	UDCINST	Voltage instantaneous DC component value	R	32-bit 2's complement		
0x00DA	IADCINST	A channel instantaneous DC component value	R	32-bit 2's complement		
0x00DB	IBDCINST	B channel instantaneous DC component value	R	32-bit 2's complement		
0x00DC	ZXDATREG	The previous sampling value of zero-crossing	R	32-bit 2's complement	0	
0x00DD	ZXDAT	The sampling value of	R	32-bit 2's	0x80000000	

Address	Register		R/W	Data format	Default	Description
		zero-crossing		complement		
0x00DE	PHDAT	Voltage phase data	R	32-bit 2's complement	1	
0x00E0	T8BAUD	The timing data of current baud rate communication under consecutive 8bit falling edge	R	32-bit 2's complement	0	This register needs to be involved in measuring the offset of the RC clock, and its value is used to compensate the frequency. Calculate the internal RC clock frequency according to the following equation: $frc = \mathrm{K}' \times \frac{\mathrm{T8BAUD}}{8}$ Where: frc: Internal high frequency RC clock actual frequency; T8BAUD: Value of the register (0x00E0); K': Actual baud rate known by host MCU Voltage frequency: $f = 0.00390625 \times \mathrm{K}' \times \frac{\mathrm{T8BAUD}}{\mathrm{FREQAVG}}$ Where: f: Actual voltage frequency T8BAUD: Value of the register (0x00E0)

Address	Register		R/W	Data format	Default	Description
						FREQAVG: Frequency average value per second register (0x00D2) K': Actual baud rate known by host MCU

10. Outline Dimensions



Dimensions (Unit: mm)			
Symbol	Min.	Nom.	Max.
A	1.40		1.73
A1	0.05		0.18
A2	1.35		1.55
E	5.84		6.24
E1	3.84		4.04
D	9.90		10.10
L	0.40		0.70
e		1.27TYP	
b	0.36		0.46
b1	0.36		0.46
c		0.2TYP	
c1		0.2TYP	
θ1		8°TYP	
θ2		8°TYP	
θ3		4°TYP	
θ4		15°TYP	

LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week