V85XXP

Datasheet

Specifications are subject to change without notice.

Revision History

Date	Version	Description
2020.06.22	V2.0	Initial release
2020.10.17	V2.1	Add LQFP100(V8500P)/LQFP80(V8530P)/LQFP64(V8510P)
2021.07.16	V2.2	Modify Table 1-10 ADC Characteristics, typical values of working time and sampling rate.
2022.01.04	V2.3	Modify ANA_REG4<2:0>=001；ANA_REG10 don't configured;
2022.02.17	V2.4	Add the description of VDCIN and VDCINHYST in Table 1-7. Modify V85XXP ADC clock source selection register in clock function block diagram;
2022.04.14	V2.5	Modify the description of RTC_ALARMCTL register; Modify X32KO and X32KI pin description; Delete RTC_ALARMTIME register;
2022.05.09	V2.6	Modify ANA_REGA Bit[6:0] set value;
2022.12.02	V2.7	Modify Equation 9-1;
2023.03.03	V2.8	Correct the SEG pin number corresponding to IOA4~IOA7; Add V8531P;

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General Description

The V85XXP series is a highly integrated 32-bit MCU which is suitable for multifunctional and Ultra-low-power IoT product. It is integrated with Cortex-M0 MCU, 512KB Flash, 64KB SRAM, UART/SPI/I^2C interface, LCD, WDT and RTC. The V85XXP series also supports kinds of low-power mode and RTC independent power-supply.

Features

- V85XXP working voltage:2.2V~5.5V
- Working current:
  - Normal mode:2.1mA@6.5536MHz
  - IDLE mode:0.5mA@6.5536MHz
  - Sleep mode (LCD active):12μA
  - RTC only mode:1.3μA
- Package:
  - LQFP100(V8503P)/ LQFP100(V8500P)
  - LQFP80(V8530P/V8531P)
  - LQFP64(V8510P)
- Operation Temperature:-40~+85°C
- Storage Temperature:-55~+150°C
- MCU
  - 32-bit Cortex-M0 with maximum 26.2144MHz operative speed.
  - Single instruction cycle for multiplier.
  - Standard 2-wires SWD debug interface.
  - Embedded 512KB FLASH with write protect and encryption, support both ISP and IAP.
  - 64K bytes SRAM with parity check, and data retention under the sleep mode.
  - 256 bytes SRAM with data retention under the deep-sleep mode.
  - Support real-time detection including FLASH checksum error, SRAM parity check error, memory address error or memory align error.
- Peripherals
  - Up to 6xUARTs with parity check.
    - Each serial channel can be coupled with IR carrier to process IR transmission.
    - Up to 2 ISO7816 controllers

  - Up to 3 SPI master/slave controllers.
  - Up to 1 I^2C master/slave controller.
  - 4x32-bit timers.
  - 4x16-bit PWM timers.
  - 4-channel DMA controller.
  - 128/192/256-bit AES CODEC.
  - ECC encrypt/decrypt accelerated engine.
  - Dual frame buffer LCD controller
    - ✓ 4COM/6COM/8COM
    - ✓ 1/3 or 1/4 bias.
    - ✓ Support multi types of scan frequency.
    - ✓ LCD voltage:the output voltage follows VDD.
  - Watchdog Timer(WDT) with programmable period.
  - Support multiple wake-up sources
  - Up to 86 GPIOs
  - Up to 16 GPIOs can be a wake-up source of external interrupt.
- Analog Controller (ANA)
  - 12 bits ADC with the highest 240K/S sample rate and up to 8 external inputs.
    - ✓ ADC supports random sample or autoatic random sample mode.
  - 2 comparators with single input or differential input.
  - Embedded 32KHz and 6.5MHz RC Oscillator.
  - Embedded 2 PLLs.
  - Support external 32.768KHz or 6.5536MHz crystal (optional).
  - Embedded 32.768KHz and 6.5536MHz monitoring circuit of crystal.
  - Each clock can be selected to a system clock.
  - Support digital clock divider, up to 1/256.
  - Support programmable low-voltage monitoring
  - Support power-on reset (POR) for AVCC and DVCC.
  - Support RTC power supply.
  - Support each input voltage monitor.
- RTC
  - Support RTC independent power supply.

- Support RTC calibration for 1ppm level.

V85XXP Product Series

Peripherals	V8503P	V8500P	V8530P	V8531P	V8510P
ADC external chan2nel	8	8	7	8	4
Tiny ADC channel	2	2	2	2	0
UART	6	6	6	6	5
ISO7816	2	2	2	2	2
SPI	3	3	3	3	3
I^2C	1	1	1	1	1
Comparator	2	2	2	2	1
GPIO	86	82	69	71	53
External IO interrupt and wake-up	16	16	15	16	15
32-bit timer	4	4	4	4	4
16-bit PWM timer	4	4	4	4	4
PWM output and capture input	4	4	4	4	4
DMA channel	4	4	4	4	4
LCD	76x4, 74x6, 72x8	76x4, 74x6, 72x8	63x4, 61x6, 59x8	65x4, 63x6, 61x8	49x4, 47x6, 45x8
FLASH	512KB	512KB	512KB	512KB	512KB
SRAM	64KB	64KB	64KB	64KB	64KB
Package Type	LQFP100	LQFP100	LQFP80	LQFP80	LQFP64

Statement

Hangzhou Vango Technologies reserves the right to correct or update the products, and related technical information involved in this manual. When using this manual, please obtain the newest information from our sales or log in to the company website *http://www.vangotech.com*.

1. Electrical Characteristics

1.1. Absolute Maximum Ratings

The maximum or minimum stress of the following listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1-1 Absolute Maximum Ratings

Symbol	Ratings	Min	Max	Unit
V_{VDD}-V_{SS}	External supply voltage	-0.3	+5.8	V
V_{IN}-V_{SS}	External signal input to GPIO pins.	-0.3	+5.8	V
S_{VDD}	IO power-on slope	5V/s	1V/μs	--
I_{INJ_PAD}	Single pin input injection current	-10	+10	mA
I_{INJ_SUM}	Sum of all input injected current	-50	+40	mA
T_W	Operation temperature	-40	+85	°C
T_S	Storage temperature	-55	+150	°C
T_J	Junction Temperature under bias	-40	+125	°C

1.2. General Operating Voltage

Table 1-2 Voltage Supply

Symbol	Parameter	Conditions (Whole Temperature Range)	Min	Typ	Max	Unit
$V_{IN,VDD}$	VDD input voltage		2.2	3.3/5	5.5	V
$V_{IN,BATRTC}$	BATRTC input voltage		2.2	3.3/5	5.5	V

1.3. Driving Characteristics

Table 1-3 Driving Conditions of Power pins

Symbol	Parameter	Conditions (Whole Temperature Range)	Min	Typ	Max	Unit
$I_{DRV,VDD}$	Driving Capability to VDD				40*[1]	mA
$I_{DRV,AVCC}$	Driving Capability to AVCC				30	mA
$I_{DRV,DVCC}$	Driving Capability to DVCC				35	mA

$I_{DRV,AVCCOUT}$	Driving Capability to AVCC_OUT*[2]				20*[2]	mA

*[1]:The driving current to VDD including the load of peripherals, AVCC, DVCC and AVCC_OUT.

*[2]:If there are AVCC, AVCC_OUT driving capability at the same time, the driving current cannot over 30mA.

1.4. Power switch conduction resistance

Table 1-4 Power switch conduction resistance

Symbol	Parameter	Conditions (Whole Temperature Range)		Min	Typ	Max	Unit
$R_{on,BATRTC2RTC}$	$R_{DS(ON)}$ between BATRTC and RTC	RTC is powered by BATRTC. IL=10μA	3.3V	325	500	675	ohm
			5V	250	400	475	ohm
$R_{on,VDD2RTC}$	$R_{DS(ON)}$ between VDD and RTC	RTC is powered by VDD. IL=10μA	3.3V	325	500	675	ohm
			5V	250	400	475	ohm
$R_{on,VDD2AVCC}$	When disable AVCCLDO, $R_{DS(ON)}$ between VDD and AVCC.	VDD=3.3V,IL*[1] <30mA		6.5	7.3	9.0	ohm

*[1]:Load current on AVCC.

1.5. Power Consumption

Table 1-5 Gerneal Conditions

Symbol	Parameter	Conditions (Measured on general temperature, AVCCLDO disable, VDD=3.3V (Except the special instruction))	Min	Typ	Max	Unit
I_{ACTIVE}	Active Current	System Clock:26.2144MHz		7014		μA
		System Clock:13.1072MHz		3852		
		System Clock:6.5536MHz		2118		
		System Clock:3.2768MHz		1175		
		System Clock:1.6384MHz		668		
		System Clock:819.2kHz		432		
		System Clock:409.6kHz		304		
		System Clock:204.8kHz		238		

		System Clock:32K RC (FLASH deep-standby)		20		
		System Clock:32K RC (FLASH ordinary)		24		
I_{IDLE}	IDLE Current	System Clock:26.2144MHz		1640		μA
		System Clock:13.1072MHz		900		
		System Clock:6.5536MHz		527		
		System Clock:3.2768MHz		343		
		System Clock:1.6384MHz		253		
		System Clock:819.2kHz		203		
		System Clock:409.6kHz		181		
		System Clock:204.8kHz		171		
		System Clock:32K RC		14		
I_{SLP1}	Sleep mode current when LCD is off.	RTCCLK no clock division		3.1 6.3@80 °C		μA
		RTCCLK 4 clock division		2.8		
I_{SLP2}	Sleep current when LCD is on.	RTCCLK no clock division		12		μA
		RTCCLK 4 clock division		11		
I_{DSLP}	Deep-sleep mode current, VDD=3.3V BATRTC=3.3V	RTCCLK no clock division		2.9		μA
		RTCCLK 4 clock division		2.6		
$I_{RTCONLY}$	RTC ONLY current, VDD=0V BATRTC=3.3V	RTCCLK no clock division		1.3		μA
		RTCCLK 4 clock division		1.1		

Table 1-6 The Power Consumption of Each Module

Module	Current (μA) (Measured on general temperature)	Status
CMP1/2	0.08	IT_CMP=00 (bias current=20nA)
	0.4	IT_CMP=01 (bias current=100nA)
	2	IT_CMP=1* (bias current=500nA)

BGP	108	
ADC	380	
TinyADC	0.7	
Tempsensor	80	
Input Buffer	60	
Ref Buffer	60	
LCD	5	Driving reisitance for LCD=600k
	9.9	Driving resistance for LCD=300k
	14.5	Driving resistance for LCD=200k
	19	Driving resistance for LCD=150k
32768 XTAL	0.6	
32K RC	0.2	
6.5M RC	80	
6.5M XTAL	120	
PLL_L	20	
PLL_H	40	
AVCCLDO	1	

1.6. Embedded Reset and Power Control Block Characteristics

Table 1-7 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions (Measured on general temperature)	Min	Typ	Max	Unit
t_{RST}	Reset debounce time			20		μs
VREF	Reference voltage (VREF)		1.222	1.3	1.352	V
V_{PORH}	PORH detect voltage (AVCCLDO)		1.955	2.08	2.2	V
V_{PORL}	PORL detect voltage (DVCCLDO)		1.222	1.3	1.352	V

V_{VDCIN}	VDCIN detect level	Rising edge			1.062	V
		Falling edge	0.868			V
$V_{VDCINHYST}$	VDCIN hysteresis	Hysteresis		100		mV
V_{AVCCLV}	Low voltage detect level for AVCC		2.35	2.5	2.6	V
$V_{VDDALRAM}$	Power detect voltage for VDD	V_{TH} configurable,V_{TH}=2.9V Reference voltage is VREF.	2.726	2.9	3.016	V
AVCC	AVCC voltage		3.2	3.3	3.4	V
V_{AVCC_Drop}	AVCC voltage drop	I_{OUT}=30mA			200	mV

Table 1-8 Hysteresis Voltage

Symbol	Parameter	Conditions (Whole Temperature Range)	Min	Typ	Max	Unit
V_{PORH_HTRES}	Hysteresis voltage detect for PORH		53.2	66.5	79.8	mV
V_{PORL_HTRES}	Hysteresis voltage detect for PORL		33.6	42.0	50.4	mV
V_{VDCIN_HTRES}	Hysteresis voltage detect for VDCIN		94/188	100/200	106/212	mV
V_{AVCCLV_HTRES}	Hysteresis voltage detect for AVCCLV		33.6	42.0	50.4	mV
$V_{VDDALRAM\_HTRES}$	Hysteresis voltage detect for VDD	$V_{TH\_VDDALARM}$ =4.5 V	114.0	142.5	171.0	mV
		$V_{TH\_VDDALARM}$ =4.2 V	106.4	133.0	159.6	mV
		$V_{TH\_VDDALARM}$ =3.9 V	98.8	123.5	148.2	mV
		$V_{TH\_VDDALARM}$ =3.6 V	91.2	114.0	136.8	mV
		$V_{TH\_VDDALARM}$ =3.2 V	81.1	101.4	121.6	mV
		$V_{TH\_VDDALARM}$ =2.9 V	73.5	91.9	110.2	mV
		$V_{TH\_VDDALARM}$ =2.6 V	65.9	82.4	98.8	mV
		$V_{TH\_VDDALARM}$ =2.3 V	58.3	72.9	87.4	mV

1.7. GPIO Characteristics

Table 1-9 GPIO Characteristics

Symbol	Parameter	V_{VDD}	Conditions(Whole Temperature Range)	Min	Max	Unit
V_{IH}	Input high voltage	5V		0.7*V_{VDD}		V
		3.3V		2		
V_{IL}	Input low voltage	5V			0.3*V_{VDD}	V
		3.3V				
V_{HSYS}	Schmitt trigger hysteresis	5V		0.1*V_{VDD}		V
		3.3V				
I_{IH}	Input high current	5V			+1	μA
		3.3V				
I_{IL}	Input low current	5V		-1		μA
		3.3V				
V_{OH}	Output high voltage	5V	Drive current 11.2mA	V_{VDD}-0.8	V_{VDD}	V
		3.3V	Drive current 5.6mA	2.4	V_{VDD}	V
V_{OL}	Output low voltage	5V	Drive current 11.2mA		0.5	V
		3.3V	Drive current 5.6mA		0.4	V
C_{IN}	Input capacitance	5V			10	pF
		3.3V				

1.8. ADC Characteristics

Table 1-10 ADC Characteristics

Symbol	Paramter	Conditions	Min	Typ	Max	Unit
Operation Voltage, Standards and Consumption						
BGPREF	BGP voltage		1.203	1.22	1.237	V
PSRR	Power supply rejection ratio (PSRR) for BGP			-55		dB
V_{ADC}	Operation voltage for ADC, powered by AVCC.		2.5	3.3	3.6	V
I_{ADC}	Operation current for ADC	ADCCLK=6.5 MHz		400		μA
Time parameters for ADC						
F_{mclk}	ADC operation clock			6.5		MHz
F_{samp}	ADC sampling rate			240		KHz

C_{ADC}	Internal sample and hold capacitance.			2.6		pF
T_{on}	ADC Power on time		5			T_{mclk}
T_{CAL}	ADC Calibration time			4096		T_{mclk}
Active Characteristics for ADC						
SNDR	Signal-noise Distortion Ratio	after calibration		70		dB
SFDR	Spurious Free Dynamic Range			87		dB
THD	Total Harmonic Destortion			-85		dB
Reactive Characteristics for ADC						
RES	Resolution	after calibration		12		bits
ED	Differential Non-linearity Error (DNL)		-1	0.7/+0.9	1	LSB
EL	Integral Nonlinearity Error (INL)		-2	±0.9	2	LSB
EO	Offset Error			-0.1		
EG	Gain Error			-1.5		
Refresh time for ADC						
(Avergae ADC data + skip ADC data) *(19+8)* ADC operative clock cycle						

1.9. Analog Comparator Characteristics

Table 1-11 Comparator Characteristics

Symbol	Parameter	Conditions (Room Temperature)	Min	Typ.	Max	Unit
V_{DDCMP}	Operation voltage of comparator (AVCC)		2.2	3.3	3.6	V
I_{CMP}	Operation current of comparator	Input bias current 20nA, input 50kHz square wave.		0.08		μA
		Input bias current 100nA, input 50kHz square wave.		0.4		μA
		Input bias current 500nA, input 50kHz square wave.		2		μA
td	Propagation delay (no filter)	Input bias current 20nA, input 50kHz square wave.		1.6		μs
		Input bias current 100nA, input 50kHz square wave.		0.63		μs
		Input bias current 500nA, input 50kHz square wave.		0.27		μs

V_{CMPIN}	Input voltage range for Comparator		0.8		VDD-0.3	V
V_{CMPREF}	Comparator Reference voltage	Reference voltage is VREF	1.222	1.3	1.352	V
		Reference voltage is BGPREF		1.22		V
V_{HTRES}	Comparator Hysteresis voltage		20.0	25.0	30.0	mV

1.10. Clock and PLL Characteristics

Table 1-12 Clock and PLL Characteristics

Symbol	Parameter	Conditions (Room Temperature)	Min	Typ.	Max	Unit
$V_{VDDPLLL}$	PLLL operation voltage PLLL (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLL}$	PLLL operation current			30		μA
$V_{VDDPLLH}$	PLLH operation voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLH}$	PLLH operation current			40		μA
V_{VDDRCL}	RCL operation voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDRCL}	RCL operation current			0.2		μA
f_{RCL}	RCL frequency		29.7	32	35.5	kHz
V_{VDDRCH}	RCH operation voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDRCH}	RCH operation current			45		μA
f_{RCH}	RCH frequency		6.357	6.5	6.75	MHz
V_{VDDXOH}	XOH operation voltage for (AVCC)		2.2	3.3	3.6	V
I_{VDDXOH}	XOH operation current			150		μA
f_{XOH}	XOH frequency			6.5536		MHz

1.11. FLASH and SRAM Characteristics

Table 1-13 FLASH and SRAM Characteristics

Symbol	Conditions	Min	Typ.	Max	Unit

Flash read access time(for a word)		38			ns
FLASH program time	-40~85°C	20000			time
FLASH data retention time	-40~85°C	20			year
FLASH byte program time		6		7.5	μs
FLASH page erase time (1024 bytes for one page)		4		5	ms
FLASH chip erase time		30		40	ms
FLASH active read current	26MHz access		2.5	3.5	mA
FLASH active program current				3.5	mA
FLASH active erase current				2	mA
FLASH standby current			80	150	μA
FLASH deep standby current			0.1	6	μA
Operation voltage for FLASH (DVCC)		1.35	1.5	1.65	V
SRAM data retention voltage (DVCC)		1.35	1.5	1.65	V
Operation temperature for SRAM		-40	+25	+85	°C

1.12. ESR Characteristics for Crystal Oscillator

Table 1-14 ESR Characteristics for Crystal Oscillator

Parameter	Conditions (Whole Temperature Range)	Min	Typ.	Max	Unit
ESR*[1] for 6.5536M crystal				100	Ω
ESR for 32.768K crystal				50	KΩ

*[1]: ESR (Equivalent Series Resistance)

1.13. Clock for Stabiliztion Time and Wakeup Time

Table 1-15 Clock for Stabilization Time and Wakeup Time

Parameter	Conditions (Whole Temperature Range)	Min	Typ.	Max	Unit
PLLL lock time				1	ms
PLLH lock time				15	μs
RCL output stabilization time				200	μs
RCH output stabilization time				5	μs
BGP output stabilization time				100	μs
The sleep mode wake-up time when RCH is the system clock			18.4		μs
The sleep mode wake-up time when PLLL is the system clock			1.03		ms
The sleep mode wake-up time when PLLH is the system clock			22.8		μs
IDLE interrupt response time when RCH is the system clock			6		μs
IDLE interrupt response time when PLLL is the system clock			1.6		μs
IDLE interrupt response time when PLLH is the system clock			1.6		μs

1.14. Convertion Time to TinyADC

Table 1-16 Convertion Time to TinyADC

Parameter	Conditions	Min	Typ.	Max	Unit
TinyADC convertion time			40		μs

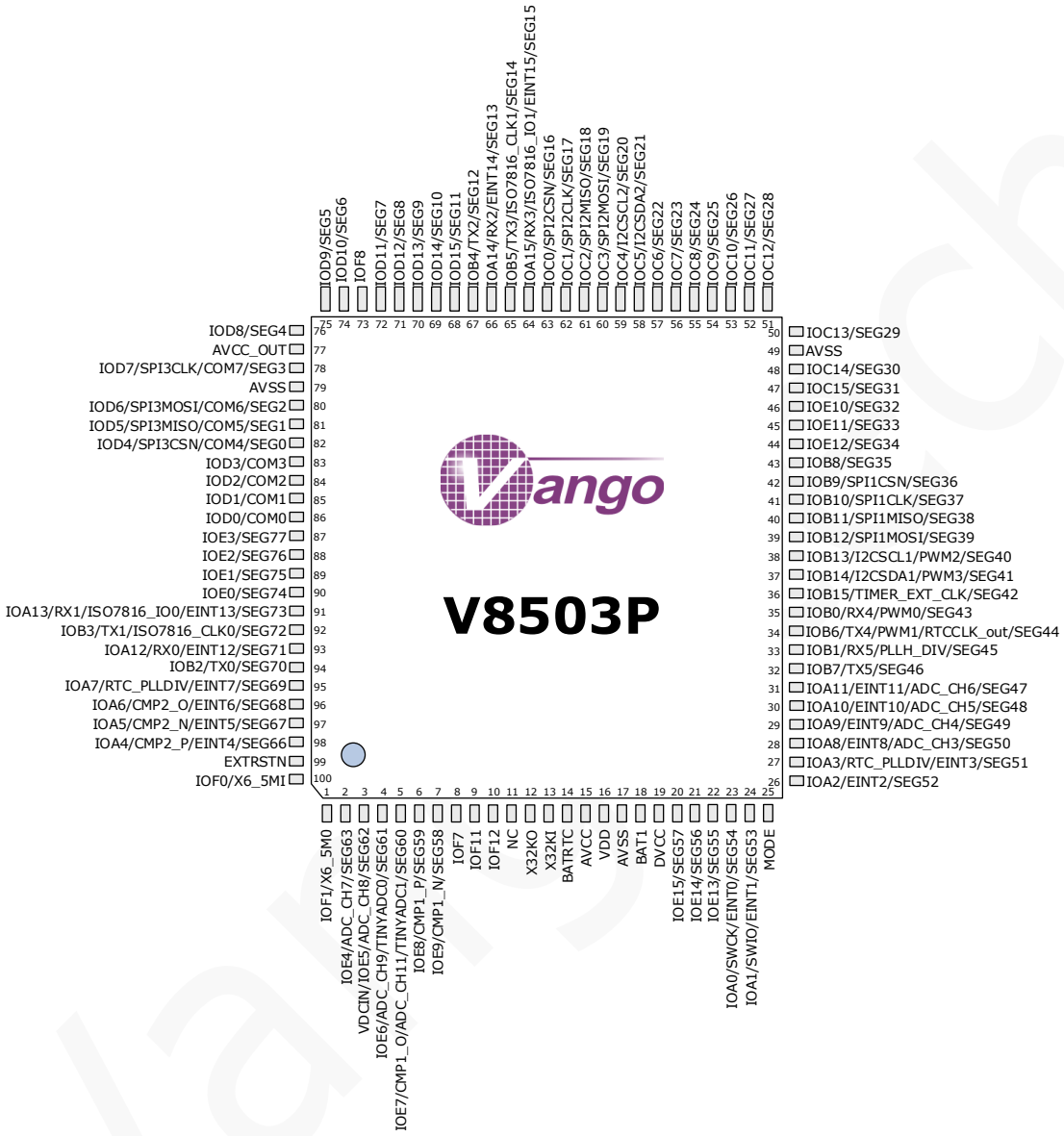
1.15. Reliability Analysis Results

Table 1-17 Reliability Analysis Results

Item	Regulation	Max
HBM	Mil-Std-883J Method 3015.9	±4000V
CDM	JS-002-2018	±2000V
LATCH-UP	JEDEC EIA/JESD78E	±200mA

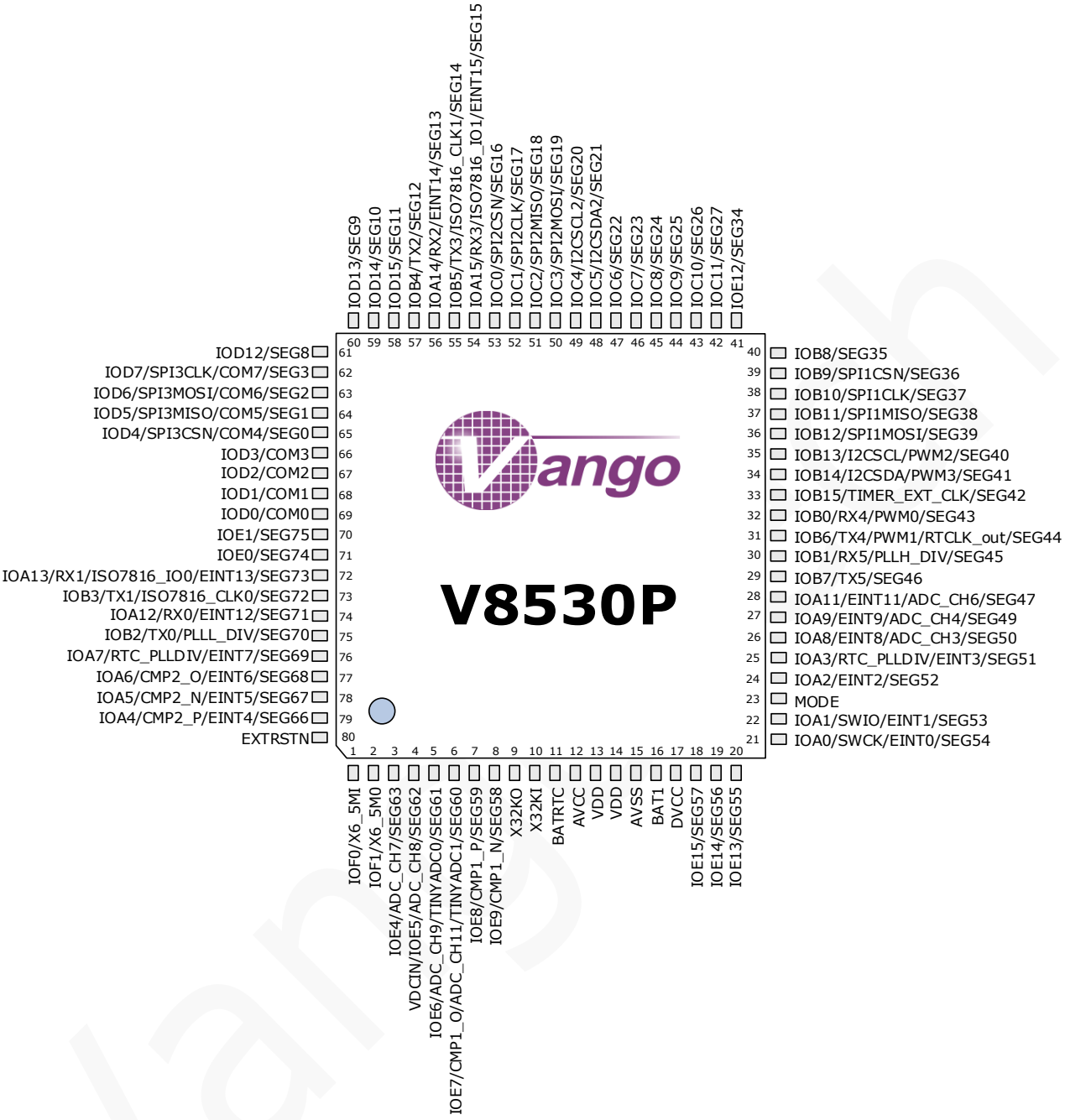
2. Pin Assignments

2.1 V8503P Pin Assignments



2.2 V8500P Pin Assignments

2.3 V8530P Pin Assignments



2.4 V8531P Pin Assignments

2.5 V8510P Pin Assignments

2.6 V85XXP Pins Description

Table 2-1 V85XXP Pins Description

No.	Pin No.					Pin Name	Type	Contents
	V8503P	V8500P	V8530P	V8510P	V8531P			
1	1	2	2		2	IOF1	I/O	Default:IOF1 Function 1:6.5536M crystal output
2	2	3	3		3	IOE4	I/O	Default:IOE4 Function 1:ADC_CH7 input Function 2:SEG63
3	3	4	4	2	4	IOE5	I/O	Default:VDCIN input Function 1:ADC_CH8 input Function 2:IOE5 Function 3:SEG62
4	4	5	5		5	IOE6	I/O	Default:IOE6 Function 1:ADC_CH9 input and TinyADC channel input Function 2:SEG61
5	5	6	6		6	IOE7	I/O	Default:IOE7 Function 1:Comparator 1 output Function 2:ADC_CH11 input and TinyADC channel 1 input Function 3:SEG60
6	6	7	7	3	7	IOE8	I/O	Default:IOE8 Function 1:compator 1 P terminal input Function 2:SEG59
7	7	8	8		8	IOE9	I/O	Default:IOE9 Function 1:comparator 1 N terminal input Function 2:SEG58

8	8					IOF7	I/O	Default:IOF7
9	9					IOF11	I/O	Default:IOF11
10	10					IOF12	I/O	Default:IOF12
11	11	9				NC		
12	12	10	9	4	9	X32KO	O	32768Hz crystal output pin, **it needs to add capacitor to ground**.
13	13	11	10	5	10	X32KI	I	32768Hz crystal output pin, **it needs to add capacitor to ground**.
14	14	12	11	6	11	BATRTC	P	RTC battery input pin.
15	15	13	12	7	12	AVCC	O/P	Internal analog power output, user should connect a 0.1uF and a 10uF decoupling capacitor to this pin.
16	16	14	13	8	13	VDD	P	Main power input pin. User should connect a 0.1uF decoupling capacitor to this pin.
17		15	14	9		VDD	P	Main power input pin. User should connect a 0.1uF decoupling capacitor to this pin.
18	17	16	15	10	14	AVSS	G	Analog ground.
19	18	17	16	11		BAT1	P	BAT1, battery detection input pin. In V85XXP series chip compatible applications, bat1 is not connected to battery and should be connected directly to VDD.
20		18				AVCC_OUT	O	Default:high resistance Function: AVCC voltage output pin, this level is consistent with the AVCC pin. User can use it to drive the small power modules.
21	19	19	17	12	15	DVCC	O/P	The internal digital power output pin, user should connect a 0.1uF and a 10uF decoupling capacitor to this pin.
22	20	20	18	13	16	IOE15	I/O	Default:IOE15 Function 2:SEG57
23	21	21	19	14	17	IOE14	I/O	Default:IOE14 Function 2:SEG56
24	22	22	20	15	18	IOE13	I/O	Default:IOE13 Function 2:SEG55
25	23	23	21	16	19	IOA0	I/O	Deafult:IOA0(MODE=1),SWCK(MODE=0)

								Function 1:EINT0 Function 2:SEG54
26	24	24	22	17	20	IOA1	I/O	Default:IOA1(MODE=1),SWIO(MODE=0) Function 1:EINT1 Function 2:SEG53
27	25	25	23	18	21	MODE	I	Debug mode or non-debug mode selection. 0: Debug mode. 1: Non-debugging mode. This pin should be pulled up by VDD, and the status of the IO should not change during normal or debugging operations.
28	26	26	24	19	22	IOA2	I/O	Default:IOA2 Function 1:EINT2 Function 2:SEG52
29	27	27	25	20	23	IOA3	I/O	Default:IOA3 Function 1:second pluse output (RTC_PLLDIV output) Function 2:EINT3 Function 3:SEG51
30	28	28	26	21	24	IOA8	I/O	Default:IOA8 Function 1:EINT8 Function 2:ADC_CH3 input Function 3:SEG50
31	29	29	27	22	25	IOA9	I/O	Default:IOA9 Function 1:EINT9 Function 2:ADC_CH4 input Function 3:SEG49
32	30	30		23	26	IOA10	I/O	Default:IOA10 Function 1:EINT10 Function 2:ADC_CH5 input

								Function 3:SEG48
33	31	31	28		27	IOA11	I/O	Default:IOA11 Function 1:EINT11 Function 2:ADC_CH6 input Function 3:SEG47
34	32	32	29		28	IOB7	I/O	Default:IOB7 Function 1:UART5_TX Function 2:SEG46
35	33	33	30	24	29	IOB1	I/O	Default:IOB1 Function 1:UART5_RX Function 2:PLLH divider output Function 3:SEG45
36	34	34	31	25	30	IOB6	I/O	Default:IOB6 Function 1:UART4_TX Function 2:PWM output or capture input 1 Function 3:RTCCLK output Function 4:SEG44
37	35	35	32	26	31	IOB0	I/O	Default:IOB0 Function 1:UART4_RX Function 2:PWM output or capture input 0 Function 3:SEG43
38	36	36	33	27	32	IOB15	I/O	Default:IOB15 Function 1:Timer external output input Function 2:SEG42
39	37	37	34	28	33	IOB14	I/O	Default:IOB14 Function 1:I2CSDA1 Function 2:PWM output or capture input 3 Function 3:SEG41

40	38	38	35	29	34	IOB13	I/O	Default:IOB13 Function 1:I2CSCL1 Function 2:PWM output or capture input 2 Function 3:SEG40
41	39	39	36	30	35	IOB12	I/O	Default:IOB12 Function 1:SPI1MOSI Function 2:SEG39
42	40	40	37	31	36	IOB11	I/O	Default:IOB11 Function 1:SPI1MISO Function 2:SEG38
43		41				AVSS	G	Analog ground
44	41	42	38	32	37	IOB10	I/O	Default:IOB10 Function 1:SPI1CLK Function 2:SEG37
45	42	43	39	33	38	IOB9	I/O	Default:IOB9 Function 1:SPI1CSN Function 2:SEG36
46	43	44	40	34	39	IOB8	I/O	Default:IOB8 Function 1:SEG35
47	44	45	41		40	IOE12	I/O	Default:IOE12 Function 1:SEG34
48	45	46			41	IOE11	I/O	Default:IOE11 Function 1:SEG33
49	46	47				IOE10	I/O	Default:IOE10 Function 1:SEG32
50	47	48				IOC15	I/O	Default:IOC15 Function 1:SEG31
51	48	49				IOC14	I/O	Default:IOC14

								Function 1:SEG30
52	49					AVSS	G	Analog ground
53	50	50				IOC13	I/O	Default:IOC13 Function 1:SEG29
54	51	51				IOC12	I/O	Default:IOC12 Function 1:SEG28
55	52	52	42		42	IOC11	I/O	Default:IOC11 Function 1:SEG27
56	53	53	43		43	IOC10	I/O	Default:IOC10 Function 1:SEG26
57	54	54	44		44	IOC9	I/O	Default:IOC9 Function 1:SEG25
58	55	55	45		45	IOC8	I/O	Default:IOC8 Function 1:SEG24
59	56	56	46		46	IOC7	I/O	Default:IOC7 Function 1:SEG23
60	57	57	47		47	IOC6	I/O	Default:IOC6 Function 1:SEG22
61	58	58	48	35	48	IOC5	I/O	Default:IOC5 Function 1:I2CSDA2 Function 2:SEG21
62		59				NC		
63	59	60	49	36	49	IOC4	I/O	Default:IOC4 Function 1:I2CSCL2 Functio 2:SEG20
64	60	61	50	37	50	IOC3	I/O	Default:IOC3 Function 1:SPI2MOSI Function 2:SEG19

65	61	62	51	38	51	IOC2	I/O	Default:IOC2 Function 1:SPI2MISO Function 2:SEG18
66	62	63	52	39	52	IOC1	I/O	Default:IOC1 Function 1:SPI2CLK Function 2:SEG17
67	63	64	53	40	53	IOC0	I/O	Default:IOC0 Function 1:SPI2CSN Function 2:SEG16
68	64	65	54	41	54	IOA15	I/O	Default:IOA15 Function 1:UART3_RX Function 2:ISO7816IO1 Function 3:EINT15 Function 4:SEG15
69	65	66	55	42	55	IOB5	I/O	Default:IOB5 Function 1:UART3_TX Function 2:ISO7816CLK1 Function 3:SEG14
70		67				AVSS	G	Analog ground
71	66	68	56	43	56	IOA14	I/O	Default:IOA14 Function 1:UART2_RX Function 2:EINT14 Function 3:SEG13
72	67	69	57	44	57	IOB4	I/O	Default:IOB4 Function 1:UART2_TX Function 2:SEG12
73	68	70	58	45	58	IOD15	I/O	Default:IOD15 Function 1:SEG11

74	69	71	59	46	59	IOD14	I/O	Default:IOD14 Function 1:SEG10
75	70	72	60	47	60	IOD13	I/O	Default:IOD13 Function 1:SEG9
76	71	73	61	48	61	IOD12	I/O	Default:IOD12 Function 1:SEG8
77	72	74				IOD11	I/O	Default:IOD11 Function 1:SEG7
78		75				VDDCAP	P	Main power supply decoupling pin, an external 0.1uF capacitor is recommended.
79	73					IOF8	I/O	Default:IOF8
80	74	76				IOD10	I/O	Default:IOD10 Function 1:SEG6
81	75	77				IOD9	I/O	Default:IOD9 Function 1:SEG5
82	76	78				IOD8	I/O	Default:IOD8 Function 1:SEG4
83						AVCC_OUT	P	Default:AVCC_OUT
84	78	79	62	49	62	IOD7	I/O	Default:IOD7 Function 1:COM7/SEG3 Function 2:SPI3CLK
85	79					AVSS	G	Analog ground
86	80	80	63	50	63	IOD6	I/O	Default:IOD6 Function 1:COM6/SEG2 Function 2:SPI3MOSI
87	81	81	64	51	64	IOD5	I/O	Default:IOD5 Function 1:COM5/SEG1 Function 2:SPI3MISO
88	82	82	65	52	65	IOD4	I/O	Default:IOD4

								Function 1:COM4/SEG0 Function 2:SPI3CSN
89	83	83	66	53	66	IOD3	I/O	Default:IOD3 Function 1:COM3
90	84	84	67	54	67	IOD2	I/O	Default:IOD2 Function 1:COM2
91	85	85	68	55	68	IOD1	I/O	Default:IOD1 Function 1:COM1
92	86	86	69	56	69	IOD0	I/O	Default:IOD0 Function 1:COM0
93	87	87				IOE3	I/O	Default:IOE3 Function 1:SEG77
94		88				NC		
95	88	89				IOE2	I/O	Default:IOE2 Function 1:SEG76
96	89	90	70		70	IOE1	I/O	Default:IOE1 Function 1:SEG75
97	90	91	71		71	IOE0	I/O	Default:IOE0 Function 1:SEG74
98	91	92	72	57	72	IOA13	I/O	Default:IOA13 Function 1:UART1_RX Function 2:ISO7816IO0 Function 3:EINT13 Function 4:SEG73
99	92	93	73	58	73	IOB3	I/O	Default:IOB3 Function 1:UART1_TX Function 2:ISO7816CLK0 Function 3:SEG72

100	93	94	74	59	74	IOA12	I/O	Default:IOA12 Function 1:UART0_RX Function 2:EINT12 Function 3:SEG71
101	94	95	75	60	75	IOB2	I/O	Default:IOB2 Function 1:UART0_TX Function 2:SEG70
102	95	96	76	61	76	IOA7	I/O	Default:IOA7 Function 1:second pulse output (RTC_PLLDIV output) Function 2:EINT7 Function 3:SEG69
103	96	97	77	62	77	IOA6	I/O	Default:IOA6 Function 1:comparator 2 output Function 2:EINT6 Function 3:SEG68
104	97	98	78	63	78	IOA5	I/O	Default:IOA5 Function 1:comparator 2 N terminal input Function 2:EINT5 Function 3:SEG67
105	98	99	79	64	79	IOA4	I/O	Default:IOA4 Function 1:comparator 2 P terminal input Function 2:EINT4 Function 3:SEG66
106	99	100	80	1	80	EXTRSTN	I	External reset pin, active low level, 510K ohm resistor and 0.1uF capacitor are recommended for RC filter circuit.
107	100	1	1		1	IOF0	I/O	Default:IOF0 Function 1:6.5536M crystal input

3. Functional Block Diagram

3.1 Functional Block Diagram

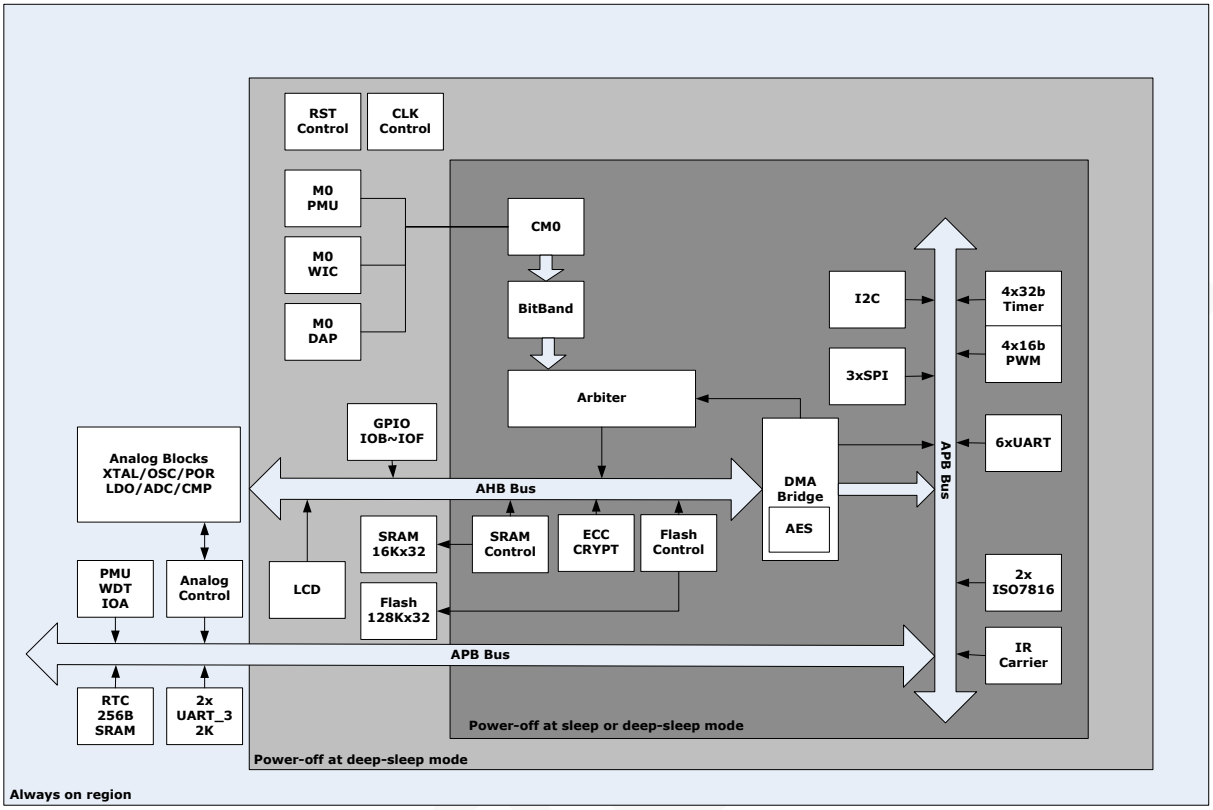


Figure 3-1 V85XXP Functional Block Diagram

3.2 Power System Block Diagram

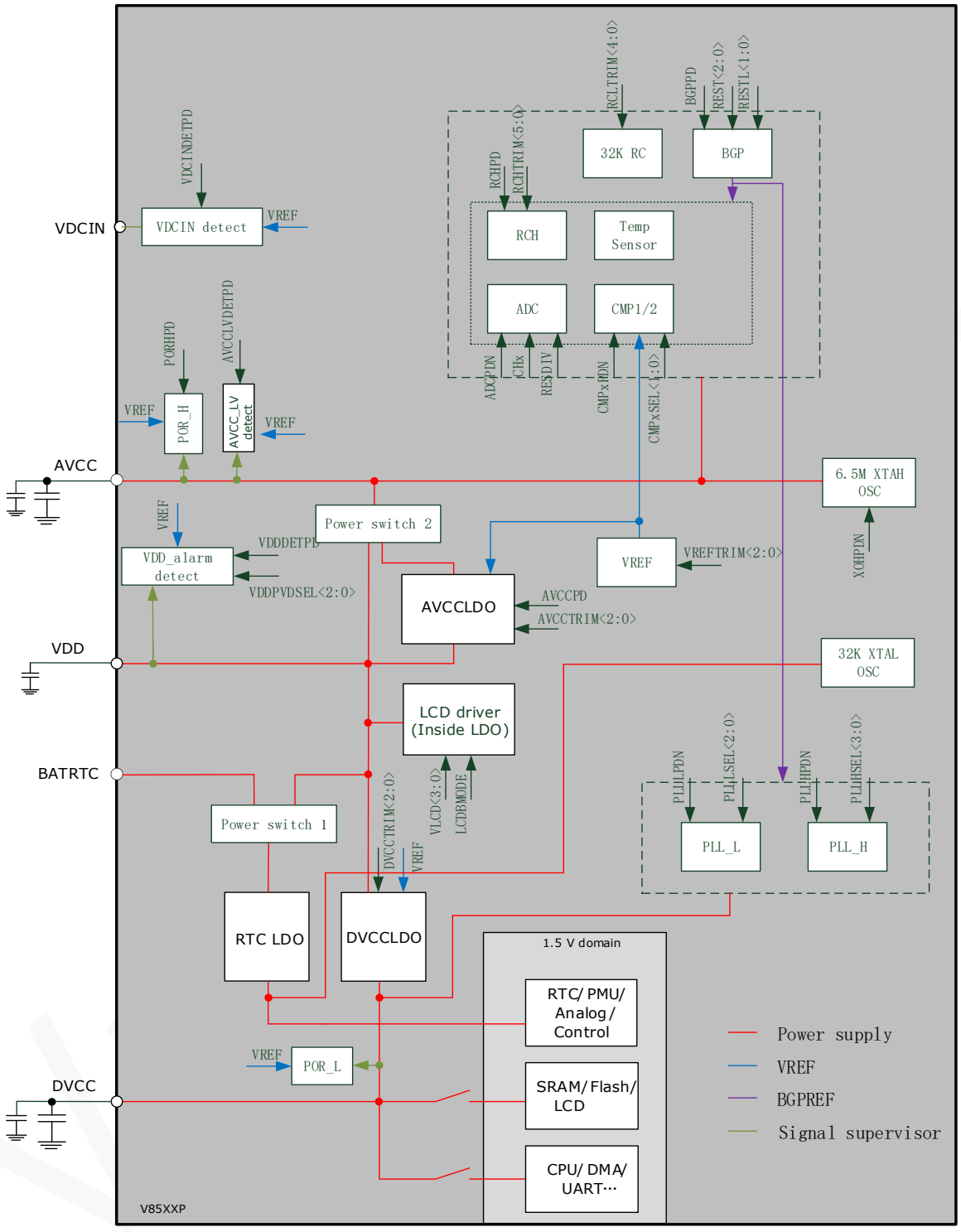


Figure 3-2 V85XXP Power System Block Diagram

3.3 Clock Block Diagram

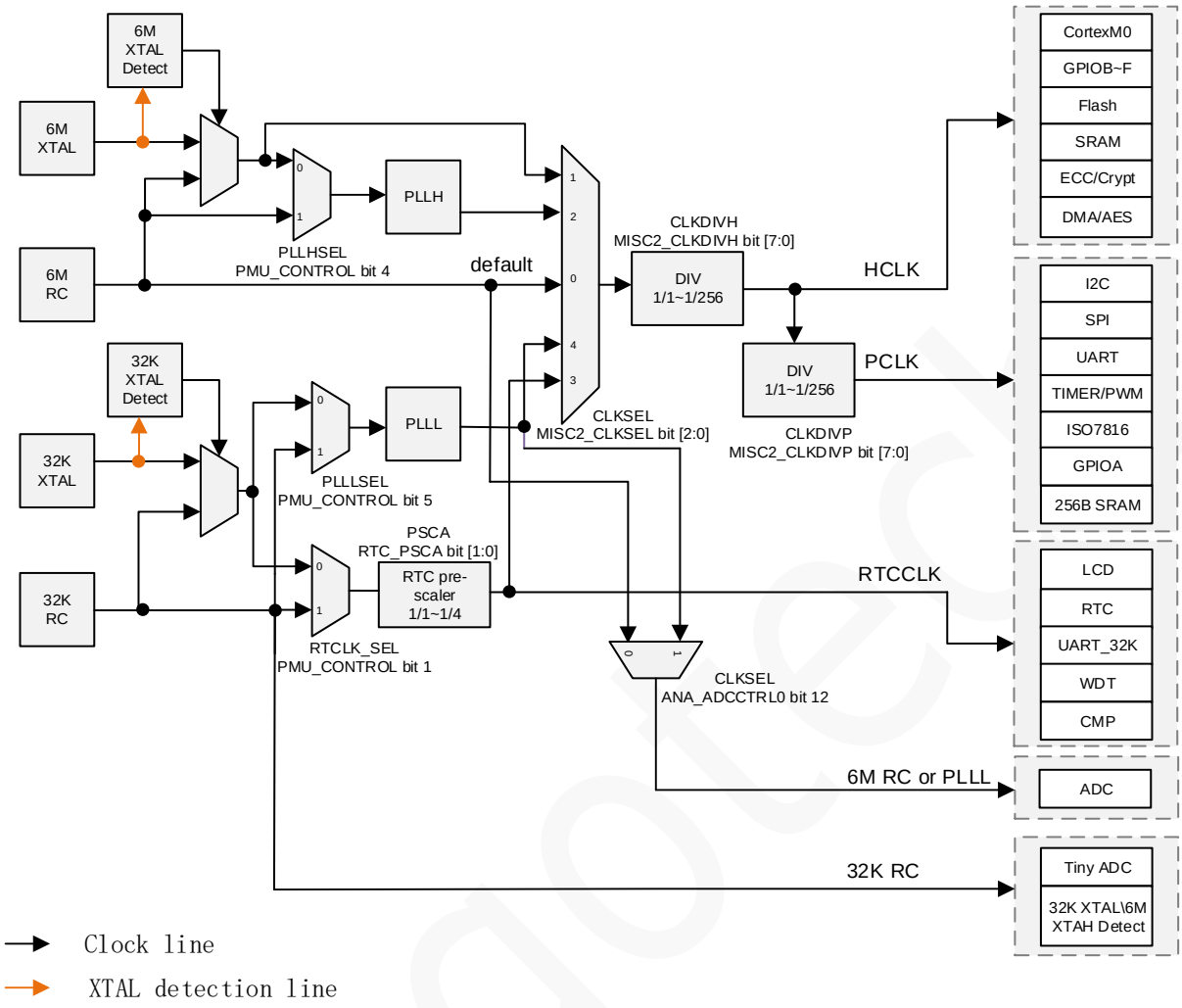


Figure 3-3 V85XXP Clock Block Diagram

4. Memory Maps

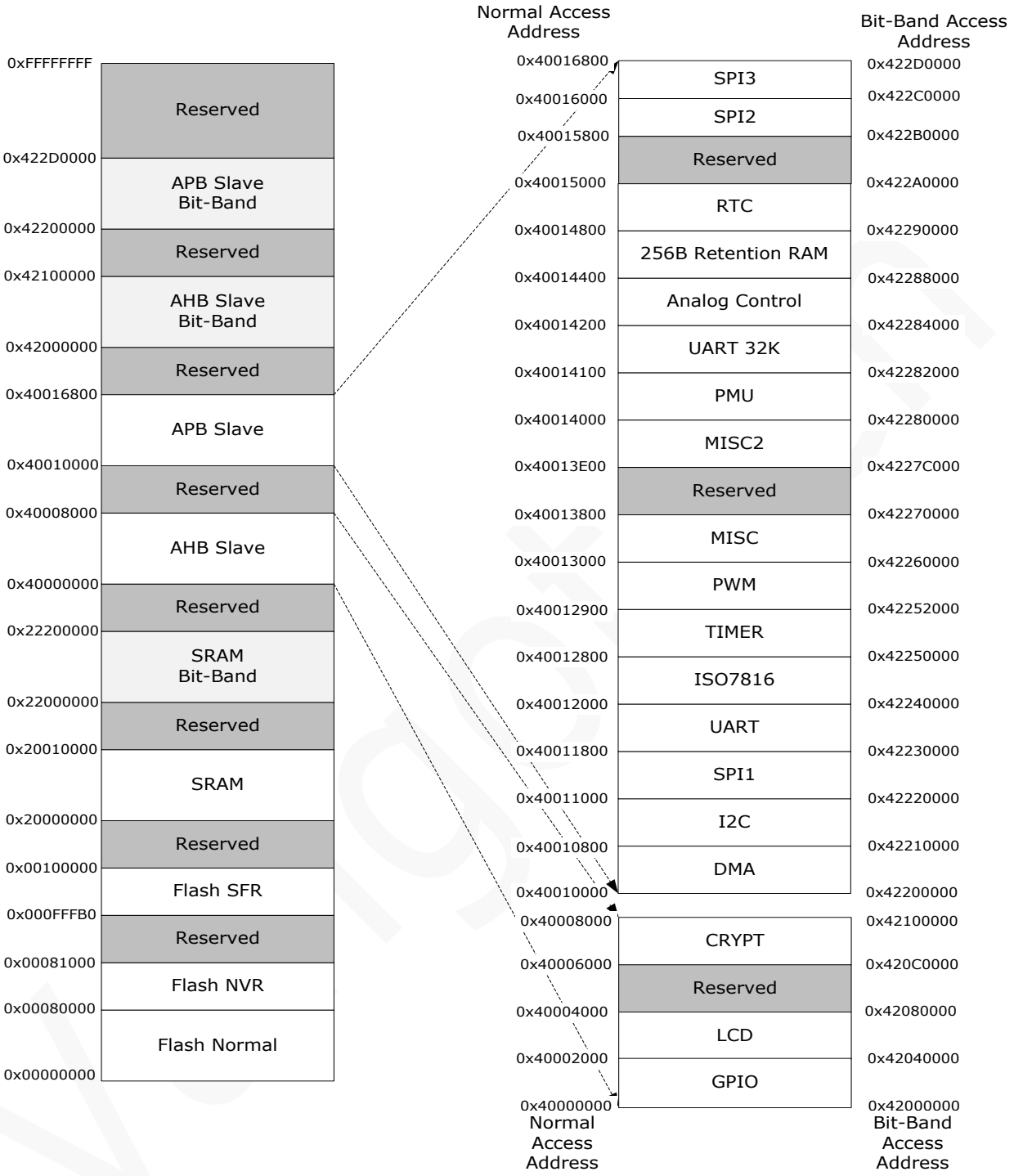


Figure 4-1 V85XXP Memory Maps

The bit-band region can only be accessed by Cortex-M0. The DMA controller can't access these regions. For others, they can be accessed by both Cortex-M0 and DMA controller.

4.1 Register Address

4.1.1 PMU Register Address

Table 4-1 PMU Register Address (PMU Base Address:0x40014000)

Name	Type	Address	Description	Default
PMU_DSLEEPEN	R/W	0x0000	PMU deep sleep enable register	0x00000000
PMU_DSLEEPPASS	R/W	0x0004	PMU deep sleep password register	0x00000000
PMU_CONTROL	R/W	0x0008	PMU control register	0x0000
PMU_STS	R/C	0x000C	PMU status register	0x0000074
PMU_IOAOEN	R/W	0x0010	IOA output enable register	0xFFFF
PMU_IOAIE	R/W	0x0014	IOA input enable register	0xFFFF
PMU_IOADAT	R/W	0x0018	IOA ouput data register	0x0000
PMU_IOAATT	R/W	0x001C	IOA attribute register	0x0000
PMU_IOAWKUEN	R/W	0x0020	IOA wake-up enable register	0x00000000
PMU_IOASTS	R	0x0024	IOA input status register	--
PMU_IOAINT	R/C	0x0028	IOa interrupt status register	0x0000
PMU_IOASEL	R/W	0x0038	IOA special function select register	0x0000
PMU_WDTPASS	R/W	0x0040	Watchdog timer unlocked register	0x00000000
PMU_WDTEN	R/W	0x0044	Watchdog timer enable register	0x1
PMU_WDTCLR	R/C	0x0048	Watchdog timer clear register	0x0000
PMU_IOANODEG	R/W	0x0050	IOA debounce control register	0x0000

Table 4-2 PMU Register Address (PMU Retention RAM Base Address:0x40014400)

Name	Type	Address	Description	Default
PMU_RAM0	R/W	0x0000	PMU 32 bits Retention RAM0	--
PMU_RAM1	R/W	0x0004	PMU 32 bits Retention RAM1	--
PMU_RAM2	R/W	0x0008	PMU 32 bits Retention RAM2	--
…	…	…	…	…
PMU_RAM63	R/W	0x00FC	PMU 32 bits Retention RAM63	--

4.1.2 ANA Register Address

Table 4-3 ANA Register Address (ANA Base Address:0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00
ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG4	R/W	0x0010	Analog register 4	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00
ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REG9	R/W	0x0024	Analog register 9	0x00
ANA_REGA	R/W	0x0028	Analog register 10	0x00
ANA_REGB	R/W	0x002C	Analog register 11	From FLASH, user cannot modify it.
ANA_REGC	R/W	0x0030	Analog register 12	From FLASH, user cannot modify it.
ANA_REGD	R/W	0x0034	Analog register 13	From FLASH, user cannot modify it.
ANA_REGE	R/W	0x0038	Analog register 14	From FLASH, user cannot modify it.
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_REG10	R/W	0x0040	Analog register 16	From FLASH
ANA_REG11	W	0x0044	Analog register 17	--
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_ADCSTATE	R	0x005C	ADC status register	--
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL0	R/W	0x0068	ADC control register 0	0x00000000

ANA_CMPCTL	R/W	0x006C	Comparator control register	0x00000000
ANA_ADCDATA0	R	0x0070	ADC Channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC Channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC Channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC Channel 3 data register channel 3	--
ANA_ADCDATA4	R	0x0080	ADC Channel 4 data register channel 4	--
ANA_ADCDATA5	R	0x0084	ADC Channel 5 data register	--
ANA_ADCDATA6	R	0x0088	ADC Channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC Channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC Channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC Channel 9 data register	--
ANA_ADCDATA10	R	0x0098	ADC Channel 10 data register	--
ANA_ADCDATA11	R	0x009C	ADC Channel 11 data register	--
ANA_ADCDATA12	R	0x00A0	ADC Channel 12 data register	--
ANA_ADCDATA13	R	0x00A4	ADC Channel 13 data register	--
ANA_ADCDATA14	R	0x00A8	ADC Channel 14 ADC data register	--
ANA_ADCDATA15	R	0x00AC	ADC Channel 15 data register	--

ANA_CMPCNT1	R/C	0x00B0	Comparator 1 counter register	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter register	0x00000000
ANA_MISC	R/W	0x00B8	Analog misc control register	0x00
ANA_ADCDOS	R	0x00C0	DOS register for ADC auto-calibration	0
ANA_ADCDCPN	R	0x00CC	DCPN register for ADC auto-calibration	0
ANA_ADCDCNM0	R	0x00D8	ADC DCNM0 register for auto-calibration	0
ANA_ADCDATADMA	R/W	0x00E0	DMA data source from ADC	0x0000
ANA_CMPTHR	R/W	0x00E4	Comparator 1/ comparator 2 threshold register	0x0000
ANA_ADCCTRL1	R/W	0x00E8	ADC control register 1	0x00000000
ANA_ADCCTRL2	R/W	0x00EC	ADC control register 2	0x00000000
ANA_ADCDATATHD1_0	R/W	0x00F4	ADC threshold control register 0	0x00000000
ANA_ADCDATATHD3_2	R/W	0x00F8	ADC threshold control register 1	0x00000000
ANA_ADCDATATHD_CH	R/W	0x00FC	ADC threshold status register	0x00000000

4.1.3 RTC Register Address

Table 4-4 RTC Register Address (RTC Base Address:0x40014800)

Name	Type	Address	Description	Default	Write Protect	Read Protect
RTC_SEC	R/W	0x0000	RTC second register	--	√	√
RTC_MIN	R/W	0x0004	RTC minute register	--	√	√
RTC_HOUR	R/W	0x0008	RTC hour register	--	√	√
RTC_DAY	R/W	0x000C	RTC day register	--	√	√

RTC_WEEK	R/W	0x0010	RTC weekday register	--	√	√
RTC_MON	R/W	0x0014	RTC month register	--	√	√
RTC_YEAR	R/W	0x0018	RTC year register	--	√	√
RTC_TIME	R/W	0x001C	RTC millisecond register	--	√	√
RTC_WKUSEC	R/W	0x0020	RTC wake-up second register	0x00	√	
RTC_WKUMIN	R/W	0x0024	RTC wake-up minute register	0x00	√	
RTC_WKUHOUR	R/W	0x0028	RTC wake-up hour register	0x00	√	
RTC_WKUCNT	R/W	0x002C	RTC wake-up counter register	0x0000000	√	
RTC_CAL	R/W	0x0030	RTC calibration register	--	√	
RTC_DIV	R/W	0x0034	RTC_PLLDIV divider register	0x0000000		
RTC_CTL	R/W	0x0038	RTC_PLLDIV divider control register	0x0		
RTC_ITV	R/W	0x003C	RTC ITV wake-up register	0x0	√	
RTC_SITV	R/W	0x0040	RTC SITV wake-up register	0x00	√	
RTC_PWD	R/W	0x0044	RTC passwords control register	0x00000000		
RTC_CE	R/W	0x0048	RTC control register for write enable	0x0		
RTC_LOAD	R/W	0x004C	RTC control register for read enable	--		
RTC_INTSTS	R/W	0x0050	RTC interrupt status control register	0x000		
RTC_INTEN	R/W	0x0054	RTC interrupt enable control register	0x000		
RTC_PSCA	R/W	0x0058	RTC clock prescaler control register	0x0	√	
RTC_ACTI	R/W	0x0084	Crystal the vertex temperature register	0x1800	√	
RTC_ACF200	R/W	0x0088	RTC 200* frequency register	0x640000	√	
RTC_ACP0	R/W	0x0090	RTC Parameter 0 register	0x0000	√	
RTC_ACP1	R/W	0x0094	RTC Parameter 1 register	0x0000	√	
RTC_ACP2	R/W	0x0098	RTC Parameter 2 register	0x0000	√	
RTC_ACP3	R	0x009C	RTC Parameter 3 register	0x0000		

RTC_ACP4	R/W	0x00A0	RTC Parameter 4 register	0x0000	√	
RTC_ACP5	R/W	0x00A4	RTC Parameter 5 register	0x0000	√	
RTC_ACP6	R/W	0x00A8	RTC Parameter 6 register	0x0000	√	
RTC_ACP7	R/W	0x00AC	RTC Parameter 7 register	0x0000	√	
RTC_ACK0	R/W	0x00B0	RTC Parameter k0 register	0x0000	√	
RTC_ACK1	R/W	0x00B4	RTC Parameter k1 register	0x0000	√	
RTC_ACK2	R/W	0x00B8	RTC Parameter k2 register	0x0000	√	
RTC_ACK3	R/W	0x00BC	RTC Parameter k3 register	0x0000	√	
RTC_ACK4	R/W	0x00C0	RTC Parameter k4 register	0x0000	√	
RTC_WKUCNTR	R	0x00CC	RTC wake-up counter register	0x000000		
RTC_ACKTEMP	R/W	0x00D0	RTC temperature section control register for K-factor	0x3C2800EC	√	
RTC_ALARMSEC	R/W	0x00D8	RTC second alarm register	0x0000	√	
RTC_ALARMMIN	R/W	0x00DC	RTC minute alarm register	0x0000	√	
RTC_ALARMHOUR	R/W	0x00E0	RTC hour alarm register	0x0000	√	
RTC_ALARMCTL	R/W	0x00E4	RTC alarm control register	0x0000	√	
RTC_ADCUCALK	R/W	0x00E8	ADC Ucal K-factor register	0x546A546A	√	
RTC_ADCMACTL	R/W	0x00EC	ADC average control register	0x70000000	√	
RTC_ADCDTCTL	R/W	0x00F0	ADC data control register	0x80000000	√	

4.1.4 FLASH Register Address

Table 4-5 FLASH Register Address (FLASH Register Base Address:0x00000000)

Name	Type	Address	Description	Default
FLASH_ICEPROT	R/W	0xFFFA8	ICE protect register	--
FLASH_RDPROT	R	0xFFFAC	FLASH register for read protect status	0x00000000
FLASH_WRPROT	R/W	0xFFFB0	FLASH register for write protect control	0x00000000
FLASH_STS	R	0xFFFBC	FLASH register for programmable status	0x00
FLASH_INTSTS	R/C	0xFFFCC	FLASH register for checksum interrupt status	0x0
FLASH_CSSADDR	R/W	0xFFFD0	FLASH register for checksum starting address	0x00000

FLASH_CSEADDR	R/W	0xFFFD4	FLASH register for checksum end address	0xFFFFF
FLASH_CSVALUE	R	0xFFFD8	FLASH read register for checksum value	--
FLASH_CSCVALUE	R/W	0xFFFDC	FLASH read register for checksum comparison value	0x00000000
FLASH_PASS	R/W	0xFFFE0	FLASH password register	0x00000000
FLASH_CTRL	R/W	0xFFFE4	FLASH control register	0x0
FLASH_PGADDR	R/W	0xFFFE8	FLASH programming address register	0x00000
FLASH_PGDATA	R/W	0xFFFEC	FLASH programming register for word data	--
FLASH_PGB0	R/W	0xFFFEC	FLASH programming register 0 for byte data	--
FLASH_PGB1	R/W	0xFFFED	FLASH programming register 1 for byte data	--
FLASH_PGB2	R/W	0xFFFEE	FLASH programming register 2 for byte data	--
FLASH_PGB3	R/W	0xFFFEF	FLASH programming register 3 for byte data	--
FLASH_PGHW0	R/W	0xFFFEC	FLASH register 0 for nibble(half-word) data	--
FLASH_PGHW1	R/W	0xFFFEE	FLASH register 1 for nibble(half-word) data	--
FLASH_SERASE	R/W	0xFFFF4	FLASH control register for sector erase	0x00000000
FLASH_CERASE	R/W	0xFFFF8	FLASH control register for chip erase	0x00000000
FLASH_DSTB	R/W	0xFFFFC	FLASH control register for deep standby	0x00000000

4.1.5 GPIO Register Address

Table 4-6 GPIO Register Address (GPIO Base Address:0x40000000)

Name	Type	Address	Description	Default
IOB_OEN	R/W	0x0020	IOB register for output enable	0xFFFF
IOB_IE	R/W	0x0024	IOB register for input enable	0xFFFF
IOB_DAT	R/W	0x0028	IOB register for output data	0x0000
IOB_ATT	R/W	0x002C	IOB attribute register	0x0000
IOB_STS	R	0x0030	IOB register for input status	--

IOC_OEN	R/W	0x0040	IOC register for output enable	0xFFFF
IOC_IE	R/W	0x0044	IOC register for input enable	0xFFFF
IOC_DAT	R/W	0x0048	IOC register for output data	0x0000
IOC_ATT	R/W	0x004C	IOC attribute register	0x0000
IOC_STS	R	0x0050	IOC register for input status	--
IOD_OEN	R/W	0x0060	IOD register for output enable	0xFFFF
IOD_IE	R/W	0x0064	IOD register for input enable	0xFFFF
IOD_DAT	R/W	0x0068	IOD register for output data	0x0000
IOD_ATT	R/W	0x006C	IOD attribute register	0x0000
IOD_STS	R	0x0070	IOD register for input status	--
IOE_OEN	R/W	0x0080	IOE register for output enable	0xFFFF
IOE_IE	R/W	0x0084	IOE register for input enable	0xFFFF
IOE_DAT	R/W	0x0088	IOE register for output data	0x0000
IOE_ATT	R/W	0x008C	IOE attribute register	0x0000
IOE_STS	R	0x0090	IOE register for input status	--
IOF_OEN	R/W	0x00A0	IOF register for output enable	0x7FFF
IOF_IE	R/W	0x00A4	IOF register for input enable	0x7FFF
IOF_DAT	R/W	0x00A8	IOF register for output data	0x0
IOF_ATT	R/W	0x00AC	IOF attribute register	0x0
IOF_STS	R	0x00B0	IOF register for input status	--
IOB_SEL	R/W	0x00C0	IOB register for special function select	0x00
IOE_SEL	R/W	0x00CC	IOE register for special function select	0x00
IO_MISC	R/W	0x00E0	IO misc. control register	0x00

4.1.6 DMA Register Address

Table 4-7 DMA Register Address (DMA Base Address:0x40010000)

Name	Type	Address	Description	Default
DMA_IE	R/W	0x0000	DMA interrupt enable register	0x000
DMA_STS	R/W	0x0004	DMA status register	0x0000
DMA_C0CTL	R/W	0x0010	DAM channel 0 control register	0x00000000

DMA_C0SRC	R/W	0x0014	DMA source address register for channel 0	0x00000000
DMA_C0DST	R/W	0x0018	DMA destination address register for channel 0	0x00000000
DMA_C0LEN	R	0x001C	DMA transfer length register for channel 0	0x0000
DMA_C1CTL	R/W	0x0020	DMA channel 1 control register	0x00000000
DMA_C1SRC	R/W	0x0024	DMA channel 1 source register	0x00000000
DMA_C1DST	R/W	0x0028	DMA channel 1 destination register	0x00000000
DMA_C1LEN	R	0x002C	DMA channel 1 transmission length register	0x0000
DMA_C2CTL	R/W	0x0030	DMA channel 2 control register	0x00000000
DMA_C2SRC	R/W	0x0034	DMA channel 2 source register	0x00000000
DMA_C2DST	R/W	0x0038	DMA channel 2 destination register	0x00000000
DMA_C2LEN	R	0x003C	DMA channel 2 transmission length register	0x0000
DMA_C3CTL	R/W	0x0040	DMA channel 3 control register	0x00000000
DMA_C3SRC	R/W	0x0044	DMA channel 3 source address register	0x00000000
DMA_C3DST	R/W	0x0048	DMA channel 3 destination register	0x00000000
DMA_C3LEN	R	0x004C	DMA channel 3 transmission length register	0x0000
DMA_AESCTL	R/W	0x0050	DMA AES control register	0x00000000
DMA_AESKEY0	R/W	0x0060	DMA AES key 0 reigster	0x00000000
DMA_AESKEY1	R/W	0x0064	DMA AES key 1 register	0x00000000
DMA_AESKEY2	R/W	0x0068	DMA AES key 2 reigster	0x00000000
DMA_AESKEY3	R/W	0x006C	DMA AES key 3 register	0x00000000
DMA_AESKEY4	R/W	0x0070	DMA AES key 4 register	0x00000000
DMA_AESKEY5	R/W	0x0074	DMA AES key 5 register	0x00000000
DMA_AESKEY6	R/W	0x0078	DMA AES key 6 register	0x00000000
DMA_AESKEY7	R/W	0x007C	DMA AES key 7 register	0x00000000

4.1.7 UART Register Address

Table 4-8 UART Register Address (UART Base Address:0x40011800)

Name	Type	Address	Description	Default
UART0_DATA	R/W	0x0000	UART0 data register	0x00
UART0_STATE	R/C	0x0004	UART0 status register	0x00
UART0_CTRL	R/W	0x0008	UART0 control register	0x000
UART0_INTSTS	R/C	0x000C	UART0 interrupt status register	0x00
UART0_BAUDDIV	R/W	0x0010	UART0 register for baud rate divider	0x00000
UART0_CTRL2	R/W	0x0014	UART0 control register 2	0x0
UART1_DATA	R/W	0x0020	UART1 data register	0x00
UART1_STATE	R/C	0x0024	UART1 status register	0x00
UART1_CTRL	R/W	0x0028	UART1 control register	0x000
UART1_INTSTS	R/C	0x002C	UART1 interrupt status register	0x00
UART1_BAUDDIV	R/W	0x0030	UART1 register for baud rate divider	0x00000
UART1_CTRL2	R/W	0x0034	UART1 control register 2	0x0
UART2_DATA	R/W	0x0040	UART2 data register	0x00
UART2_STATE	R/C	0x0044	UART2 status register	0x00
UART2_CTRL	R/W	0x0048	UART2 control register	0x000
UART2_INTSTS	R/C	0x004C	UART2 interrupt status register	0x00
UART2_BAUDDIV	R/W	0x0050	UART2 register for baud rate divider	0x00000
UART2_CTRL2	R/W	0x0054	UART2 control register 2	0x0
UART3_DATA	R/W	0x0060	UART3 data register	0x00
UART3_STATE	R/C	0x0064	UART3 status register	0x00
UART3_CTRL	R/W	0x0068	UART3 control register	0x000
UART3_INTSTS	R/C	0x006C	UART3 interrupt status register	0x00
UART3_BAUDDIV	R/W	0x0070	UART3 register for baud rate divider	0x00000
UART3_CTRL2	R/W	0x0074	UART3 control register 2	0x0
UART4_DATA	R/W	0x0080	UART4 data register	0x00
UART4_STATE	R/C	0x0084	UART4 status register	0x00
UART4_CTRL	R/W	0x0088	UART4 control register	0x000

UART4_INTSTS	R/C	0x008C	UART4 interrupt status register	0x00
UART4_BAUDDIV	R/W	0x0090	UART4 register for baud rate divider	0x00000
UART4_CTRL2	R/W	0x0094	UART4 control register 2	0x0
UART5_DATA	R/W	0x00A0	UART5 data register	0x00
UART5_STATE	R/C	0x00A4	UART5 status register	0x00
UART5_CTRL	R/W	0x00A8	UART5 control register	0x000
UART5_INTSTS	R/C	0x00AC	UART5 interrupt status register	0x00
UART5_BAUDDIV	R/W	0x00B0	UART5 register for baud rate divider	0x00000
UART5_CTRL2	R/W	0x00B4	UART5 control register 2	0x0

4.1.8 UART32K Register Address

Table 4-9 UART32K Register Address (UART32K Base Address:0x40014100)

Name	Type	Address	Description	Default
U32K0_CTRL0	R/W	0x0000	UART32K0 control register 0	0x000
U32K0_CTRL1	R/W	0x0004	UART32K0 control register 1	0x00
U32K0_BAUDDIV	R/W	0x0008	UART32K0 register for baud rate divider	0x4B00
U32K0_DATA	R	0x000C	UART32K0 register for receive data	--
U32K0_STS	R/C	0x0010	UART32K0 interrupt status register	0x0
U32K1_CTRL0	R/W	0x0080	UART32K1 control register 0	0x000
U32K1_CTRL1	R/W	0x0084	UART32K1 control register 1	0x00
U32K1_BAUDDIV	R/W	0x0088	UART32K1 register for baud rate divider	0x4B00
U32K1_DATA	R	0x008C	UART32K1 register for receive data	--
U32K1_STS	R/C	0x0090	UART32K1 interrupt status register	0x0

4.1.9 ISO7816 Register Address

Table 4-10 ISO7816 Register Address (ISO7816 Base Address:0x40012000)

Name	Type	Address	Description	Default
ISO78160_BAUDDIVL	R/W	0x0004	ISO 78160 baud-rate low byte register	0x00
ISO78160_BAUDDIVH	R/W	0x0008	ISO78160 baud-rate high byte register	0x00
ISO78160_DATA	R/W	0x000C	ISO78160 data register	0x00
ISO78160_INFO	R/C	0x0010	ISO78160 information register	0x00

ISO78160_CFG	R/W	0x0014	ISO78160 control register	0x00
ISO78160_CLK	R/W	0x0018	ISO78160 clock divider control register	0x00
ISO78161_BAUDDIVL	R/W	0x0044	ISO78161 baud-rate low byte register	0x00
ISO78161_BAUDDIVH	R/W	0x0048	ISO78161 baud-rate high byte register	0x00
ISO78161_DATA	R/W	0x004C	ISO78161 data register	0x00
ISO78161_INFO	R/C	0x0050	ISO78161 information register	0x00
ISO78161_CFG	R/W	0x0054	ISO78161 control register	0x00
ISO78161_CLK	R/W	0x0058	ISO78161 clock divider control register	0x00

4.1.10 TIMER/PWM Register Address

Table 4-11 TIMER Register Address (32-byte TIMER Base Address:0x40012800)

Name	Type	Address	Description	Default
TMR0_CTRL	R/W	0x0000	Timer0 control register	0x0
TMR0_VALUE	R/W	0x0004	Timer0 real-time counting register	0x00000000
TMR0_RELOAD	R/W	0x0008	Timer0 reloading register	0x00000000
TMR0_INTSTS	R/C	0x000C	Timer0 interrupt status register	0x0
TMR1_CTRL	R/W	0x0020	Timer1 control register	0x0
TMR1_VALUE	R/W	0x0024	Timer1 real-time counting register	0x00000000
TMR1_RELOAD	R/W	0x0028	Timer1 reloading register	0x00000000
TMR1_INTSTS	R/C	0x002C	Timer1 interrrupt status register	0x0
TMR2_CTRL	R/W	0x0040	Timer2 control register	0x0
TMR2_VALUE	R/W	0x0044	Timer2 real-time counting register	0x00000000
TMR2_RELOAD	R/W	0x0048	Timer2 reloading register	0x00000000
TMR2_INTSTS	R/C	0x004C	Timer2 interrupt status register	0x0
TMR3_CTRL	R/W	0x0060	Timer3 control register	0x0
TMR3_VALUE	R/W	0x0064	Timer3 real-time counting register	0x00000000
TMR3_RELOAD	R/W	0x0068	Timer3 reloading register	0x00000000
TMR3_INTSTS	R/C	0x006C	Timer3 interrupt status register	0x0

Table 4-12 PWM TIMER Register Address (16-byte PWM TIMER Base Address:0x40012900)

Name	Type	Address	Description	Default
PWM0_CTL	R/W	0x0000	PWM Timer0 control register	0x00
PWM0_TAR	R	0x0004	PWM Timer0 real-time counting register	0x0000
PWM0_CCTL0	R/W	0x0008	PWM Timer0 compare/ capture control register 0	0x000
PWM0_CCTL1	R/W	0x000C	PWM Timer0 compare/capture control register 1	0x000
PWM0_CCTL2	R/W	0x0010	PWM Timer0 compare/ capture control register 2	0x000
PWM0_CCR0	R/W	0x0014	PWM Timer0 compare /capture data register 0	0x0000
PWM0_CCR1	R/W	0x0018	PWM Timer0 compare/capture data register 1	0x0000
PWM0_CCR2	R/W	0x001C	PWM Timer0 compare/ capture data register 2	0x0000
PWM1_CTL	R/W	0x0020	PWM Timer1 control register	0x00
PWM1_TAR	R	0x0024	PWM Timer1 real-time counting register	0x0000
PWM1_CCTL0	R/W	0x0028	PWM Timer1 compare/ capture data register 0	0x000
PWM1_CCTL1	R/W	0x002C	PWM Timer1 compare/ capture data register 1	0x000
PWM1_CCTL2	R/W	0x0030	PWM Timer1 compare /capture data register 2	0x000
PWM1_CCR0	R/W	0x0034	PWM Timer1 compare/capture data register 0	0x0000
PWM1_CCR1	R/W	0x0038	PWM Timer1 compare/capture data register 1	0x0000
PWM1_CCR2	R/W	0x003C	PWM Timer1 compare/capture data register 2	0x0000
PWM2_CTL	R/W	0x0040	PWM Timer2 control register	0x00
PWM2_TAR	R	0x0044	PWM Timer2 real-time counting register	0x0000

PWM2_CCTL0	R/W	0x0048	PWM Timer2 compare/capture control register 0	0x000
PWM2_CCTL1	R/W	0x004C	PWM Timer2 compare/capture control register 1	0x000
PWM2_CCTL2	R/W	0x0050	PWM Timer2 compare/capture control register 2	0x000
PWM2_CCR0	R/W	0x0054	PWM Timer2 compare/capture data register 0	0x0000
PWM2_CCR1	R/W	0x0058	PWM Timer2 compare/capture data register 1	0x0000
PWM2_CCR2	R/W	0x005C	PWM Timer2 compare/capture data register 2	0x0000
PWM3_CTL	R/W	0x0060	PWM Timer3 control register	0x00
PWM3_TAR	R	0x0064	PWM Timer3 real-time counting register	0x0000
PWM3_CCTL0	R/W	0x0068	PWM Timer3 compare/ capture control register 0	0x000
PWM3_CCTL1	R/W	0x006C	PWM Timer3 compare/capture control register 1	0x000
PWM3_CCTL2	R/W	0x0070	PWM Timer3 compare/capture control register 2	0x000
PWM3_CCR0	R/W	0x0074	PWM Timer3 compare/capture data register 0	0x0000
PWM3_CCR1	R/W	0x0078	PWM Timer3 compare/capture data register 1	0x0000
PWM3_CCR2	R/W	0x007C	PWM Timer3 compare/ capture data register 2	0x0000
PWM_O_SEL	R/W	0x00F0	PWM output selectable register	0xDB51
PWM_I_SEL01	R/W	0x00F4	PWM0 PWM1 input selectable register	0x00390024
PWM_I_SEL23	R/W	0x00F8	PWM2 PWM3 input selectable register	0x0013000E

4.1.11 LCD Register

Table 4-13 LCD Register Address (LCD Base Address:0x40002000)

Name	Type	Address	Description	Default

LCD_FB00	R/W	0x0000	LCD frame buffer 0 register	--
LCD_FB01	R/W	0x0004	LCD frame buffer 1 register	--
LCD_FB02	R/W	0x0008	LCD frame buffer 2 register	--
LCD_FB03	R/W	0x000C	LCD frame buffer 3 register	--
LCD_FB04	R/W	0x0010	LCD frame buffer 4 register	--
LCD_FB05	R/W	0x0014	LCD frame buffer 5 register	--
LCD_FB06	R/W	0x0018	LCD frame buffer 6 register	--
LCD_FB07	R/W	0x001C	LCD frame buffer 7 register	--
LCD_FB08	R/W	0x0020	LCD frame buffer 8 register	--
LCD_FB09	R/W	0x0024	LCD frame buffer 9 register	--
LCD_FB0A	R/W	0x0028	LCD frame buffer 10 register	--
LCD_FB0B	R/W	0x002C	LCD frame buffer 11 register	--
LCD_FB0C	R/W	0x0030	LCD frame buffer 12 register	--
LCD_FB0D	R/W	0x0034	LCD frame buffer 13 register	--
LCD_FB0E	R/W	0x0038	LCD frame buffer 14 register	--
LCD_FB0F	R/W	0x003C	LCD frame buffer 15 register	--
LCD_FB10	R/W	0x0040	LCD frame buffer 16 register	--
LCD_FB11	R/W	0x0044	LCD frame buffer 17 register	--
LCD_FB12	R/W	0x0048	LCD frame buffer 18 register	--
LCD_FB13	R/W	0x004C	LCD frame buffer 19 register	--
LCD_FB14	R/W	0x0050	LCD frame buffer 20 register	--
LCD_FB15	R/W	0x0054	LCD frame buffer 21 register	--
LCD_FB16	R/W	0x0058	LCD frame buffer 22 register	--
LCD_FB17	R/W	0x005C	LCD frame buffer 23 register	--
LCD_FB18	R/W	0x0060	LCD frame buffer 24 register	--
LCD_FB19	R/W	0x0064	LCD frame buffer 25 register	--
LCD_FB1A	R/W	0x0068	LCD frame buffer 26 register	--
LCD_FB1B	R/W	0x006C	LCD frame buffer 27 register	--

LCD_FB1C	R/W	0x0070	LCD frame buffer 28 register	--
LCD_FB1D	R/W	0x0074	LCD frame buffer 29 register	--
LCD_FB1E	R/W	0x0078	LCD frame buffer 30 register	--
LCD_FB1F	R/W	0x007C	LCD frame buffer 31 register	--
LCD_FB20	R/W	0x0080	LCD frame buffer 32 register	--
LCD_FB21	R/W	0x0084	LCD frame buffer 33 register	--
LCD_FB22	R/W	0x0088	LCD frame buffer 34 register	--
LCD_FB23	R/W	0x008C	LCD frame buffer 35 register	--
LCD_FB24	R/W	0x0090	LCD frame buffer 36 register	--
LCD_FB25	R/W	0x0094	LCD frame buffer 37 register	--
LCD_FB26	R/W	0x0098	LCD frame buffer 38 register	--
LCD_FB27	R/W	0x009C	LCD frame buffer 39 register	--
LCD_CTRL	R/W	0x0100	LCD control register	0x00
LCD_CTRL2	R/W	0x0104	LCD control register 2	0x0000
LCD_SEGCTRL0	R/W	0x0108	LCDSEG enable control register 0	0x00000000
LCD_SEGCTRL1	R/W	0x010C	LCDSEG enable control register 1	0x00000000
LCD_SEGCTRL2	R/W	0x0110	LCDSEG enable control register 2	0x00000000

4.1.12 SPI Register Address

Table 4-14 SPI1 Register Address (SPI1 Base Address:0x40011000)

Name	Type	Address	Description	Default
SPI1_CTRL	R/W	0x0000	SPI1 Control Register	0x0000
SPI1_TXSTS	R/W	0x0004	SPI1 transmit status register	0x8200
SPI1_TXDAT	R/W	0x0008	SPI1 transmit FIFO register	--
SPI1_RXSTS	R/W	0x000C	SPI1 receive status register	0x0000
SPI1_RXDAT	R/W	0x0010	SPI1 receive FIFO register	--
SPI1_MISC	R/W	0x0014	SPI1 Misc control register	0x0003

Table 4-15 SPI2 Register Address (SPI2 Base Address:0x40015800)

Name	Type	Address	Description	Default

SPI2_CTRL	R/W	0x0000	SPI2 control register	0x0000
SPI2_TXSTS	R/W	0x0004	SPI2 transmit status register	0x8200
SPI2_TXDAT	R/W	0x0008	SPI2 transmit FIFO register	--
SPI2_RXSTS	R/W	0x000C	SPI2 receive status register	0x0000
SPI2_RXDAT	R/W	0x0010	SPI2 receive FIFO register	--
SPI2_MISC	R/W	0x0014	SPI2 Misc control register	0x0003

Table 4-16 SPI3 Register Address (SPI3 Base Address:0x40016000)

Name	Type	Address	Description	Default
SPI3_CTRL	R/W	0x0000	SPI3 control register	0x0000
SPI3_TXSTS	R/W	0x0004	SPI3 transmit status register	0x8200
SPI3_TXDAT	R/W	0x0008	SPI3 transmit FIFO register	--
SPI3_RXSTS	R/W	0x000C	SPI3 receive status register	0x0000
SPI3_RXDAT	R/W	0x0010	SPI3 receive FIFO register	--
SPI3_MISC	R/W	0x0014	SPI3 Misc control register	0x0003

4.1.13 I^2C Register Address

Table 4-17 I^2C Register Address (I^2C Base Address:0x40010800)

Name	Type	Address	Description	Default
I2C_DATA	R/W	0x0000	I^2C data register	0x00
I2C_ADDR	R/W	0x0004	I^2C address register	0x00
I2C_CTRL	R/W	0x0008	I^2C control/ status register	0x00
I2C_STS	R/W	0x000C	I^2C status register	0xF8
I2C_CTRL2	R/W	0x0018	I^2C interrupt enable register	0x0

4.1.14 MISC Register Address

Table 4-18 MISC Register Address (MISC Base Address:0x40013000)

Name	Type	Address	Description	Default
MISC1_SRAMINT	R/C	0x0000	SRAM interrupt status register for parity check error	0x00
MISC1_SRAMINIT	R/W	0x0004	SRAM initialization register	0x01
MISC1_PARERR	R	0x0008	SRAM parity check error address register	0x000

MISC1_IREN	R/W	0x000C	IR enable control register	0x00
MISC1_DUTYL	R/W	0x0010	IR duty-low width control register	0x0000
MISC1_DUTYH	R/W	0x0014	IR duty-high width control register	0x0000
MISC1_IRQLAT	R/W	0x0018	Cortex-M0 IRQ delay control register	0x000
MISC1_HIADDR	R	0x0020	Record the illegal address of accessing AHB	--
MISC1_PIADDR	R	0x0024	Record the illegal address of accessing APB	--

Table 4-19 MISC2 Base Address (MISC2 Base Address:0x40013E00)

Name	Type	Address	Description	Default
MISC2_FLASHWC	R/W	0x0000	FLASH waiting cycle register	0x2100
MISC2_CLKSEL	R/W	0x0004	System clock select register	0x0
MISC2_CLKDIVH	R/W	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	R/W	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	R/W	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB clock enable control register	0xFFFFFFFF

4.1.15 CRYPT Register Address

Table 4-20 CRYPT Register Address (CRYPT Base Address:0x40006000)

Name	Type	Address	Description	Default
CRYPT_CTRL	R/W	0x0000	CRYPT control register	0x0000
CRYPT_PTRA	R/W	0x0004	CRYPT clock pointer A	0x0000
CRYPT_PTRB	R/W	0x0008	CRYPT clock pointer B	0x0000
CRYPT_PTRO	R/W	0x000C	CRYPT clock pointer O	0x0000
CRYPT_CARRY	R	0x0010	CRYPT borrow/ carry register	0x0

4.1.16 Info Register

The information of Info register is stored in the area starting with 0x00080400, and can only be read but not written. All information has double backup, the first data in the table is represented by 1, and the second data is represented by 2. Each piece of data comes with a checksum, a check algorithm: the data of the data items in each piece are added, and the result after the addition is inverted.

The data at address 0x00080400~0x000805FF is the default value that requires software to load the chip register. The data has been written before leaving the factory.

The data at address 0x00080800~0x0008085C is written by special programming tool (offline programming and RTC calibration function is enabled). Other data has been written before leaving the factory.

Table 4-21 Info Message Register

Address	Symbol	Message	Description
0x00080400		Count	The configuration value requires the number of registers loaded by the software from the info area.
0x00080404		Check_sum1	INV(SUM(0x80400, 0x80400))
0x00080408		address0	ANA_REG0, 0x40014200
0x0008040C		value0	0x30
0x00080410		Check_sum1	INV(SUM(0x80408, 0x8040C))
0x00080414		address1	ANA_REG4, 0x40014210
0x00080418		value1	0x01
0x0008041C		Check_sum1	INV(SUM(0x80414, 0x80418))
0x00080420		address2	ANA_REG7, 0x4001421C
0x00080424		value2	0x80
0x00080428		Check_sum1	INV(SUM(0x80420, 0x80424))
0x0008042C		address3	ANA_REGA, 0x40014228
0x00080430		value3	0x02
0x00080434		Check_sum1	INV(SUM(0x8042C, 0x80430))
0x00080438		address4	ANA_ADCCTRL0, 0x40014268
0x0008043C		value4	0x300000
0x00080440		Check_sum1	INV(SUM(0x80438, 0x8043C))
0x00080444		address5	LCD_CTRL, 0x40002100
0x00080448		value5	0x84
0x0008044C		Check_sum1	INV(SUM(0x80438, 0x8043C))
0x00080450		address6	RTC_ADCUCALK, 0x400148E8
0x00080454		value6	0x599A599A
0x00080458		Check_sum1	INV(SUM(0x80450, 0x80458))
0x0008045C		address7	RTC_ADCMACTL, 0x400148EC
0x00080460		value7	0x78000000

0x00080464		Check_sum1	INV(SUM(0x8045C, 0x80460))
0x00080468		address8	RTC_ADCDTCTL, 0x400148F0
0x0008046C		value8	0x80000000
0x00080470		Check_sum1	INV(SUM(0x80468, 0x8046C))
0x00080474		address9	GPIOA_IE
0x00080478		value9	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x0008047C		Check_sum1	
0x00080480		address10	GPIOB_IE
0x00080484		value10	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00080488		Check_sum1	
0x0008048C		address11	GPIOC_IE
0x00080490		value11	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00080494		Check_sum1	
0x00080498		address12	GPIOD_IE
0x0008049C		value12	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x000804A0		Check_sum1	
0x000804A4		address13	GPIOE_IE
0x000804A8		value13	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x000804AC		Check_sum1	
0x000804B0		address14	GPIOF_IE
0x000804B4		value14	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x000804B8		Check_sum1	

…		…	…
0x00080500		Count	The configuration value requires the number of registers loaded by the software from the infor area
0x00080504		Check_sum2	INV(SUM(0x80500, 0x80500))
0x00080508		address0	ANA_REG0, 0x40014200
0x0008050C		value0	0x30
0x00080510		Check_sum2	INV(SUM(0x80508, 0x8050C))
0x00080514		address1	ANA_REG4, 0x40014210
0x00080518		value1	0x01
0x0008051C		Check_sum2	INV(SUM(0x80514, 0x80518))
0x00080520		address2	ANA_REG7, 0x4001421C
0x00080524		value2	0x80
0x00080528		Check_sum2	INV(SUM(0x80520, 0x80524))
0x0008052C		address3	ANA_REGA, 0x40014228
0x00080530		value3	0x02
0x00080534		Check_sum2	INV(SUM(0x8052C, 0x80530))
0x00080538		address4	ANA_ADCCTRL0, 0x40014268
0x0008053C		value4	0x300000
0x00080540		Check_sum2	INV(SUM(0x80538, 0x8053C))
0x00080544		address5	LCD_CTRL, 0x40002100
0x00080548		value5	0x84
0x0008054C		Check_sum2	INV(SUM(0x80538, 0x8053C))
0x00080550		address6	RTC_ADCUCALK, 0x400148E8
0x00080554		value6	0x599A599A
0x00080558		Check_sum2	INV(SUM(0x80550, 0x80558))
0x0008055C		address7	RTC_ADCMACTL, 0x400148EC
0x00080560		value7	0x78000000
0x00080564		Check_sum2	INV(SUM(0x8055C, 0x80560))
0x00080568		address8	RTC_ADCDTCTL, 0x400148F0
0x0008056C		value8	0x80000000

0x00080570		Check_sum2	INV(SUM(0x80568, 0x8056C))
0x00080574		address9	GPIOA_IE
0x00080578		value9	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x0008057C		Check_sum2	
0x00080580		address10	GPIOB_IE
0x00080584		value10	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00080588		Check_sum2	
0x0008058C		address11	GPIOC_IE
0x00080590		value11	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00080594		Check_sum2	
0x00080598		address12	GPIOD_IE
0x0008059C		value12	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x000805A0		Check_sum2	
0x000805A4		address13	GPIOE_IE
0x000805A8		value13	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x000804AC		Check_sum2	
0x000805B0		address14	GPIOF_IE
0x000805B4		value14	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x000805B8		Check_sum2	
…	…	…	…
0x00080800	P4	Crystal temperature offset 1	Unit(0.1ppm), lower 16-bit download to RTC_ACP4 register such as 0.

0x00080804		Checksum1	INV(SUM(0x80800, 0x80800))
0x00080808	P4	Crystal temperature offset 2	Unit(0.1ppm), lower 16-bit download to RTC_ACP4 register such as 0.
0x0008080C		Checksum2	INV(SUM(0x80808, 0x80808))
0x00080810	K0	K0 cofficient 1	Load to RTC_ACK0 register, the calculation formula of K0 is as below: K0=B0/1000000*65536, B0 is the segmentation coefficient of the crystal curve. K0=20827.
0x00080814	K1	K1 cofficient 1	Load to RTC_ACK1 register, the calculation formula of K1 is as below: K1=B1/1000000*65536, B1 is the segmentation coefficient of the crystal curve. K1=21496.
0x00080818	K2	K2 cofficient 1	Load to RTC_ACK2 register, the calculation formula of K2 is as below: K2=B2/1000000*65536, B2 is the segmentation coefficient of the crystal curve. K1=22020.
0x0008081C	K3	K3 cofficient 1	Load to RTC_ACK3 register, the calculation formula of K3 is as below: K3=B3/1000000*65536, B3 is the segmentation coefficient of the crystal curve. K3=24517.
0x00080820	K4	K4 cofficient 1	Load to RTC_ACK4 register, the calculation formula of K4 is as below: K4=B4/1000000*65536, B4 is the segmentation coefficient of the crystal curve. K4=25257.
0x00080824		Checksum1	INV(SUM(0x80810, 0x80820))
0x00080828	K0	K0 cofficient 2	Load to RTC_ACK0 register, the calculation formula of K0 is as below: K0=B0/1000000*65536, B0 is the segmentation coefficient of the crystal curve. K0=20827.
0x0008082C	K1	K1 cofficient 2	Load to RTC_ACK1 register, the calculation

			formula of K1 is as below: K1=B1/1000000*65536, B1 is the segmentation coefficient of the crystal curve. K1=21496.
0x00080830	K2	K2 cofficient 2	Load to RTC_ACK2 register, the calculation formula of K2 is as below: K2=B2/1000000*65536, B2 is the segmentation coefficient of the crystal curve. K2=22020.
0x00080834	K3	K3 cofficient 2	Load to RTC_ACK3 register, the calculation formula of K3 is as below: K3=B3/1000000*65536, B3 is the segmentation coefficient of the crystal curve. K3=24517.
0x00080838	K4	K4 cofficient 2	Load to RTC_ACK4 register, the calculation formula of K4 is as below: K4=B4/1000000*65536, B4 is the segmentation coefficient of the crystal curve. K4=25257.
0x0008083C		Checksum2	INV(SUM(0x80828, 0x80838))
0x00080840	ACTI	the highest temperature 1	Download 0x1800 to RTC_ACTI register. .
0x00080844		Checksum1	INV(SUM(0x80840, 0x80840))
0x00080848	ACTI	the highest temperature 2	Download 0x1800 to RTC_ACTI register. .
0x0008084C		Checksum2	INV(SUM(0x80848, 0x80848))
0x00080850	KTEMPx(x=4~1)	Temperature coefficient 1	Download 0x3C2800EC to RTC_ACKTEMP register. .
0x00080854	—	Checksum1	INV(SUM(0x80850, 0x80850))
0x00080858	KTEMPx(x=4~1)		Download 0x3C2800EC to RTC_ACKTEMP register.
0x0008085C		Checksum2	INV(SUM(0x80858, 0x80858))
…	-	-	Reserved.
0x00080C00	a1	a1(ADC_CH4 no voltage division and set 1) (5V system)	Vdc=a1/100000000*X+b1/100000000+offset1 (Negative values are stored in complements.)

0x00080C04	b1	b1(ADC_CH4 no voltage division and set 1) (5V system)	
0x00080C08	a2	a2(ADC_CH4 resistance and voltage division to set 1) (5V system)	Vdc=a2/100000000*X+b2/100000000+offset2 (Negative values are stored in complements.)
0x00080C0C	b2	b2(ADC_CH4 resistance and voltage division to set 1) (5V system)	
0x00080C10	a3	a3(BAT1 resistance and voltage division to set 1) (5V system)	Vdc=a3/100000000*X+b3/100000000+offset3 (Negative values are stored in complements.)
0x00080C14	b3	b3(BAT1 resistance and voltage division to set 1) (5V system)	
0x00080C18	a4	a4(BATRTC resistance and voltage division to set1) (5V system)	Vdc=a4/100000000*X+b4/100000000+offset4 (Negative values are stored in complements.)
0x00080C1C	b4	b4 (BATRTC reisistance voltage division to set 1) (5V system)	
0x00080C20		Checksum1	INV(SUM(0x00080C00, 0x00080C1C))
0x00080C24	a1	a1(ADC_CH4 no voltage division and set 2) (5V system)	Same as backup 1
0x00080C28	b1	b1(ADC_CH4 no voltage division and set 2) (5V system)	
0x00080C2C	a2	a2(ADC_CH4 reisistance voltage division to set 2) (5V system)	
0x00080C30	b2	b2(ADC_CH4 resistance voltage division to set 2)	

		(5V system)	
0x00080C34	a3	a3(BAT1 resistance voltage division to set 2) (5V system)	
0x00080C38	b3	b3 (BAT1 voltgae division to set 2)(5V system)	
0x00080C3C	a4	a4(BATRTC voltage division to set 2) (5V system)	
0x00080C40	b4	b4 (BATRTC voltage division to set 2) (5V system)	
0x00080C44		Checksum2	
0x00080C48	a1	a1(ADC_CH4 no voltage division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C4C	b1	b1(ADC_CH4 no voltage division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C50	a2	a2(ADC_CH4 no voltage division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C54	b2	b2(ADC_CH4 resistance division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C58	a3	a3 (BAT1 resistance division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C5C	b3	b3 (BAT1 resistance division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)

0x00080C60	a4	a4(BATRTC resistance division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C64	b4	b4(BATRTC resistance division to set 1) (3.3V system)	The original value is enlarged by 100000000 times, and the 32-bit value is stored (Negative values are stored in complements.)
0x00080C68		Checksum1	INV(SUM(0x80C48, 0x80C64))
0x00080C6C	a1	a1 (ADC_CH4 no voltage division to set 2) (3.3V system)	Same as backup 1
0x00080C70	b1	b1 (ADC_CH4 no voltage division to set 2) (3.3V system)	
0x00080C74	a2	a2(ADC_CH4 resistance division to set 2) (3.3V system)	
0x00080C78	b2	b2(ADC_CH4 resistance division to set 2）(3.3V system)	
0x00080C7C	a3	a3(BAT1 resistance division to set 2) (3.3V system)	
0x00080C80	b3	b3(BAT1 resistance division to set 2) (3.3V system)	
0x00080C84	a4	a4(BATRTC resistance division to set 2) (3.3V system)	
0x00080C88	b4	b4(BATRTC resistance division to set 2) (3.3V system)	
0x00080C8C		Checksum2	
0x00080C90	Offset1	ADC_CH4 non-divided voltage test deviation 1	(test value – theoretical value)*1000

0x00080C94	Offset2	ADC_CH4 Resistance divider test deviation 1 (5V system)	(test value – theoretical value)*1000
0x00080C98	Offset3	BAT1 Resistance voltage division offset 1 (5V system)	(test value – theoretical value)*1000
0x00080C9C	Offset4	BATRTC Resistance voltage division offset 1 (5V system)	(test value – theoretical value)*1000
0x00080CA0		Checksum1	INV(SUM(0x80C90, 0x80C9C))
0x00080CA4	Offset1	ADC_CH4 no voltage division to test offset 2 (5V system)	Same to backup 1
0x00080CA8	Offset2	ADC_CH4 Resistance voltage division offset 2 (5V system)	
0x00080CAC	Offset3	BAT1 Resistance voltage division offset 2 (5V system)	
0x00080CB0	Offset4	BATRTC Resistance voltage division offset 2 (5V system)	
0x00080CB4		Checksum2	
0x00080CB8	Offset1	ADC_CH4 no voltage division to test offset 1 (3.3V system)	(test value – theoretical value)*1000
0x00080CBC	Offset2	ADC_CH4 Resistance voltage division to test offset 1 (3.3V system)	(test value – theoretical value)*1000
0x00080CC0	Offset3	BAT1 Resistance voltage division offset 1 (3.3V system)	(test value – theoretical value)*1000
0x00080CC4	Offset4	BATRTC Resistance voltage division offset 1 (3.3V system)	(test value – theoretical value)*1000
0x00080CC8		Checksum1	INV(SUM(0x80CB8, 0x80CC4))

0x00080CCC	Offset1	ADC_CH4 no voltage division to test offset 2 (3.3V system)	Same to backup 1
0x00080CD0	Offset2	ADC_CH4 Resistance voltage division offset 2 (3.3V system)	
0x00080CD4	Offset3	BAT1 Resistance voltage division offset 2 (3.3V system)	
0x00080CD8	Offset4	BATRTC Resistance voltage division offset 2 (3.3V system)	
0x00080CDC		Checksum2	
0x00080D10	P1/P0	RTC_ACP1/0 set 1	The upper 16-bit are loaded into the RTC_ACP1 register, such as: 1060; the lower 16-bit are loaded into the RTC_ACP0 register, such as: -214.
0x00080D14	P2’	RTC_ACP2 set 1	The stored value of this address is recorded as P2', for example: -19746971. According to the formula: P2=P2’+(Tr-Tm)*256, load P2 into the RTC_ACP2 register.
0x00080D18	P5	RTC_ACP5 set 1	The upper 16-bit are loaded into the RTC_ACP5 register, for example: 6444; the lower 16 bits are discarded.
0x00080D1C	P7/P6’	RTC_ACP7/6 set 1	The upper 16-bit are loaded into the RTC_ACP7 register, for example: 0; the lower 16-bit are loaded into P6'. For example: 1342. According to the formula P6=a*P6', load P6 into the RTC_ACP6 register. According to the formula P6=a*P6', load P6 into the RTC_ACP6 register.
0x00080D20		Checksum1	INV(SUM(0x80D10, 0x80D1C)
0x00080D24	P1/P0	RTC_ACP1/0 set 2	Same to backup 1
0x00080D28	P2’	RTC_ACP2 set 2	

0x00080D2C	P5	RTC_ACP5 set 2	
0x00080D30	P7/P6'	RTC_ACP7/6 set 2	
0x00080D34		Checksum2	
0x00080D38		AVCC gain 1	Pre-trim result/3.3 * 10000
0x00080D3C		DVCC gain 1	Pre-trim result/1.5 * 10000
0x00080D40		BGP gain 1	Pre-trim result/1.2 * 10000
0x00080D44		RCL gain 1	Pre-trim result/32768 * 10000
0x00080D48		RCH gain 1	Pre-trim result/6553600 * 10000
0x00080D4C		Checksum1	INV(SUM(0x80D38, 0x80D48))
0x00080D50		AVCC gain 2	Same to backup 1
0x00080D54		DVCC gain 2	
0x00080D58		BGP gain 2	
0x00080D5C		RCL gain 2	
0x00080D60		RCH gain 2	
0x00080D64		Checksum2	
0x00080D68		ID word 0, Backup 1	
0x00080D6C		ID word 1, Backup 1	
0x00080D70		Checksum1	INV(SUM(0x80D68, 0x80D6C))
0x00080D74		ID word 0, Backup 2	Same to backup 1
0x00080D78		ID word 1, Backup 2	
0x00080D7C		Checksum2	
0x00080D80	Tr	The real temperature Tr1 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256, P2 loads to RTC_ACP2 register.
0x00080D84	Tm	Measure temperature Tm1 (from ADC)	According to the formula: P2=P2'+(Tr-Tm)*256, load P2 into the RTC_ACP2 register
0x00080D88		Checksum1	INV(SUM(0x80D80, 0x80D84))
0x00080D8C	Tr	The real temperature Tr2 (from tmp275)	Same to backup 1
0x00080D90	Tm	Measure temperature Tm2 (from ADC)	
0x00080D94		Checksum2	

…			Reserved.
0x00080DC0		ANA_REGBCDE trim data1	After the chip is reset, the value of ANA_REGx (x=B~E) is automatically loaded.
0x00080DC4		0xFFFFFFFF	
0x00080DC8		0xFFFFFFFF	
0x00080DCC		Checksum1	INV(SUM(0x80DC0, 0x80DC8)), where 0x00080DC8 address does not support read operation, and the data is replaced by 0xFFFFFFFF.
0x00080DD0		ANA_REGBCDE trim data2	The value of ANA_REGx (x=B~E) is automatically loaded after the chip is reset.
0x00080DD4		0xFFFFFFFF	
0x00080DD8		0xFFFFFFFF	
0x00080DDC		Checksum2	INV(SUM(0x80DD0, 0x80DD8)), where the 0x00080DD8 address does not support read operations, and the data is replaced by 0xFFFFFFFF.
0x00080DE0		ANA_REG10 trim data1	The value is automatically loaded to ANA_REG10 after chip reset.
0x00080DE4		Checksum1	INV(SUM(0x80DE0, 0x80DE0))
0x00080DE8		ANA_REG10 trim data2	The value is automatically loaded to ANA_REG10 after chip reset.
0x00080DEC		Checksum2	INV(SUM(0x80DE8, 0x80DE8))

5. Power Setting

V85XXP power controller has the following characteristics:

- Working voltage:2.2V~5.5V
- Support standalone RTC battery input.
- GPIO power supply is VDD.
- Analog circuit is powered by AVCC.
- Digital and PLL circuit is powered by DVCC.
- Supports low-voltage and real-time batterydetection.

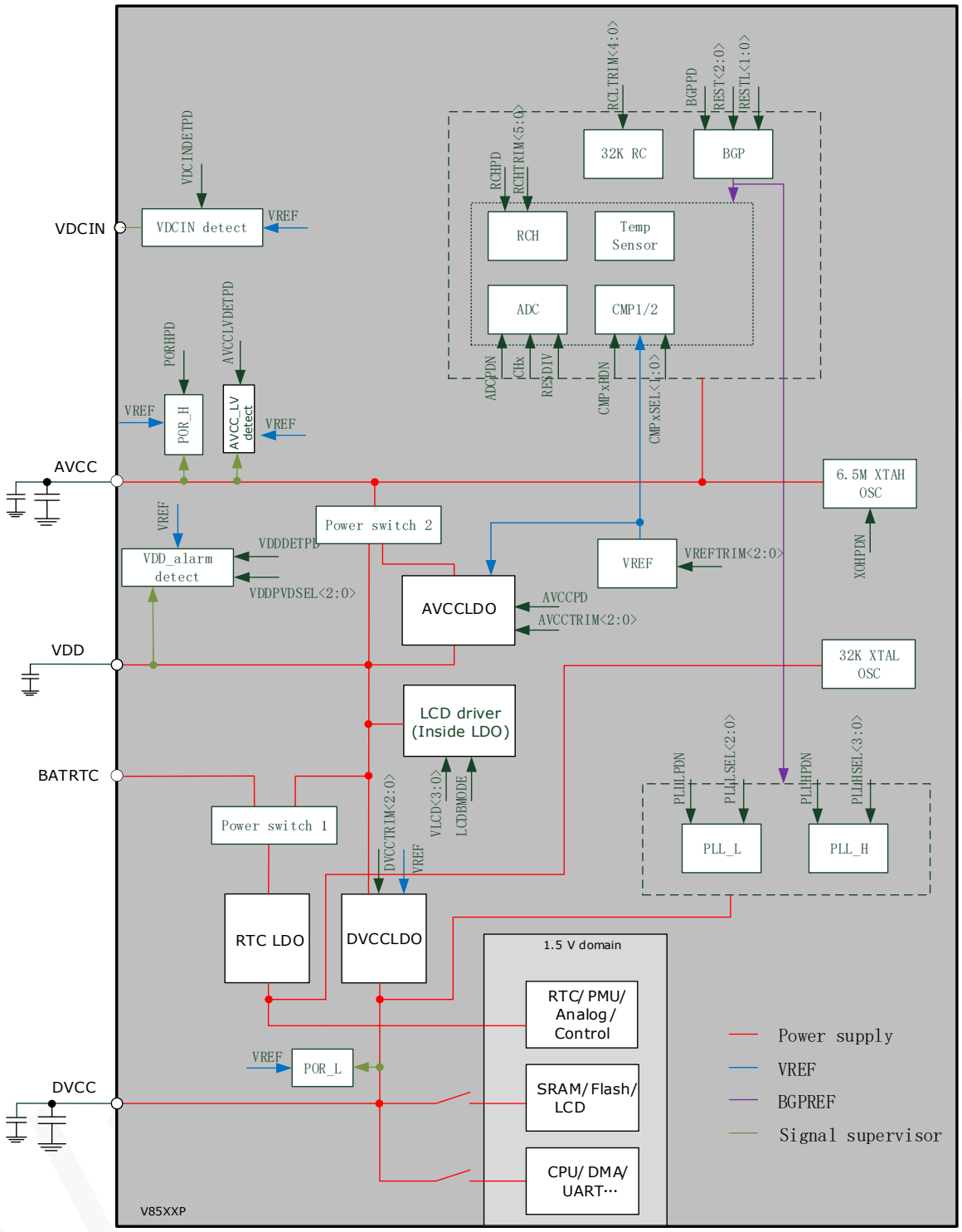


Figure 5-1 V85XXP Power System Block Diagram

5.1 Register Address

Table 5-1 ANA Register Address (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00

ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REG9	R/W	0x0024	Analog register 9	0x00
ANA_REGA	R/W	0x0028	Analog register 10	0x00
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparative result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_CMPCTL	R/W	0x006C	Comparative control register	0x00000000

5.2 The Definition of Register

5.2.1 ANA_REG5 Register

Table 5-2 ANA_REG5 Register

Bit	Name	Type	Contents	Default
6	PD_AVCCDET	R/W	Disable AVCC low-voltage detection module. 0:enable 1:disable	0

5.2.2 ANA_REG6 Register

Table 5-3 ANA_REG6 Register

Bit	Name	Type	Contents	Default
7	BATRTCDISC	R/W	Discharge BATRTC for RTC. The resistance of discharge is 1.7k, the current of discharge is Vbatrtc/1.7k. 0: Prohibited using 1.7k ohmic resistance from BATRTC to GND. 1: Enable 1.7k ohmic resistance from BATRTC to GND.	0

5.2.3 ANA_REG7 Register

Table 5-4 ANA_REG7 Register

Bit	Name	Type	Contents	Default
7:3	-	R/W	Reserved.	0
2	VDCINHYSSEL	R/W	VDCIN pin voltage detection hysteresis selection. 0:100mV 1:200mV	0
1:0	-	R/W	Reserved.	0

5.2.4 ANA_REG8 Register

Table 5-5 ANA_REG8 Register

Bit	Name	Type	Contents	Default
3:0	-	-	Reserved.	0
6:4	VDDPVDSEL[2:0]	R/W	VDD voltage alarm threshold register. When VDD voltage is less than the setting value, VDDALARM interrupt flag bit 1. 000:4.5V 001:4.2V 010:3.9V 011:3.6V 100:3.2V 101:2.9V 110:2.6V 111:2.3V	0
7	AVCCLDOPD	R/W	0: enable LDO, AVCC pins voltage is 3.3V. 1: disable LDO, AVCC pins connect to VDD throuth a switch. The switch resistance please refer to **Table** 1-4. Only when input voltage of VDD pins are lower than 3.6V, we can disable AVCCLDO.	0

5.2.5 ANA_REG9 Register

Table 5-6 ANA_REG9 Register

Bit	Name	Type	Contents	Default
7	VDDDETPD	R/W	The switch control for VDD voltage detection module(VDDALARM). The module is powered by VDD. 0:enable, the module cannot be controlled by hardware. 1:disable, the module can be enabled by hardware, the details please refer to the bit22~23 of ANA_CMPCTL.	0

5.2.6 ANA_REGA Register

Table 5-7 ANA_REGA Register

Bit	Name	Type	Contents	Default
6:0	-	R/W	Reserved.	Default value 0x0, must set 0x02
7	VDCINDETPD	R/W	The switch for VDCIN detection module. 0:enable VDCIN detection 1:disable VDCIN detection	0

5.2.7 ANA_REGF Register

Table 5-8 ANA_REGF Register

Bit	Name	Type	Contents	Default
2	AVCCO_EN	R/W	AVCC_OUT pins output enable control. 0:high resistance 1: AVCC_OUT outputs AVCC, it can drive the small power module.	0

5.2.8 ANA_CTRL Register

Table 5-9 ANA_CTRL Register

Bit	Name	Type	Contents	Default
26	PDNS2	R/W	When the bit controlling VDDALARM 0 (meanwhile, consider the setting of PDNS), enters in deep sleep mode. 0: When VDDALARM is 0, it does not enter in deep sleep mode. When VDDALARM is 1, system enters in deep sleep mode; meanwhile, when VDDALARM	0x0

			changes to 0, system will automatically wake up from deep sleep mode. 1: VDDALARM is not the condtion of deep sleep mode.	
6	PDNS	R/W	The bit controls the beahavior of entering the deep sleep mode when VDCINDROP is 0 (while considering the PDNS2 settings). 0: When VDCINDROP is 0, it does not enter in deep sleep mode. When VDCINDROP is 1, system enters in deep sleep mode; meanwhile, when VDCINDROP changes to 0, system will automatically wake up from deep sleep mode. 1: VDCINDROP is not the condtion of deep sleep mode.	0x0

5.2.9 ANA_CMPOUT Register

Table 5-10 ANA_CMPOUT Register

Bit	Name	Type	Contents	Default
10	AVCCLV	R	AVCC low-voltage status. Hysteresis voltage is 20mV~30mV. 0:AVCC is higher than 2.5V. 1:AVCC is lower than 2.5V.	0x0
8	VDCINDROP	R	VDCIN power down status bit. 0:VDCIN did not power down (VDCIN is greater than threshold.) 1:VDCIN power down (VDCIN is smaller than threshold.)	0x0
7	VDDALARM	R	VDD voltage alarm status. 0:VDD voltage is higher then the setting voltage of VDDPVDSEL. 1:VDD voltage is lower than the setting voltage of VDDPVDSEL.	0x0

5.2.10 ANA_INTSTS Register

Table 5-11 ANA_INTSTS Register

Bit	Name	Type	Contents	Default

11	INTSTS11	R/C	When VDCINDROP is 0, it enters in interrupt flag bit of sleep mode (VDCIN is greater than threshold.) When VDCINDROP is 0 and detects that entered in sleep mode, it will set the interrupt flag bit. User also can enable the interrupt bit (INTEN11) to wake up from sleep mode or deep sleep mode (VDCINDROP is 0.) Read 0: no sleep event occurs (VDCINDROP=0) Read 1: the sleep mode event occured (VDCINDROP=0) Write 0: no effect Write 1: clear the bit	0x0
10	INTSTS10	R/C	The interrupt flag bit of AVCCLV. The interrupt event willoccur when AVCCLV rising or falling. Read 0: no AVCCLV interrupt Read 1: AVCCLV interrupt occurs Write: invalid Write 1: clear the bit	0x0
8	INTSTS8	R/C	The interrupt flag bit of VDCINDROP. The interrupt event will occur during VDCINDROP rising or falling. Read 0: no VDCIN interrupt Read 1: VDCIN interrupt occurs Write 0: invald Write 1: clear the bit	0x0
7	INTSTS7	R/C	The interrupt flag bit of VDDALARM. The interrupt event will occur when VDDALARM rising or falling. Read 0: no VDDALARM interrupt Read 1: VDDALARM interrupt occurs Write 0: invalid Write 1: clear the bit	0x0

5.2.11 ANA_INTEN Register

Table 5-12 ANA_INTEN Register

Bit	Name	Type	Contents	Default
11	INTEN11	R/W	When VDCINDROP is 0, an action to enter sleep mode is detected, and the interrupt and wake-up enable control of this event. 0: When VDCINDROP is 0, sleep mode is detected, the interrupt or wake-up is disabled. 1: When VDCINDROP is 0, sleep mode is detected, the interrupt or wake-up is enabled.	0x0
10	INTEN10	R/W	AVCCLV interrupt or wake-up enable control. 0: disable AVCCLV interrupt or wake-up. 1: enable AVCCLV interrupt or wake-up.	0x0
8	INTEN8	R/W	VDCINDROP interrupt or wake-up enable control. 0: disable VDCIN interrupt or wake-up. 1: enable VDCIN interrupt or wake-up.	0x0
7	INTEN7	R/W	VDDALARM interrupt or wake-up enable control. 0: disable VDDALARM interrupt or wake-up. 1: enable VDDALARM interrupt or wake-up.	0x0

5.2.12 ANA_CMPCTL Register

Table 5-13 ANA_CMPCTL Register

Bit	Name	Type	Contents	Default
31:24	PWR_DEB_SEL	R/W	The digital filtering control register of VDDALARM, VDCIN and AVCCDET. 0:no filter. 1:2 x RTCCLK clock filter. 2:3 x RTCCLK clock filter. 3:4 x RTCCLK clock filter. 4:5 x RTCCLK clock filter. … 255:256 x RTCCLK clock filter.	0x00
23:22	VDDALARM_CHK_FRQ_SEL	R/W	VDDALARM detects hardware intermittent turn-on control. When bit7 of ANA_REG9 is	0x0

			configured as 1, the hardware control takes effect. 0:Never enable, no detection 1:With RTCCLK clock frequency, always enable the detection. 2:The test is enabled every 7.8125ms, and it is automatically disabled after the test is completed.	

5.3 AVCC

In V85XXP, the analog circuit is powered by AVCC. AVCC is controlled via the control bit AVCCLDOPD (ANA_REG8 bit7). Only when the input voltage of VDD is lower than 3.6V, user can disable AVCCLDO.

The driving capability of AVCC is 30mA.

AVCC_OUT is a controllable AVCC power output pin. Through the control bit AVCCOEN (ANA_REGF bit2), it can disable and default pins output. The driver capacity of AVCC_OUT is 20mA, but if AVCC and AVCC_OUT is driving at the same time, the driving current cannot over 30mA.

There are designing a voltage detection module for AVCC. When AVCC voltage is lower than 2.5V, it will generate a interrupt.

The pin external of AVCC needs to be connected the decoupling capacitor. It is recommended to use a 10uF capacitor in parallel with a 0.1uF capacitor.

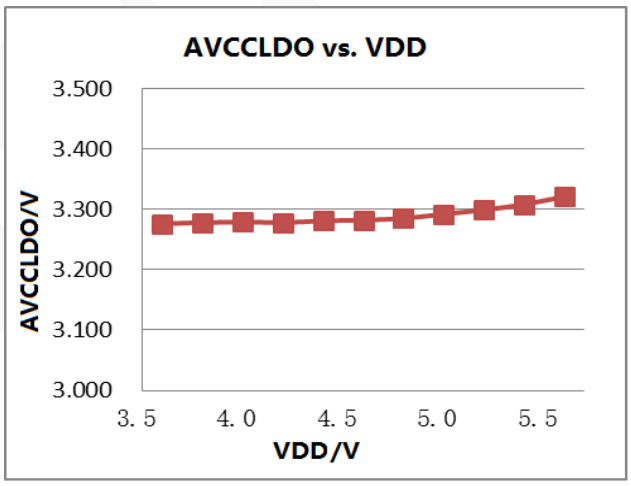


Figure 5-2 The Revelant between AVCCLDO Output Voltage and VDD Input Voltage

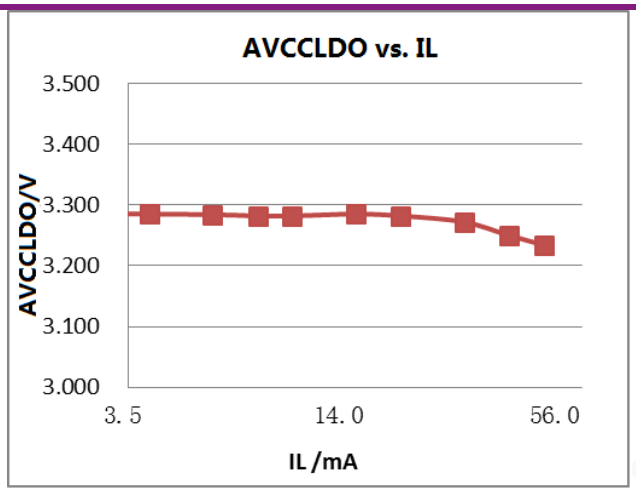


Figure 5-3 The Revelant between AVCCLDO Output Voltage and Load Current

5.4 DVCC

In V85XXP, PLL and digital circuit are powered by DVCC. When DVCC input voltage is greater than 1.7V, DVCC will output the steady voltage 1.5V.

The driving capacity of DVCC is 35mA. When the load current is smaller than or equal to 35mA, power output and steady voltage; when the load current is greater than 35mA, the higher load current, the lower digital power.

DVCC always works except the whole chip power-down.

The pin external of DVCC needs to be connected the decoupling capacitor. We suggest connecting a 10uF with a 0.1uF capacitor.

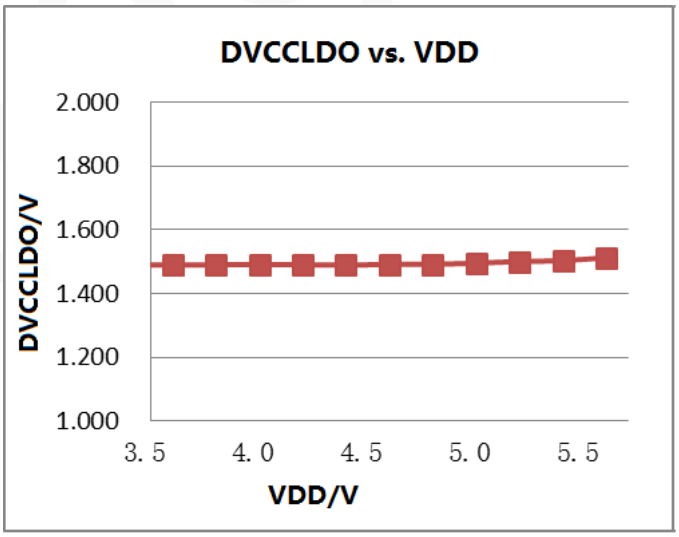


Figure 5-4 The Revelant between DVCCLDO Output Voltage and VDD Input Voltage

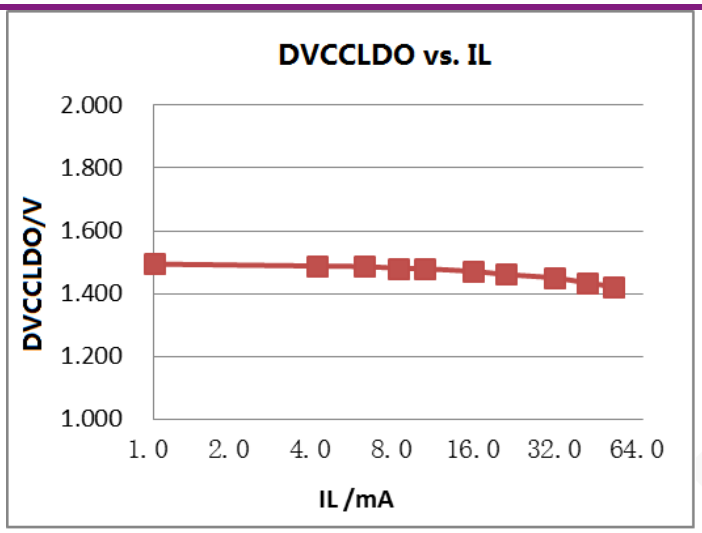


Figure 5-5 The Revelant between DVCCLDO Output Voltage and Load Current

5.5 Power Monitor

5.5.1 VDCIN Power Monitor

In V85XXP, the main power resistance is divided into VDCIN pin. The power detection system will continue detect voltage of VDCIN pin. When VDCIN voltage is lower than 1.0V, the flag bit VDCINDROP (ANACMP_OUT bit8) will be set to 1 and a powered-down interrupt will be generated. VDCINDROP will continue to be1until the voltage returning to 1.1V or 1.2V above, and the hysteresis can be configured through VDCINHYSSEL (ANA_REG7 bit2).

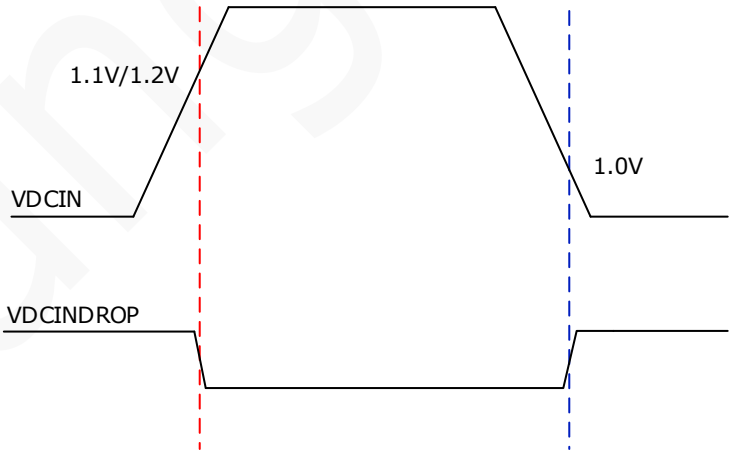


Figure 5-6 The Relevant of VDCIN Pin Signal Input and VDCINDROP

5.5.2 VDD Power Detection

The power detection module monitors the input voltage of VDD. When the voltage of VDD is lower than the threshold value (the voltage set by VDDPVDSEL<2:0> in register ANA_REG8), the detection module will issue a warning interrupt to the MCU.

VDDPVDSEL<2:0>	Voltage Alarm Threshold Configuration	000:4.5V 001:4.2V 010:3.9V 011:3.6V 100:3.2V 101:2.9V 110:2.6V 111:2.3V

5.5.3 AVCC Power Detection

The low-voltage detection module detects the low-voltage status of AVCC. When AVCC voltage is lower than 2.5V, AVCC detection module will generate a low-voltage interrupt signal for MCU; meanwhile, the accuracy of ADC will significantly reduced, so do not use ADC to catch any signal.

5.6 Power Switch

5.6.1 Power Switch 1

The power switch 1 is used to select the input source of RTC between VDD and BATRTC. When VDD is higher than the voltage of the RTC battery BATRTC, the power switch will select VDD as the power supply for RTC, otherwise, select BATRTC as the power supply for RTC.

5.6.2 Power Switch 2

Power switch 2 is used to choose the input source of AVCC. When AVCCLDOPD(ANA_REG8 bit 7) is 0, the input source of AVCC is the output of AVCCLDO, and the voltage 3.3V; when AVCCLDOPD(ANA_REG8 bit 7) is 1, AVCC pin connects VDD through a switch, and the switch resistance please refer to **Table 1-4**. Only when the input voltage of VDD is lower than 3.6V, user can disable AVCCLDO.

5.7 Application Note

Dual Power Supply: VDD is powered by one source, BATRTC is powered by another.

Single Power Supply: VDD, BARRTC pins are connected to the single power supply.

6. Operating Mode

6.1 Introduction

PMU controller (Power Management Unit, PMU) is used to control V85XXP sleep mode and deep sleep mode. PMU controller supports up to 16 external IO wake-up sources to wake chips up from sleep mode or deep sleep mode.

Some peripherals will be turned off in sleep mode, and only CPU, SRAM, GPIO, RTC, analog controller, PMU and UART32K modules will work in this mode. .

Some peripherals will be turned off in deep sleep mode with CPU and others (including FLASH, SRAM, LCD controller and GPIOB~GPIOF.) Only GPIOA, RTC, analog controller, PMU and UART32K modules will work in this mode.

RTC ONLY mode is configured the power-down CPU and others for peripherals, including FLASH, SRAM, LCD controller, GPIO, analog controller, PMU and UART32K modules. Only RTC will work in this mode.

6.2 Features

The entry and exit of the deep sleep mode is controllable, and the corresponding module is reset after woke up from deep sleep mode. The program starts to run from address 0.

--The entry and exit of the light sleep mode is controllable. After it woke up from sleep mode, MCU enters the corresponding wake-up source to interrupt the service function. After the interrupt event response is completed, it returns to the main program and continues running.

--Password protection to avoid entering the deep sleep mode in unexpected events.

--16 GPIOs with wake-up and interrupt functions.

--The clock will be automatically disabled when entering sleep and deep sleep mode, and the system clock before sleep will be automatically enabled after woke up from sleep mode; the RCH clock will be automatically enabled after woke up from deep sleep mode.

--Crystal damage detection and interruption.

--Embedded 256 bytes SRAM can preserve essential data in deep sleep mode.

--Automatically enable watchdog after woke up from deep sleep mode or sleep mode.

6.3 Functional Diagram

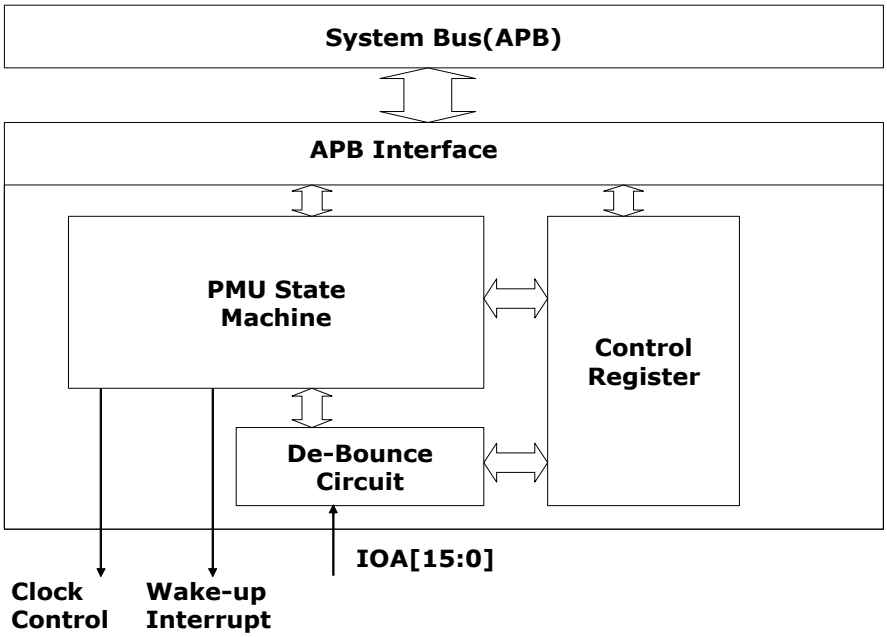


Figure 6-1 Functional Diagram of PMU Controller

6.4 Register Address

Table 6-1 PMU Register Address for Operating Mode (PMU Base Address:0x40014000)

Name	Type	Address	Contents	Default
PMU_DSLEEPEN	R/W	0x0000	PMU deep sleep enable register	0x00000000
PMU_DSLEEPPASS	R/W	0x0004	PMU deep sleep passwords register	0x00000000
PMU_CONTROL	R/W	0x0008	PMU control register	0x00000000
PMU_STS	R/C	0x000C	PMU status register	0x00000074

Table 6-2 PMU RAM Retention Register Address (PMU Retention RAM Base Address:0x40014400)

Name	Type	Address	Contents	Default
PMU_RAM0	R/W	0x0000	PMU32 retention RAM0	--
PMU_RAM1	R/W	0x0004	PMU32 retention RAM1	--
PMU_RAM2	R/W	0x0008	PMU32 retention RAM2	--
…	…	…	…	--
PMU_RAM63	R/W	0x00FC	PMU32 retention RAM63	--

Table 6-3 ANA Register Address (Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000

6.5 Register Definition

6.5.1 PMU_DSLEEPEN Register

In order to enable the deep-sleep mode, user should first write passwords 0xAA5555AA to PMU_DSLEEPPASS register, then write 0x55AAAA55 to PMU_DSLEEPEN register. When in the debug mode (mode is 0), it is not allowed to enter deep sleep or sleep mode, and all values which wrote in PMU_DSLEEPEN register will be discarded. If the chip is in the deep sleep mode and the MODE pin changes from 1 to 0, it will automatically wake-up, reset and enable the access of ICE interface.

Table 6-4 PMU_DSLEEPEN Register

Bit	Name	Type	Contents	Default
31	WKU	R	Currently wake-up signal status. If it is 1, it is inidicated that there is a wake-up signal that has not been cleared. User should clear the interrupt flag bit to ensure that the bit 0 before entering the deep sleep mode. Otherwise, system will wake up immediately because the wake-up events is not cleared.	0x0
30:0	-	-	Reserved.	0

6.5.2 PMU_DSLEEPPASS Register

Table 6-5 PMU_DSLEEPPASS Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0
0	UNLOCK	R	This bit indicates that the deep sleep mode entry has been unlocked and is ready to enter the deep sleep mode. To unlock the deep sleep mode, user should write 0xAA5555AA to the register. This bit will be cleared immediately after any register read or PMU register wrote, including ICE read/write. Therefore, user should immediately set the correct password in PMU_DSLEEPEN.	0x0

6.5.3 PMU_CONTROL Register

Table 6-6 PMU_CONTROL Register

Bit	Name	Type	Contents	Default
31:21	-	-	Reserved.	0
20	FORCE_CLKSEL_RCH		Wake-up clock selection for idle mode 0:Same as idle mode before 1:RCH	0x0
19:16	-	-	Reserved.	0
15:8	PWUPCYC	R/W	Power-up cycle count. The register control the power-up wating time during receiving wake-up. Suggest to configure 0.	0x0
7:6	-	-	Reserved.	0
5	PLLL_SEL	R/W	Low-speed PLL input clock selection. 0:32K XTAL 1:32K RC	0x0
4	PLLH_SEL	R/W	High-speed PLL input clock selection. 0:6.5MHz RC 1:6.5536MHz XTAL	0x0
3	INT_6M_EN	R/W	6.5536M XTAL fail interrupt enable control bit. The bit is used to control the interrupt signal output to CPU. After the bit is set to 1, if the 6.5536M crystal oscillator is removed or damaged, an interrupt will be issued to the CPU.	0x0
2	INT_32K_EN	R/W	32K XTAL fail interrupt enable control bit. The bit is used to control the interrupt signal output to CPU. After this bit is set to 1, if the 32K crystal is removed or damaged, an interrupt will be issued to CPU. If this event occurs during the sleep mode, CPU will be woke-up.	0x0
1	RTCCLK_SEL	R/W	RTC clock selection. 0:32K XTAL 1:32K RC	0x0
0	INT_IOA_EN	R/W	IOA0~15 disable the control bit, it is used to set the enable control for external wake-up IO.	0x0

6.5.4 PMU_STS Register

Table 6-7 PMU_STS Register

Bit	Name	Type	Contents	Default
31:25	-	-	Reserved.	0
24	MODE	R	The bit shows currently status of MODE. 0:debug mode 1:not debug mode	--
23	-	-	Reserved.	0
22	WKUMODE	R	This register is used to indicate if the previous wake-up source from deep-sleep mode is MODE pin change from 1 to 0. This bit will be cleared to 0 as long as the entry of deep-sleep mode.	
21	-	-	Reserved.	--
20	WKUXTAL	R	This register is used to indicate if the previous wake-up source from deep-sleep mode is crystal osciallator detection module. This bit will be cleared to 0 as long as the entry of deep-sleep mode.	--
19	WKUU32K	R	This register is used to indicate if the previous wake-up source from deep-sleep mode is UART32K module. This bit will be cleared to 0 as long as the entry of deep-sleep mode.	--
18	WKUANA	R	This register is used to indicate if the previous wake-up source from deep-sleep mode is analog module. This bit will be cleared to 0 as long as the entry of deep-sleep mode.	--
17	WKURTC	R	This register is used to indicate if the previous wake-up source from deep-sleep mode is RTC module. This bit will be cleared to 0 as long as the entry of deep-sleep mode.	--
16	WKUIOA	R	This register is used to indicate if the previous wake-up source from deep-sleep mode is IOA module. This bit will be cleared to 0 as long as the entry of deep-sleep mode.	--
15:11	-	-	Reserved.	

10	MODERST	R/C	This register indicates that in sleep or deep sleep mode, MODE wake-up and reset due to pins change from high to low. User can read this bit to know if this reset source is the mode wake-up reset. Write 1 to clear the bit.	--
9	-	-	Reserved.	
8	SFTRST	R/C	This register indicates that a soft reset has happened. User can read this bit to know if this reset source is the soft reset. Write 1 to clear the bit.	--
7	WDTRST	R/C	The register indicates that the WDT reset. User can read this bit to know if this reset source is the WDT reset. Write 1 to clear the bit.	--
6	DPORST	R/C	This bit indicated if the last reset is caused by internal digital power-on reset signal. It will be set only when the power is enabled for the first time (BATRTC is also discharged). Write 1 to clear the bit.	0x1
5	PORST	R/C	This bit indicated if the last reset was PORH reset or PORL reset. PORHis a reset that occurs when AVCCLDO voltage is lower than 2.08V; PORL is a reset that occurs when DVCCLDO voltage is lower than 1.3V. Write 1 to clear the bit.	0x1
4	EXTRST	R/C	This bit indicated if the last reset is caused by external reset signal. Write 1 to clear the bit.	0x1
3	EXIST_6M	R	6.5536M XTAL has status register. This bit indicates the presence or absence of 6.5536M XTAL. After 6.5536M XTAL is enabled (BIT7 of ANA_REG3 to set 1), the bit will be refreshed; otherwise, the previous status will be maintained. 0: 6.5536M crystaldoes not exist 1: 6.5536M crystal exists	0x0
2	EXIST_32K	R	32K XTAL exists in the status register. This bit indicates the presence or absence of 32K XTAL. 0: 32K crystal does not exist 1: 32K crystal exists	0x1

1	INT_6M	R/C	This bit indicates the failure interrupt status of the 6.5536M crystal oscillator. When the EXIST_6M status bit changes from 1 to 0, the status bit set 1. When the bit set 1, it represents that the 6.5536M crystal is removed or damaged. Write 1 to clear the bit.	0x0
0	INT_32K	R/C	This bit indicates the failure interrupt state of the 32K crystal oscillator . When the EXIST_32K status bit changes from 1 to 0, the status bit set 1.When the bit set 1, it represents that the 32K crystal is removed or damaged. Write 1 to clear the bit.	0x0

6.5.5 ANA_CTRL Register

Table 6-8 ANA_CTRL Register

Bit	Name	Type	Contents	Default
26	PDNS2	R/W	This bit controls the behavior of entering deep sleep mode when VDDALARM is 0 (while considering the setting of PDNS). When VDDALARM is 0, it will not enter the deep sleep mode. When VDDALARM is 1, the system can enter the deep sleep mode, and when VDDALARM becomes 0, the system automatically wakes up from deep sleep mode. 1: VDDALARM is not used as the deep sleep condition.	0x0
6	PDNS	R/W	The bit controls the behavior of entering the deep sleep mode when VDDALARM is 0 (while considering the setting of PDNS2.) 0: When VDDALARM is 0, it will not enter in the deep sleep mode. When VDDALARM is 1, system will enter in deep sleep mode; meanwhile, when VDCINDROP changes to 0, system automatically wakes up from deep sleep mode. 1: The value of VDCINDROP is not used as the condition of entering deep sleep mode.	0x0

6.5.6 PMU_RAMx Register

Table 6-9 PMU_RAMx Register

Bit	Name	Type	Description	Default
31:0	RAM	R/W	There is a 256 bytes (64x32) SRAM is embedded in the PMU controller. This RAM can retain data in deep-sleep mode. Only word access is allowed to these ports.	--

6.6 Reset

When the chip changes from one working mode to another, some of the hardware module will be reset automatically, the following table shows the reset details of each module.

Table 6-10 The Reset Conditions of Each Module Under Different Evvents or Wake-up from Sleep Mode

Module	External Reset	Power-on Reset	Watchdog Reset	M0 Soft Reset MODE		Exit RTC only mode	Before Wake-up Mode		
				High	Low		Deep Sleep	Sleep	IDLE
Cortex-M0	√	√	√	√	√	√	√	-	-
System SRAM	-	-	-	-	-	Data lost	Data lost	-	-
Retention SRAM	-	-	-	-	-	Data lost	-	-	-
PMU(IOA)	√	√	√	-	√	√	-	-	-
WDT	√	√	√	-	√	√	-	-	-
RTC	√*	√*	√*	-	√*	√*	-	-	-
UART32K0	√	√	√	-	√	√	-	-	-
UART32K1	√	√	√	-	√	√	-	-	-
Analog Controller	√	√	√	-	√	√	-	-	-
LCD	√	√	√	√	√	√	√	-	-
GPIO(IOB~IOF)	√	√	√	√	√	√	√	-	-
MISC2	√	√	√	√	√	√	√	-	-
MISC	√	√	√	√	√	√	√	√	-
I2C	√	√	√	√	√	√	√	√	-

SPI	√	√	√	√	√	√	√	√	-
UART	√	√	√	√	√	√	√	√	-
ISO7816	√	√	√	√	√	√	√	√	-
TIMER	√	√	√	√	√	√	√	√	-
PWM	√	√	√	√	√	√	√	√	-
DMA	√	√	√	√	√	√	√	√	-
SRAM Controller	√	√	√	√	√	√	√	√	-
FLASH Controller	√	√	√	√	√	√	√	√	-

Note (√*):RTC registers with write protection will not be reset by the three reset sources of the external reset, power-on reset or watchdog reset. Other RTC registers can be reset by these three wake-up sources. Under the different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables show the detail of clock status under the different mode.

Table 6-11 Clock Operating Status under the Different Mode

Clock Source	Power Mode				
	RTC only	Deep Sleep	Sleep	IDLE	Active
6.5536M RC	OFF	OFF	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	ON	
32K XTAL	ON	ON	ON	ON	

Clock Source	Exit RTC only mode	Wake up from different mode		
		Deep Sleep	Sleep	IDLE
6.5536M RC	OFF	ON	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	
32K XTAL	ON	ON	ON	

6.6.1 External Reset

The external reset pin (EXTRSTN) can reset most of module in V85XXP, the detail information please refer to **Table 6-10**. To avoid external noise from coupling into this pin, a de-glitch circuit is embedded V85XXP. The following diagram shows the working principle of de-glitch circuit. When RTCCLK prescaler is set to a non-zero value, the deglitch time will be increased accordingly. For example, when RTCCLK prescaler is set to 1/4, the de-glitch time will be increased to 91*4=364μs.

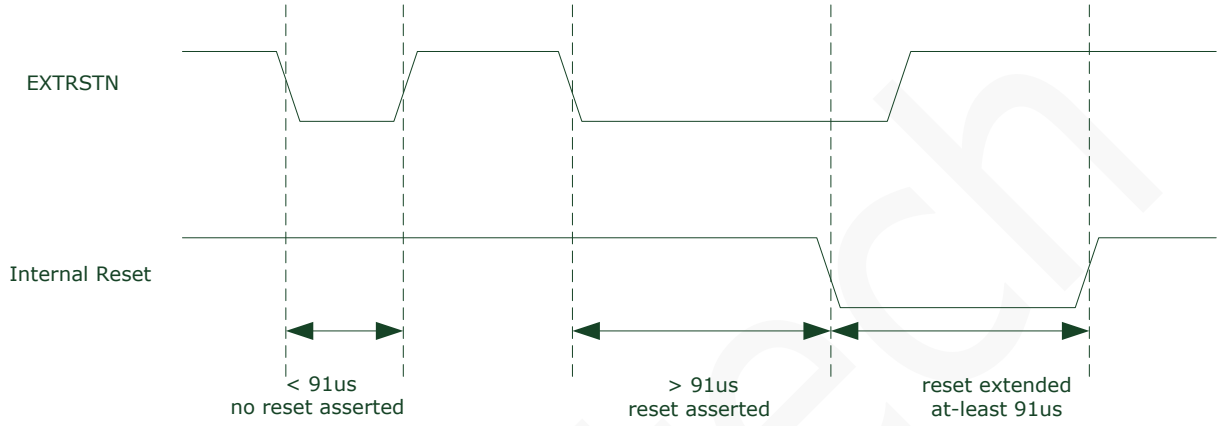


Figure 6-2 External Reset De-glitch Timing

6.6.2 Watchdog Timer (WDT) Reset

The level of watchdog timer reset is the same as power on reset, which provides the internal reset mechanism of the chip.

6.6.3 Power-on reset (POR)

Power-on reset (POR) provides the internal reset mechanism of chips which cooperates with external reset.

6.6.4 M0 Soft Reset

M0 soft reset instruction can reset most of V85XXP modules. The detail information please refer to **Table 6-10**.

6.6.5 Wake Up from Sleep/Deep Sleep/IDLE

Any interrupt can wake up the chip from IDLE state. Some of them can wake up chips from sleep mode, and some of them can wake up chips from deep sleep mode.

Table 6-12 Interrupt Source

Item	Vector Address	Interrup tNumber	Description	Enable bit of peripheral event	Flag of peripheral event	Before Wake-up Source	
						Deep	Sleep

						Sleep	
NMI	00000008h	-14	NMI				
HardFault	0000000Ch	-13	HardFault				
SVCall	0000002Ch	-5	SVCall				
PendSV	00000038h	-2	PendSV				
SysTick	0000003Ch	-1	SysTick				
PMU	00000040h	0	IOA0~15	PMU_CONTROL.0and PMU_IOAWKUEN.0~15	PMU_IOAINTSTS.0~15	√	√
			32K crystal disable	PMU_CONTROL.2	PMU_STS.0	√	√
			6M crystal disable	PMU_CONTROL.3	PMU_STS.1		
RTC	00000044h	1	ITV and SITV interrupt	RTC_INTEN.0	RTC_INTSTS.0	√	√
			Illegal time format	RTC_INTEN.1	RTC_INTSTS.1	√	√
			Multi-second interrupt	RTC_INTEN.2	RTC_INTSTS.2	√	√
			Multi-minute interrupt	RTC_INTEN.3	RTC_INTSTS.3	√	√
			Multi-hour interrupt	RTC_INTEN.4	RTC_INTSTS.4	√	√
			Mid-night (00:00) interrupt	RTC_INTEN.5	RTC_INTSTS.5	√	√
			32K counter interrupt	RTC_INTEN.6	RTC_INTSTS.6	√	√
			Illegal write in CE register	RTC_INTEN.8	RTC_INTSTS.8		
			Alarm interrupt	RTC_INTEN.10	RTC_INTSTS.10	√	√

U32K0~1	00000048h 0000004Ch	2\3	Receive data	U32Kx_CTRL1.0	U32Kx_STS.0	√	√
			Receive parity error	U32Kx_CTRL1.1	U32Kx_STS.1	√	√
			Receive buffer overrun	U32Kx_CTRL1.2	U32Kx_STS.2	√	√
I2C	00000050h	4	I^2C serial interrupt	I2C_CTRL2.0	I2C_CTRL.3		
SPI1~3	00000054h \000000ACh\ 000000B0h	5\27\28	SPI Transmit	SPIx_TXSTS.14	SPIx_TXSTS.15		
			SPI Receive	SPIx_RXSTS.14	SPIx_RXSTS.15		
UART0~5	00000058h ~0000006Ch	6\7\8\ 9\10\11	Receive Interrupt	UARTx_CTRL.3	UARTx_INTSTS.1		
			Transmit Overrun	UARTx_CTRL.4	UARTx_INTSTS.2		
			Receive Overrun	UARTx_CTRL.5	UARTx_INTSTS.3		
			Receive parity error	UARTx_CTRL.7	UARTx_INTSTS.4		
			Transmit done	UARTx_CTRL.8	UARTx_INTSTS.5		
ISO78160~1	00000070h ~00000074h	12\13	Receive error	ISO7816x_CFG.2	ISO7816x_INFO.2		
			Receive interrupt	ISO7816x_CFG.5	ISO7816x_INFO.5		
			Transmit interrupt	ISO7816x_CFG.6	ISO7816x_INFO.6		
			Receive overrun	ISO7816x_CFG.7	ISO7816x_INFO.7		
			Transmit and reset error	ISO7816x_CFG.8	ISO7816x_INFO.8		

Timer0~3	00000078h ~00000084h	14\15\16\17	Timer overrun	TMRx_CTRL.3	TMRx_INTSTS.0		
PWM0~3	00000088h ~000094h	18\19\20\21	PWM timer overrun	PWMx_CTL.1	PWMx_CTL.0		
			Capture/ compare 0	PWMx_CCTL0.4	PWMx_CCTL0.0		
			Capture/ compare 1	PWMx_CCTL1.4	PWMx_CCTL1.0		
			Capture /compare 2	PWMx_CCTL2.4	PWMx_CCTL2.0		
DMA	00000098h	22	Channel 0 end	DMA_IE.0	DMA_STS.4		
			Channel 1 end	DMA_IE.1	DMA_STS.5		
			Channel 2 end	DMA_IE.2	DMA_STS.6		
			Channel 3 end	DMA_IE.3	DMA_STS.7		
			Channel 0 frame end	DMA_IE.4	DMA_STS.8		
			Channel 1 frame end	DMA_IE.5	DMA_STS.9		
			Channel 2 frame end	DMA_IE.6	DMA_STS.10		
			Channel 3 frame end	DMA_IE.7	DMA_STS.11		
			Channel 0 data abort	DMA_IE.8	DMA_STS.12		
			Channel 1 data abort	DMA_IE.9	DMA_STS.13		
			Channel 2 data abort	DMA_IE.10	DMA_STS.14		
			Channel 3 data abort	DMA_IE.11	DMA_STS.15		

FLASH	0000009Ch	23	Checksum error	FLASH_CTRL.2	FLASH_INTSTS.0		
ANA	000000A0h	24	Manual ADC conversion done	ANA_INTEN.0	ANA_INTSTS.0		
			Automatic ADC conversion done	ANA_INTEN.1	ANA_INTSTS.1		
			CMP1 rising or falling	ANA_INTEN.2	ANA_INTSTS.2	√	√
			CMP2 rising or falling	ANA_INTEN.3	ANA_INTSTS.3	√	√
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INTSTS.7	√	√
			VDCIN rising or falling	ANA_INTEN.8	ANA_INTSTS.8	√	√
			AVCCLV rising or falling	ANA_INTEN.10	ANA_INTSTS.10	√	√
			VDCINDROP =0, the entry of sleep or deep-sleep mode at the same time	ANA_INTEN.11	ANA_INTSTS.11	√	√
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	√	√
			TADC changes over threhosld	ANA_INTEN.13	ANA_INTSTS.13	√	√
			ADC over threshold	ANA_INTEN.14~21	ANA_INTSTS.14~21		

6.7 Working Mode Switch

The following diagram shows the working mode switch and status of V85XXP.

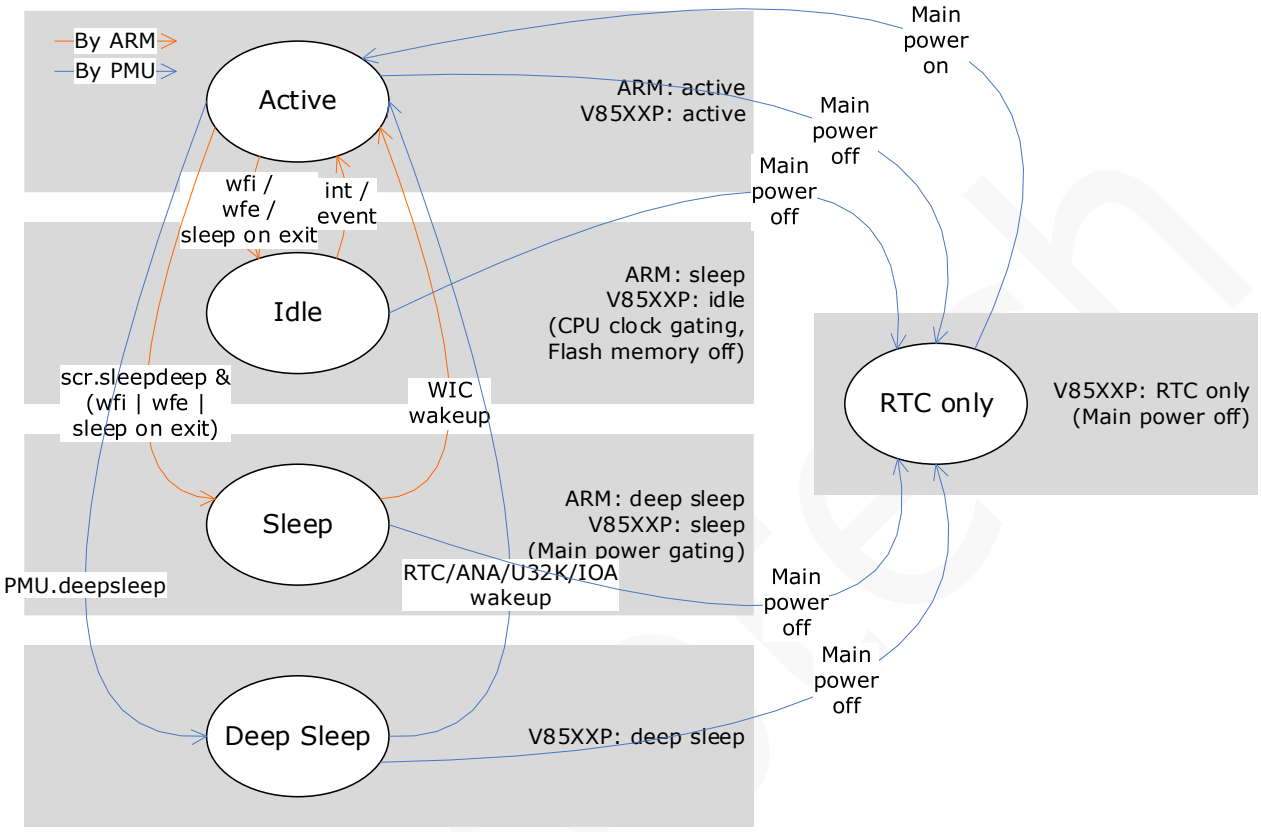


Figure 6-3 V85XXP Working Mode Conversion

According to the diagram above, IDLE or sleep mode is controlled by CPU directly, and user only needs to execute the corresponding instruction (WFI or WFE) to enter these two modes. For deep sleep mode, PMU controller will handle the entry and exit of this mode and it will always return to working mode after wake-up. Corresponded wake-up source must be set before enter the deep sleep mode, this part should be taken by software. The following shows the wake-up source under each mode.

Note:

（1）It should be noted that MCU could enter sleep mode or deep sleep mode only when MODE=1. If MCU execute instruction for entry sleep mode when MODE=0, MCU will enter IDLE mode. Before MCU enter deep sleep mode, user should configure PDNS (ANA_CTRL bit6) and PDNS2 (ANA_CTRL bit24) firstly, or judge the state of VDCINDROP and VDDALRAM. For details, please refer to ANA_CTRL register.

（2）When MCU woke up from sleep mode, MCU will switch the system clock to the setting before entering sleep mode. For example, the system clock is PLLL before enter the sleep mode, the hardware will switch the system clock to PLLL when wake up from sleep mode. When MCU woke up from deep sleep mode, hardware will automatic enable RCH as the system clock. Before or after IDLE mode, hardware does not automatic change the system clock.

（3）When woke up from sleep mode, PLLL locked time is around 1ms, and PLLH locked time is around 15μs.

Table 6-13 Wake-up Source Under Each Working Mode

INT Number	Wake-up Source	Before Wake-up Source		
		Deep Sleep	Sleep	IDLE
Event	-	-	-	-
NMI	SRAM parity error	-	-	√
0	PMU(ExtInt)	√	√	√
1	RTC	√	√	√
2	UART32K0	√	√	√
3	UART32K1	√	√	√
4	I2C	-	-	√
5	SPI1	-	-	√
6	UART0	-	-	√
7	UART1	-	-	√
8	UART2	-	-	√
9	UART3	-	-	√
10	UART4	-	-	√
11	UART5	-	-	√
12	ISO78160	-	-	√
13	ISO78161	-	-	√
14	TIMER0	-	-	√
15	TIMER1	-	-	√
16	TIMER2	-	-	√
17	TIMER3	-	-	√
18	PWM0	-	-	√
19	PWM1	-	-	√
20	PWM2	-	-	√
21	PWM3	-	-	√
22	DMA	-	-	√
23	FLASH	-	-	√

24	ANA	√	√	√
27	SPI2	-	-	√
28	SPI3	-	-	√

6.8 Application Note

6.8.1 External IO Wake-up

All 16 IOAs can wake the system from light sleep or deep sleep mode. There is a debounce circuit in V85XXP to prevent a glitch on the signal from accidentally waking up the system.

The following figure is a schematic diagram of the de-glitch circuit. The de-glitch time is 4 RTCCLK clock cycles. When RTCCLK is not divided (RTC_PSCA=0), anti-interference time is around 122μs. When RTCCLK 4 is divided (RTC_PSCA=1), the de-glitch time will increase to 122*4=488μs. The de-glitch circuit is only valid for IOA edge wake-up signal of sleep and deep sleep mode, but it is invalid for normal interrupts and IOA level wake-up signal in sleep and deep sleep mode.

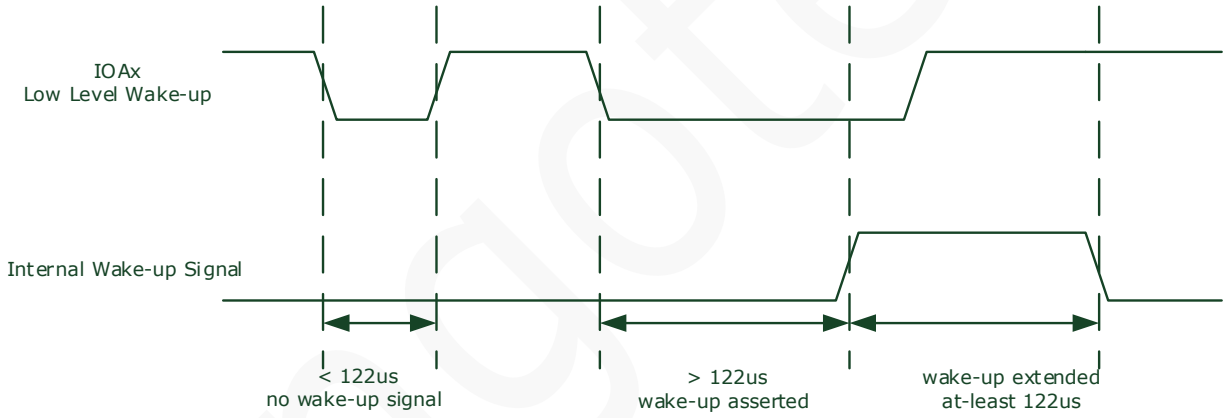
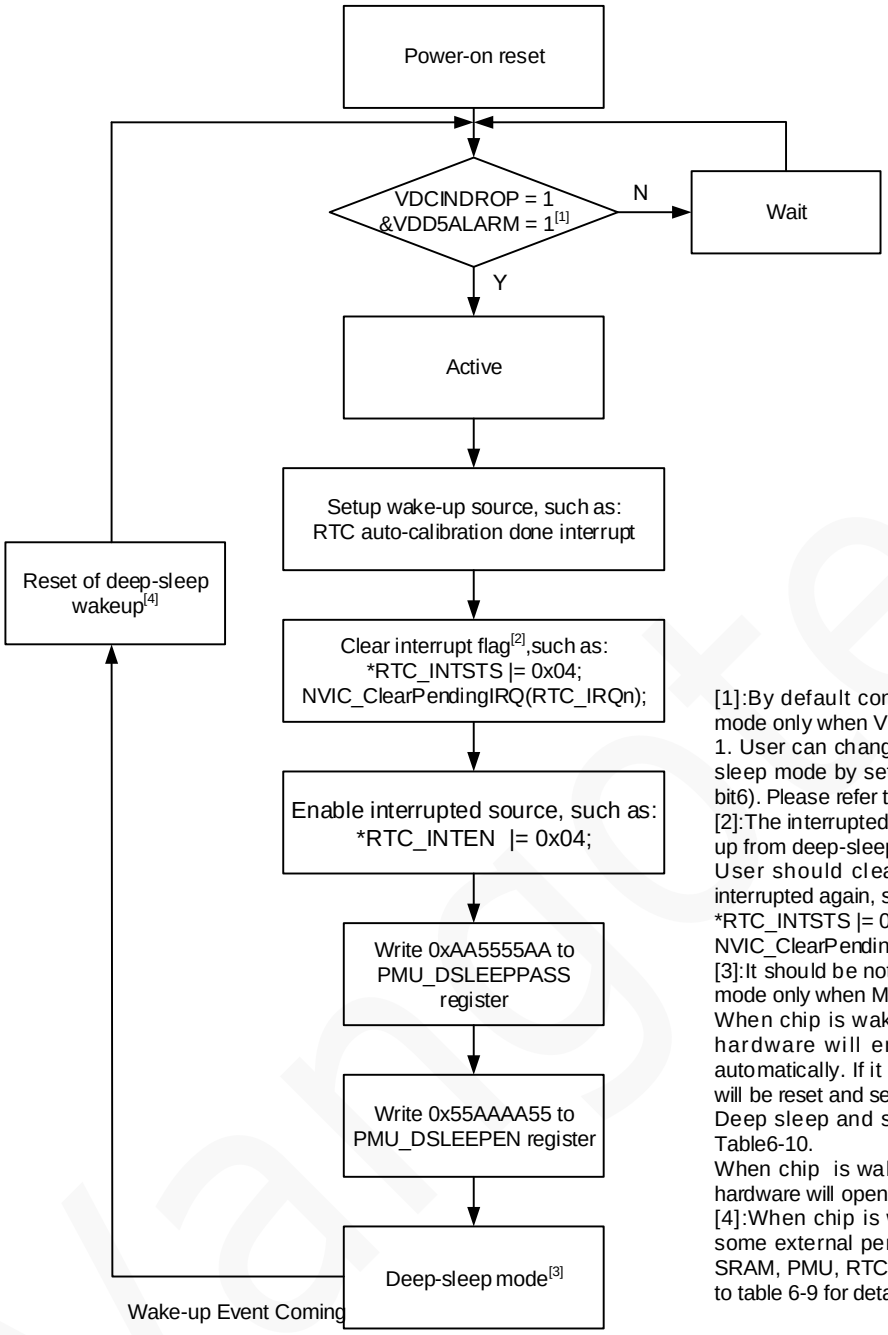


Figure 6-4 External Wake-up Diagram

6.8.2 Deep-sleep Mode Entry Procedure

The following figure shows an example of deep-sleep mode entry procedure.

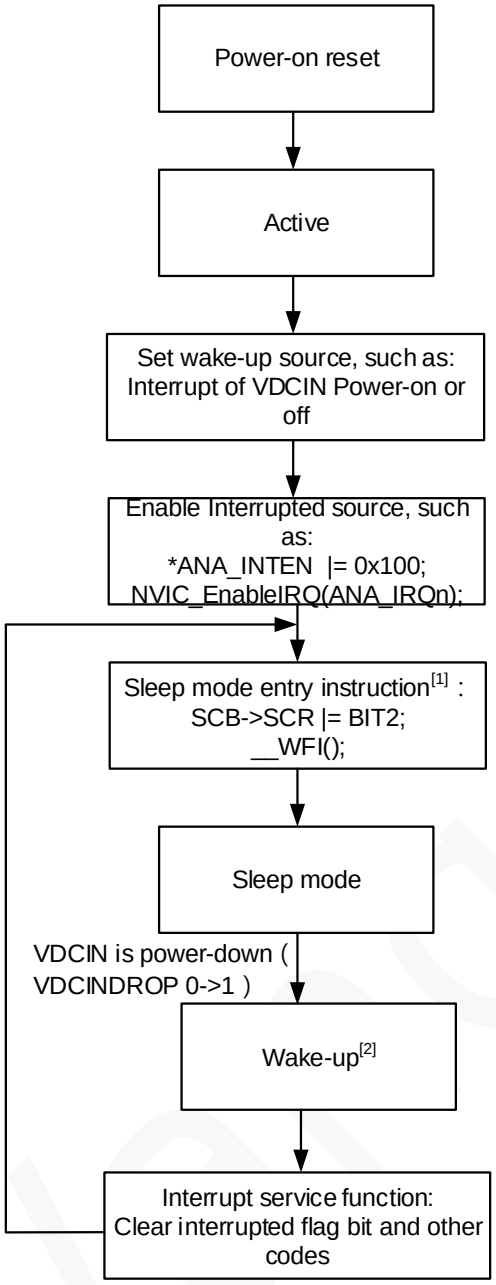


[1]:By default condition, chip can entry deep-sleep mode only when VDDALARM and VDCINROP must be 1. User can change the condition of chip entry deep-sleep mode by setting ANA_CTRL register(bit26 and bit6). Please refer to ANA_CTRL description for details.
[2]:The interrupted flag will be set when MCU is waken up from deep-sleep mode, such as: RTC_INTSTS bit4. User should clear flag bit before enabling NVIC interrupted again, such as:
*RTC_INTSTS |= 0x04;
NVIC_ClearPendingIRQ(RTC_IRQn);
[3]:It should be noted that MCU can enter deep- sleep mode only when MODE=1.
When chip is waken up from deep sleep mode, the hardware will enable the system clock to RCH automatically. If it needs other clock source as RTC, it will be reset and set by software.
Deep sleep and sleep mode status, please refer to Table6-10.
When chip is waken up from deep-sleep mode, the hardware will open watch dog automatically.
[4]:When chip is waken up from deep-sleep mode, some external peripherals will not be reset including SRAM, PMU, RTC, WDT, ANA and so on. Please refer to table 6-9 for details.

Figure 6-5 Dleep Sleep Mode Entry Flow

6.8.3 Sleep Mode Entry Procedure

The following figure shows an example of sleep mode entry procedure.

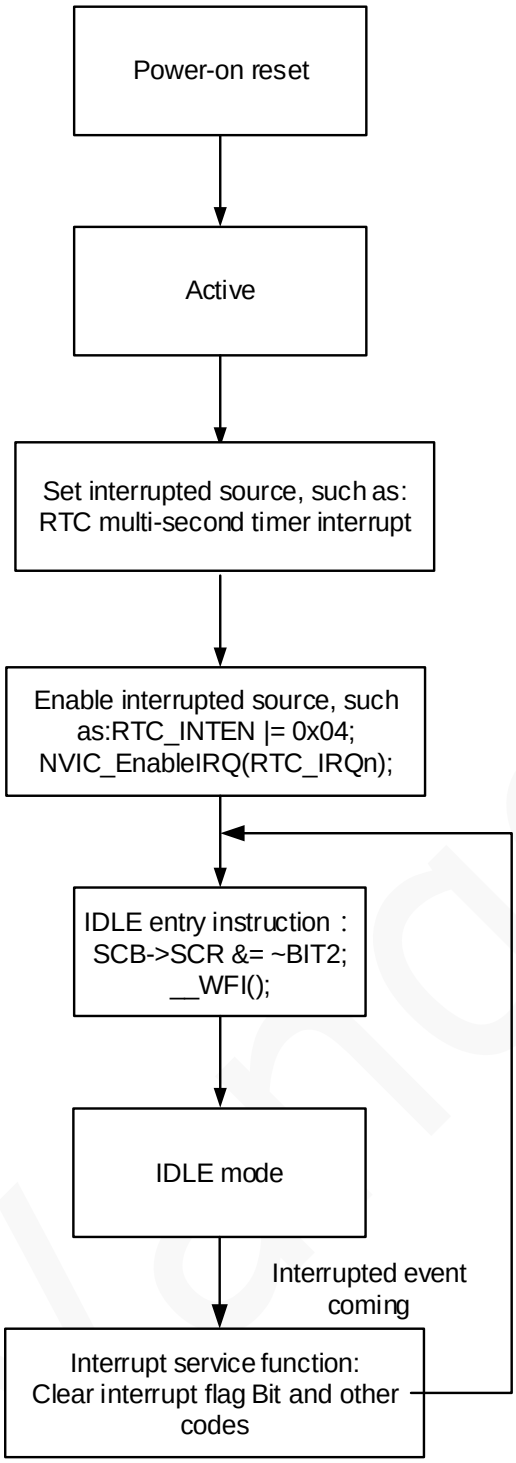


[1]:It should be noted that MCU can enter sleep mode only when MODE=1. If MCU executes instruction for entry sleep mode when MODE=0, MCU will enter IDLE mode.
[2]:When MCU is waken up from sleep mode, some external peripherals will be reset including UART , SPI , I2C and so on, but LCD , GPIO , ANA will not be reset. Please refer to Table 6-9 for details.
When MCU is waken up from sleep mode, hardware will switch the system clock before the state of entry sleep mode. For example, the system clock is PLLL before entering sleep mode, and the hardware will switch the system clock to PLLL when waking up from sleep mode.
The clock status of sleep or after woke up from sleep mode, please refer to Table 6-10 for details.
When MCU woke up from sleep mode, the hard will open watch dog automatically.

Figure 6-6 Sleep Mode Entry Flow

6.8.4 IDLE Mode Entry Procedure

The following figure shows an example of IDLE mode entry procedure.



[1]:Any interrupt source can wake up MCU from IDLE.
Before or after IDLE mode, hardware does not change the system clock automatically.
After woke up from IDLE mode, WDT state is controlled by software.

Figure 6-7 IDLE Mode Entry Flow

7. Clock System

7.1 Introduction

The related settings of the clock system will be reset after the system is reset or wake up from deep sleep mode. After waking up from deep sleep mode, user needs to manually restore the clock-related register settings.

In V85XXP, there are 4 clock sources:

--32K RC oscillator circuit, to generate a 32K RC clock. This circuit is always running and frequency can be trimmed.

--32K crystal oscillator circuit, to generate a 32.768K XTAL clock which is always enabled. 32.768K XTAL clock ismonitored by RTC. When it stops running, 32K RTC will automatically replace it; meanwhile, before RTC running again, the detective circuit will always monitor the crystal oscillator.

--6M RC clock oscillator circuit, to generate a 6.5536M RC clock. User can stop the circuit operation via register settings. The circuit will automatically start running after chips is reset.

--6M crystal oscillator circuit, used to generate 6.5536M crystal oscillator clock. The 6.5536M crystal oscillator clock is disabled by default when power is on, and user needs to manually enable the 6.5536M XTAL clock output.

In V85XXP, there are 3 clock domains:

--HCLK is generated by 6.5536M crystal oscillator clock, 6.5536M RC clock, 32.768K XTAL clock or 32K RC clock or their frequency multiplication. HCLK provides clock for CPU\FLASH\SRAM\DMA\GPIO\LCD\CRYPT.

--PCLK is generated by frequency division of HCLK. PCLK provides clock for low-speed peripherals.

--RTCCLK is generated from 32.768K XTAL clock or 32K RC clock, and it provides clock for RTC\WDT\UART32K\LCD.

Table 7-1 Clock Source Enable or Disable in Different Mode

Clock Source	Power Mode				
	RTC only	Deep Sleep	Sleep	IDLE	Active
6.5536M RC	OFF	OFF	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	OFF	Controlled by PLLLPDN	

32K RC	ON	ON	ON	ON
32K XTAL	ON	ON	ON	ON
Clock Source	**Exit RTC only mode**	**Wake up from different mode**		
		Deep Sleep	**Sleep**	**IDLE**
6.5536M RC	OFF	ON	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	
32K XTAL	ON	ON	ON	

7.2 Features

--Clock control of the submodule;

--Clock divider of AHBCLK and APBCLK;

--Real crystal detection;

The working clock of crystal osciallator detective circuit is 32K RC, to detect the real status of high frequency crystal (default is disable, and enable by manual) and low-frequency crystal status. When 6.5536M XTAL stops running, 6M RC will automatically replace 6.5536M XTAL; meanwhile, after 6.5536M XTAL is restored, 6.5536M XTAL will be used automatically.When 32.768K XTAL stops osciallating, 32K RC will automatically replace 32.768 XTAL; meanwhile, after 32.768K XTAL is restored, 32.768K XTAL will be used automatically. Note: HCLK indicates AHB clock, it also called AHBCLK; meanwhile, PCLK indicates APB clock, it also called APBCLK.

7.3 Functional Diagram

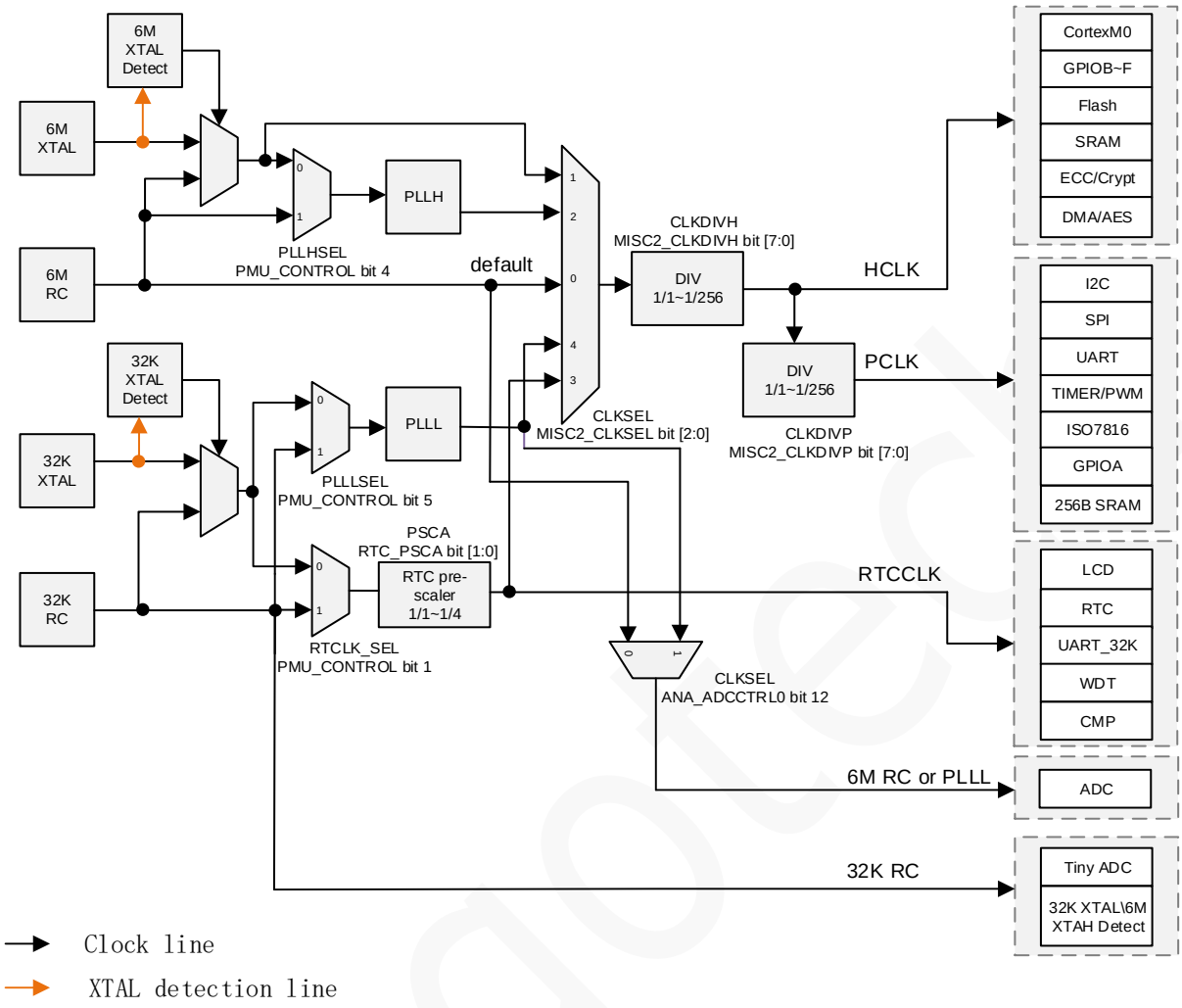


Figure 7-1 V85XXP CLK Functional Diagram

7.4 Register Address

Table 7-2 ANA Register (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REG3	R/W	0x000C	Analog register 3	0x00000000
ANA_REG4	R/W	0x0010	Analog register 4	0x00000000
ANA_REG9	R/W	0x0024	Analog register 9	0x00000000
ANA_REGB	R/W	0x002C	Analog register 11	From FLASH
ANA_REGC	R/W	0x0030	Analog register 12	From FLASH
ANA_CMPOUT	R	0x0054	Comparator result register	0x00000030

Table 7-3 PMU Register (PMU Base Address:0x40014000)

Name	Type	Address	Contents	Default
PMU_CONTROL	R/W	0x0008	PMU control register	0x0000000
PMU_STS	R/C	0x000C	PMU status register	0x0000074

Table 7-4 MISC2 Control Register (MISC2 Base Address:0x40013E00)

Name	Type	Address	Contents	Default
MISC2_CLKSEL	R/W	0x0004	Clock selection register	0x00000000
MISC2_CLKDIVH	R/W	0x0008	AHB CLK divider control register	0x00000000
MISC2_CLKDIVP	R/W	0x000C	APB CLK divider control register	0x00000001
MISC2_HCLKEN	R/W	0x0010	AHB CLK enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB CLK enable control register	0xFFFFFFFF

7.5 Register Definition

7.5.1 ANA_REG3 Register

Table 7-5 ANA_REG3 Control Register

Bit	Name	Type	Contents	Default
3	BGPPD*[1]	R/W	BGP power down control 0:enable BGP 1:disable BGP	0
4	RCHPD	R/W	High frequency RCH(6.5536M RC) enable/disable control signal. 0:enable RCH 1:disable RCH	0
5	PLLLPDN	R/W	PLLL(32768Hz input PLL) enable/disable control signal. 0:disable PLLL 1:enable PLLL	0
6	PLLHPDN	R/W	PLLH(6.5536MHz input PLL) enable/ disable control signal. 0:disable PLLH 1:enable PLLH	0
7	XOHPDN	R/W	6.5536M XTAL clock enable/disable control signal. 0:disable XOH 1:enable XOH	0

*[1]: RCH, PLL, and ADC are related to BGP. Before enabling RCH, PLL, and ADC, BGP must be enabled. If BGP is not used in the system, user can disable BGP through the BGPPD bit; if BGP is used, user cannot disable BGP through BGPPD at this time. Because the system has a protection function and it will enable BGP again. In sleep or deep sleep mode, user can disable BGP regardless of whether it is used.

7.5.2 ANA_REG4 Register

Table 7-6 ANA_REG4 Control Register

Bit	Name	Type	Contents	Default
7:0	-	R/W	Reserved.	Default is 0x00, must set 0x01.

7.5.3 ANA_REG9 Register

Table 7-7 ANA_REG9 Control Register

Bit	Name	Type	Contents	Default

2:0	PLLLSEL[2:0]	R/W	Select CLK frequency of PLLL. 000:26.2144MHz 001:13.1072MHz 010:6.5536MHz 011:3.2768MHz 100:1.6384MHz 101:0.8192MHz 110:0.4096MHz 111:0.2048MHz	0
6:3	PLLHSEL[3:0]	R/W	The CLK frequency control bit of PLLH. PLLH CLK frequency is a multiple of the external XOH or internal RCH. 1000~1011:reserved. 1100:2x input CLK frequency. 1101:2.5x input CLK frequency. 1110:3x input CLK frequency. 1111:3.5x input CLK frequency. 0000:4x input CLK frequency. 0001:4.5x input CLK frequency. 0010:5x input CLK frequency. 0011:5.5x input CLK frequency. 0100:6x input CLK frequency. 0101:6.5x input CLK frequency. 0110:7x input CLK frequency. 0111:7.5x input CLK frequency.	0

7.5.4 ANA_REGB Register

Table 7-8 ANA_REGB Control Register

Bit	Name	Type	Contents	Default
4:0	RCLTRIM[4:0]	R	32kHz RC clock frequency trimming. 00000~01111:increase 4% for each step; 10000~11111:decrease 4% for each step.	0

7.5.5 ANA_REGC Register

Note: User do not modify ANA_REGx register (x=B~E, 10), it can be loaded from FLASH automatically.

Table 7-9 ANA_REGC Control Register

Bit	Name	Type	Contents	Default
5:0	RCHTRIM[5:0]	R	6.5536MHzRC clock frequency trimming. 000000~011111:increase 1.25% for each step; 100000~111111:decrease 1.25% for each step.	0
Note: User do not modify ANA_REGx(x=B~E、10), it can be loaded from FLASH automatically.				

7.5.6 ANA_CMPOUT Register

Table 7-10 ANA_CMPOUT Register

Bit	Name	Type	Contents	Default
1	LOCKL	R	PLLL locked status. The lock time is around 1ms. 0:PLLL is not locked. 1:PLLL is locked.	0x0
0	LOCKH	R	PLLH locked status. The lock time is around 15μs. 0:PLLH is not locked. 1:PLLH is locked.	0x0

7.5.7 PMU_CONTROL Register

Table 7-11 PMU_CONTROL Register

Bit	Name	Type	Contents	Default
5	PLLL_SEL	R/W	Low speed PLL input clock selection. 0:32.768K XTAL 1:32K RC	0x0
4	PLLH_SEL	R/W	High speed PLL input clock selection. 0:6.5MHz RC 1:6.5536MHz XTAL	0x0
3	INT_6M_EN	R/W	6.5536M XTAL failure interruptenable register. The bit is used to control the interrupt signal output to CPU. After the bit is set 1, if 6.5536M crystal oscillator is removed or damaged, an interrupt will be issued to the CPU.	0x0

2	INT_32K_EN	R/W	32.768K XTAL fail interrupt enable register. The bit is used to control the interrupt signal output to CPU. After the bit is set 1, if 32.768K crystal oscillator is removed or damaged, an interrupt will be issued to the CPU.If the event occurs during the sleep mode, CPU will be awakened.	0x0
1	RTCCLK_SEL	R/W	RTC clock selection. 0:32.768K XTAL 1:32K RC	0x0

7.5.8 PMU_STS Register

Table 7-12 PMU_STS Register

Bit	Name	Type	Contents	Default
3	EXIST_6M	R	6.5536M XTAL presence status register. This bit indicates the status(interrrupt) of 6.5536M XTAL. After 6.5536M XTAL is enabled (BIT7 of ANA_REG3 is configured as 1), the status bit will be refreshed, otherwise the previous status will be maintained. 0:6.5536M crystal is absent. 1:6.5536M is present.	0x0
2	EXIST_32K	R	32.768K XTAL presence the status register. This bit indicates the status(interrupt) of 32.768K XTAL. 0:32K crystal is absent. 1:32K crystal is present.	0x1
1	INT_6M	R/C	The bit indicates the status (interrupt) of 6.5536M XTAL diable. When EXIST_6M status bit changed from 1 to 0, the status bit set 1. When the bit is 1, it represents 6.5536M crystal is removed or damaged. Write 1 to clear the bit.	0x0
0	INT_32K	R/C	The bit indicates the status (interrupt) of 32.768K XTAL disable. When EXIST_32K status bit changed from 1 to 0, the status bit set 1. When the bit set 1, it represents 32.768K crystal is removed or damaged. Write 1 to clear the bit.	0x0

7.5.9 MISC2_CLKSEL Register

Table 7-13 MISC2_CLKSEL Register

Bit	Name	Type	Contents	Default
31:3	-	-	Reserved.	0
2:0	CLKSEL	R/W	The register is used to control AHB clock source. 0:RCH (6.5M RC) 1:XOH (6.5536M XTAL) 2:PLLH 3: RTCCLK (Controlled by RTCCLK_SEL from PMU_CONTROL register) 4:PLLL Others:Reserved Before the clock selects a clock source, the user should first enable the corresponding module by setting the PMU_CONTROL register.	0x0

7.5.10 MISC2_CLKDIVH Register

Table 7-14 MISC2_CLKDIVH Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVH	R/W	The register is used to control AHB clock divider. 0:Clock source divide by 1. 1:Clock source divide by 2. 2:Clock source divide by 3. ... 255:Clock source divided by 256.	0x00

7.5.11 MISC2_CLKDIVP Register

Table 7-15 MISC2_CLKDIVP Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVP	R/W	The register is used to control APB clock divider. 0:AHB clock divide by 1. 1:AHB clock divide by 2. 2:AHB clock divide by 3	0x01

			... 255:AHB clock divide by 256.	

7.5.12 MISC2_HCLKEN Register

Table 7-16 MISC2_HCLKEN Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved.	0
8:0	HCLKEN	R/W	The register is used to control the clock enable of each AHB module. The corresponding module can be disabled only when its function is not used. The details about each module, please refer to the following table. 0:disable 1:enable	0x1FF

Table 7-17 HCLK Clock Enable

Bit	Module	Note
0	--	Reserved.
1	Arbiter&BusMatrix	Reserved.
2	FLASH controller	Reserved.
3	SRAM controller	Reserved.
4	DMA controller	
5	GPIO controller	
6	LCD controller	
7	--	
8	CRYPT controller	

7.5.13 MISC2_PCLKEN Register

Table 7-18 MISC2_PCLKEN Register

Bit	Name	Type	Contents	Default
31:0	PCLKEN	R/W	The register is used to control the clock enable of each APB module. The corresponding module can be disabled only when its function is not used. The details about each module, please refer to the following table.	0xFFFFFFFF

			0:disable 1:enable	

Table 7-19 PCLK Clock Enable for Each Module

Bit	Module	Note
0	AHB2APB Bridge	Reserved.
1	DMA Controller	
2	I2C	
3	SPI1	
4	UART0	
5	UART1	
6	UART2	
7	UART3	
8	UART4	
9	UART5	
10	ISO78160	
11	ISO78161	
12	TIMER	
13	MISC1	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K0	
19	U32K1	
20	Reserved	
21	SPI2	
22	SPI3	
31:23	Reserved	

8. Analog Controller

8.1 Introduction

Analog controller is used to control analog functions of V85XXP. All the analog related controls such as ADC, comparator and other analog detect units are controlled by this module. Analog controller is always power-on, so all the analog settings will be kept under the deep-sleep mode and will not be reset.

8.2 Features

--Generate the analog detective interruption/ wake-up signal;

--Generate the comparator interruption;

--Comparator counter;

--ADC by manual and auto-sampling mode;

--Generate ADC interruption.

8.3 Functional Block Diagram

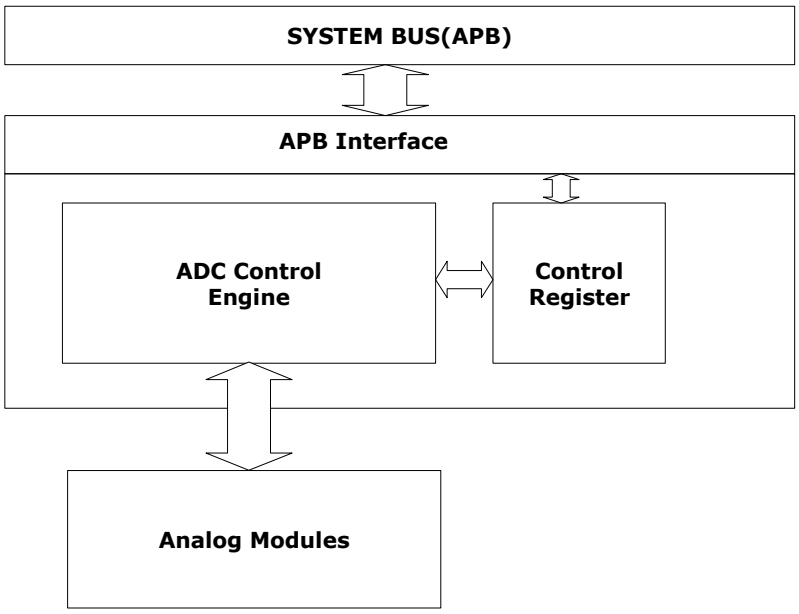


Figure 8-1 Functional Block Diagram of Analog Controller

8.4 Register Address

Table 8-1 ANA Control Register (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00

ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog reigster 3	0x00
ANA_REG4	R/W	0x0010	Analog register 4	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00
ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REG9	R/W	0x0024	Analog register 9	0x00
ANA_REGA	R/W	0x0028	Analgo register 10	0x00
ANA_REGB	R/W	0x002C	Analog register 11	From FLASH
ANA_REGC	R/W	0x0030	Analog register 12	From FLASH
ANA_REGD	R/W	0x0034	Analog register 13	From FLASH
ANA_REGE	R/W	0x0038	Analog register 14	From FLASH
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_REG10	R/W	0x0040	Analog register 16	From FLASH
ANA_REG11	W	0x0044	Analog register 17	--
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_ADCSTATE	R	0x005C	ADC status register	--
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL0	R/W	0x0068	ADC control register 0	0x00000000
ANA_CMPCTL	R/W	0x006C	Comparator control register	0x00000000
ANA_ADCDATA0	R	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	R	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	R	0x0084	ADC channel 5 data register	--

ANA_ADCDATA6	R	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC channel 9 data register	--
ANA_ADCDATA10	R	0x0098	ADC channel 10 data register	--
ANA_ADCDATA11	R	0x009C	ADC channel 11 data register	--
ANA_ADCDATA12	R	0x009C	ADC channel 12 data register	--
ANA_ADCDATA13	R	0x009C	ADC channel 13 data register	--
ANA_ADCDATA14	R	0x009C	ADC channel 14 data register	--
ANA_ADCDATA15	R	0x009C	ADC channel 15 data register	--
ANA_CMPCNT1	R/C	0x00B0	Comaprator 1 counter	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter	0x00000000
ANA_MISC	R/W	0x00B8	Analog misc control register	0x00
ANA_ADCDOS	R	0x00C0	ADC self-calibration register DOS	0
ANA_ADCDCPN	R	0x00CC	ADC self-calibration register DCPN	0
ANA_ADCDCNM0	R	0x00D8	ADC self-calibration register DCNM0	0
ANA_ADCDATADMA	R/W	0x00E0	ADC data source of DMA	--
ANA_CMPTHR	R/W	0x00E4	CMP1/CMP2 threshold register	0x00000000
ANA_ADCCTRL1	R/W	0x00E8	ADC control register 1	0x000000C0
ANA_ADCCTRL2	R/W	0x00EC	ADC control register 2	0x00000000
ANA_ADCDATATHD1_0	R/W	0x00F4	ADC threshold control register	0x00000000
ANA_ADCDATATHD3_2	R/W	0x00F8	ADC threshold control register	0x00000000
ANA_ADCDATATHD_CH	R/W	0x00FC	ADC threshold status register	0x00000000

8.5 Register Definition

8.5.1 ANA_REGx Register

Table 8-2 ANA_REGx Table

Name	Bit								Address
	7	6	5	4	3	2	1	0	
ANA_REG0	-	-	must write 0x3		-	-	-	ADCFRQSEL	0x0000
ANA_REG1	ADCMODESEL	-	-	-	ADCSEL[3:0]				0x0004
ANA_REG2	-	-	CMP2REFSEL	CMP1REFSEL	CMP2SEL[1:0]		CMP1SEL[1:0]		0x0008
ANA_REG3	XOHPDN	PLLHPDN	PLLLPDN	RCHPD	BGPPD	CMP2PDN	CMP1PDN	-	0x000C
ANA_REG4	-		-		-	must write 0x1			0x0010
ANA_REG5	-	AVCCLVDETPD	-	-	CMP2IT[1:0]		CMP1IT[1:0]		0x0014
ANA_REG6	BATRTCDISC	BAT1DISC	-	-				LCDBMODE	0x0018
ANA_REG7	must write 1	-	-	-	-	VDCINHYSSEL	-	-	0x001C
ANA_REG8	AVCCLDOPD	VDDPVDSEL[2:0]			-	-	DVCCSEL[1:0]		0x0020
ANA_REG9	VDDDETPD	PLLHSEL[3:0]			PLLLSEL[2:0]				0x0024
ANA_REGA	VDCINDETPD	-	-	-	-	-	must write 1	-	0x0028
ANA_REGB[1]	-			RCLTRIM<4:0>					0x002C
ANA_REGC[1]	-		RCHTRIM[5:0]						0x0030
ANA_REGD[1]	-	-	-		-				0x0034
ANA_REGE[1]	BKPWREN	-	-		-	-			0x0038
ANA_REGF	ADTREF3SEL	ADTREF2SEL	ADTREF1SEL	ADTSEL	ADTPDN	AVCCOEN	BATRTCDETEN	BAT1DETEN	0x003C
ANA_REG10[1]	-	-			-	-			0x0040
ANA_REG11[2] W	VINBUFPD	REFBUFPD	-	-	-	-	-	-	0x0044

[1]: These register (REGB~REGE and REG10) are the parameter adjusting registers of analog module. When the chip is reset, it automatically loaded from FLASH and usershould not modify it.

[2]: ANA_REG11 is a write-onlyregister, not for read, and the data read is uncertain. Meanwhile, after writing the register, it cannot be confirmed whether the writing is successful or not. The default value is a random value, user cannot use AND and OR operation.

8.5.2 ANA_REG0 Register

Table 8-3 Function description of each bit of ANA_REG0

Bit	Name	Type	Contents	Default
7:0	-	R/W	Reserved.	Default is 0, and it must set 0x30.

8.5.3 ANA_REG1 Register

Table 8-4 Function description of each bit of ANA_REG1

Bit	Name	Type	Contents	Default
6:0	-	-	Reserved.	0
7	ADCMODESEL	R/W	ADC mode selection. When RESDIV_CHx=1, the control bit is valid. 0:When the test channel inputs non-AC cycle. 1:When the test channel inputs AC cycle (i.e.±300mV signal)	0

8.5.4 ANA_REG2 Register

Table 8-5 Function description of each bit of ANA_REG2

Bit	Name	Type	Contents	Default
1:0	CMP1SEL[1:0]	R/W	The selection of CMP1 signal input source 00:CMP1_P and REF 01:CMP1_N and REF 1*:CMP1_P and CMP1_N	0
3:2	CMP2SEL[1:0]	R/W	The selection of CMP2 signal input source 00:CMP2_P and REF 01:CMP2_N and REF 1*:CMP2_P and CMP2_N	0
4	CMP1REFSEL	R/W	REF selection of CMP1 0:VREF 1:BGPREF	0
5	CMP2REFSEL	R/W	REF selection of CMP2 0:VREF 1:BGPREF	0
7:6	-	-	Reserved.	0

8.5.5 ANA_REG3 Register

Table 8-6 Function description of each bit of ANA_REG3

Bit	Name	Type	Contents	Default
0	-	-	Reserved.	0
1	CMP1PDN	R/W	CMP1 power on/ down control signal 0:disable CMP1 1:enable CMP1	0
2	CMP2PDN	R/W	CMP2 power on/down control signal 0:disable CMP2 1:enable CMP2	0
3	BGPPD*[1]	R/W	BGP power on/down control signal 0:enable BGP 1:disable BGP	0
4	RCHPD	R/W	(High frequency RC clock circuit) RCH (6.5536M RC) power on/ down control signal 0:enable RCH 1:disable RCH	0
5	PLLLPDN	R/W	PLLL (32768Hz input PLL) power on/down control signal 0:disable PLLL 1:enable PLLL	0
6	PLLHPDN	R/W	PLLH (6.5536MHz input PLL) power on/down control signal 0:disable PLLH 1:enable PLLH	0
7	XOHPDN	R/W	6.5536M crystal osicallator circuit power on/down control signal 0:disable XOH 1:enable XOH	0
*[1]:RCH, PLL, and ADC are related to BGP. Before enabling RCH, PLL, ADC, user must enable BGP first. IfBGP is not used in the system, user can disable BGP via BGPPD. Meanwhile, if BGP is used, user cannot disable BGP via BGPPD. Because the system has a protection to enable BGP again., In sleep or deep-sleep mode, user can disable BGP no matter it is used or not.				

8.5.6 ANA_REG4 Register

Table 8-7 Function description of each bit of ANA_REG4

Bit	Name	Type	Contents	Default
7:0	-	R/W	Reserved.	Default is 0x00, an it must set 0x01.

8.5.7 ANA_REG5 Register

Table 8-8 Function description of each bit of ANA_REG5

Bit	Name	Type	Contents	Default
1:0	CMP1IT[1:0]	R/W	Bias current selection for CMP1 00:20nA ; 01:100nA ; 1*:500nA ;	0
3:2	CMP2IT[1:0]	R/W	Bias current selection for CMP2 00:20nA ; 01:100nA ; 1*:500nA ;	0
5:4	-	-	Reserved.	0
6	AVCCLVDETPD	R/W	AVCC power on/ down control for low voltage detection. 0:enable; 1:disable	0
7	-	-	Reserved.	0

8.5.8 ANA_REG6 Register

Table 8-9 Function description of each bit of ANA_REG6

Bit	Name	Type	Contents	Default
0	LCDBMODE	R/W	LCD bias mode selection 0:1/3 bias 1:1/4 bias	0
4:1	VLCD[3:0]	R/W	When VLCD=0:Default; When VLCD=0~6:the equlation range =+50mV*VLCD; When VLCD=7~15:the equlation range =-50mV*(VLCD-6);	
5	-	-	Reserved.	0
6	BAT1DISC	R/W	BAT1 battery dischagred, the resistance is 1.7K, and the current is Vbat1/1.7k. 0:disable 1:enable the 1.7k resistance from BAT1 to GND	0
7	BATRTCDISC	R/W	BATRTC battery dischagred, the resistance is 1.7k, and the current is Vbatrtc/1.7k. 0:disable 1:enable the 1.7k resistance from BATRTC to GND.	0

8.5.9 ANA_REG7 Register

Table 8-10 Function description of each bit of ANA_REG7

Bit	Name	Type	Contents	Default
7:3	-	R/W	Reserved.	Default is 0, must set 0x10.
2	VDCINHYSSEL	R/W	The hysteresis selection for VDCIN pin voltage detection. 0:100mV 1:200mV	0
1:0	-	R/W	Reserved.	0

8.5.10 ANA_REG8 Register

Table 8-11 Function description of each bit of ANA_REG8

Bit	Name	Type	Contents	Default

1:0	DVCCSEL[1:0]	R/W	DVCC voltage regulation . 00:+0.0V 01:+0.1V 10:-0.1V 11:+0.2V	0
3:2	-	-	Reserved.	0
6:4	VDDPVDSEL[2:0]	R/W	VDD low-voltage monitor threshold register. The setting wilaffect the status of VDDALARM. 000:4.5V 001:4.2V 010:3.9V 011:3.6V 100:3.2V 101:2.9V 110:2.6V 111:2.3V	0
7	AVCCLDOPD	R/W	AVCC LDO control in order to the disable or enable of LDO. 0: enable LDO, AVDD pins voltage is 3.3V. 1: disable LDO, AVCC pins is connected to VDD through a switch. The internal resistance of the switch please refer to Table1-4. AVCCLDO will be disabled only when the supply voltage is lower than 3.6V.	0

8.5.11 ANA_REG9 Register

Table 8-12 Function description of each bit of ANA_REG9

Bit	Name	Type	Contents	Default
2:0	PLLLSEL[2:0]	R/W	PLLL frequency selection. 000:26.2144MHz 001:13.1072MHz 010:6.5536MHz 011:3.2768MHz 100:1.6384MHz	0

			101:0.8192MHz 110:0.4096MHz 111:0.2048MHz	
6:3	PLLHSEL[3:0]	R/W	PLLH frequency selection. The frequency of PLLH is external XOH or the multiples of internal RCH. 1000~1011:Reserved. 1100:2x input clock frequency 1101:2.5x input clock frequency 1110:3x input clock frequency 1111:3.5x input clock frequency 0000:4x input clock frequency 0001:4.5x input clock frequency 0010:5x input clock frequency 0011:5.5x input clock frequency 0100:6x input clock frequency 0101:6.5x input clock frequency 0110:7x input clock frequency 0111:7.5x input clock frequency	0
7	VDDDETPD	R/W	Diable the VDD voltage monitor module. The module is powered by VDD. 0:enable 1:disable	0

8.5.12 ANA_REGA Register

Table 8-13 Functional Description of each bit of ANA_REGA

Bit	Name	Type	Contents	Default
6:0	-	R/W	Reserved, and it must set 0x02.	0x0
7	VDCINDETPD	R/W	VDCIN monitoring module switch. 0:enable VDCIN monitoring 1:disable VDCIN monitoring	0

8.5.13 ANA_REGB Register

Table 8-14 Functional Description of each bit of ANA_REGB

Bit	Name	Type	Contents	Default
4:0	RCLTRIM[4:0]	R	32kHz RC frequency egulation. 00000~01111:frequency increase in 4% steps. 10000~11111:frequency decrease in 4% steps.	0
7:5	-	-	Reserved.	0
Note: User do not configure the register ANA_REGx(x=B~E and 10), these register values will be automatically loaded from FLASH.				

8.5.14 ANA_REGC Register

Table 8-15 Functional Description of each bit of ANA_REGC

Bit	Name	Type	Contents	Default
5:0	RCHTRIM[5:0]	R	6.5536MHz RC frequency egulation 000000~011111:frequency increases in 1.25% steps. 100000~111111:frequency decareses in 1.25% steps.	0
7:6	-	-	Reserved	0
Note: User do not configure the register ANA_REGx(x=B~E and 10), these register values will be automatically downloaded from FLASH.				

8.5.15 ANA_REGD Register

Table 8-16 Functional Description of each bit of ANA_REGD

Bit	Name	Type	Contents	Default
7:0	-	-	Reserved	0
Note: User do notconfigure the register ANA_REGx(x=B~E and 10), these register values will be automatically downloaded from FLASH.				

8.5.16 ANA_REGE Register

Table 8-17 Functional Description of each bit of ANA_REGE

Bit	Name	Type	Contents	Default
6:0	-	-	Reserved	0
7	BKPWREN	R	Enable low-power backup power supply (Disable AVCC when entering the sleep mode, and it will enable low-power backup power supply.)0:Disable(Still use AVCC during the sleep mode) 1:Enable	0
Note: User do not set register ANA_REGx(x=B~E and 10), these register values will be automatically loaded from FLASH.				

8.5.17 ANA_REGF Register

Table 8-18 Functional Description of each bit of ANA_REGF

Bit	Name	Type	Contents	Default
0	BAT1DETEN	R/W	Enable BAT1 to connect to the P terminal input of comparator 1 0:disable 1:enable	0
1	BATRTCDETEN	R/W	Enable BATRTC to connect to the P terminal input of comparator 2 0:disable 1:enable	0
2	AVCCOEN	R/W	AVCC_OUT pin output enable control 0:output the high resistance 1: Allow AVCC_OUT pin to output the power voltage of internal AVCC module.	0
3	ADTPDN	R/W	Tiny ADC switch control 0:disable 1:enable	0
4	ADTSEL	R/W	Tiny ADC signal input source selection 0:connects to IOE6 1:connects to IOE7	0
5	ADTREF1SEL	R/W	ADTREF1 voltage selection 0:0.9V 1:0.7V	0
6	ADTREF2SEL	R/W	ADTREF2 voltage selection 0:1.8V 1:1.6V	0
7	ADTREF3SEL	R/W	ADTREF3 voltage selection 0:2.7V 1:2.5V	0

8.5.18 ANA_REG10 Register

Table 8-19 Functional Description of each bit of ANA_REG10

Bit	Name	Type	Contents	Default

7:0	-	-	Reserved.	0
Note: User do not configure the register ANA_REGx(x=B~E and 10), these register values will be automatically downloaded from FLASH.				

8.5.19 ANA_REG11 Register

Table 8-20 Functional Description of each bit of ANA_REG11

Bit	Name	Type	Contents	Default
7:0	-	-	Reserved, user only can write 0.	--
Note: ANA_REG11 register only supports writing 0, there are not related of the reading and writing contents. User cannot use "OR" and "AND" operation.				

8.5.20 ANA_CTRL Register

Table 8-21 ANA_CTRL Register

Bit	Name	Type	Contents	Default
31:27	-	-	Reserved.	0
26	PDNS2	R/W	This bit controls the behavior of entering deep sleep mode when VDDALARM is 0 (while considering the setting of PDNS). 0: When VDDALARM is 0, it will not enter the deep-sleep mode. When VDDALARM is 1, system can enter the deep-sleep mode; and when VDDALARM changes to 0, the system automatically wakes up from deep-sleep mode. 1: VDDALARM is not used as a deep–sleep mode condition.	0x0
25:24	-	-	Reserved.	0
23:22	CMP2DEB	R/W	Comparator 2 debounce control register. 0: no debounce 1: 2 x RTCCLK debounce cycles 2: 3 x RTCCLK debounce cycles 3: 4 x RTCCLK debounce cycles When the debounce is enabled, the input signal is valid only when the signal does not change within multiple cycles of the RTCCLK clock. In addition, the	0x0

			response time of wake-up and interrupt will be delayed until the signal is valid. The circuit can work in all modes, including sleep and deep- sleep mode.	
21:20	CMP1DEB	R/W	Comparator 1 de-bounce control register. 0: no de-bounce 1: 2 x RTCCLK debounce cycles. 2: 3 x RTCCLK debounce cycles. 3: 4 x RTCCLK debounce cycles. When the debounce is enabled, the input signal is valid only when the signal does not change within multiple cycles of the RTCCLK clock. In addition, the response time of wake-up and interrupt will be delayed until the signal is valid. The circuit can work in all modes, including sleep and deep-sleep mode.	0x0
19:16	-	-	Reserved.	0
15:8	RCHTGT	R/W	The setting of high frequency RCH auto-calibration. The register is used to store the high-frequency clock target value to be set by the user. If the target frequency value to be set by the user is 6.5536MHz, then the user needs to fill in 6553600/32768=200 in this register.	0x0
7	-	-	Reserved.	0
6	PDNS	R/W	This bit controls the behavior of entering the deep-sleep mode when VDCINDROP is 0 (while considering the setting of PDNS2). 0: When VDDALARM is 0, it will not enter the deep-sleep mode. When VDDALARM is 1, the system can enter the deep-sleep mode; and the VDDALARM changes to 0, the system automatically wakesup from deep-sleep mode. 1: No matter what the value of VDCINDROP is, it can enter the deep-sleep mode.	0x0
5:4	-	-	Reserved.	0
3:2	CMP2SEL	R/W	The register is used to control the counter accumulative condition of comparator 2. 0: disable	0x0

			1: the rising edge of comparator 2 output 2: the falling edge of comparator 2 output 3: the both edge of comparator 2 output	
1:0	CMP1SEL	R/W	The register is used to control the counter accumulative condition of comparator 1. 0: disable 1: the rising edge of comparator 1 output 2: the falling edge of comparator 1 output 3: the both edge of comparator 1 output	0x0

8.5.21 ANA_CMPOUT Register

Table 8-22 ANA_CMPOUT Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:14	TADCO	R	TinyADC output	-
13:11	-	-	Reserved	0
10	AVCCLV	R	AVCC low-voltage status bit. The Hystersis voltage is 20mV~30mV. 0:AVCC is higher than 2.5V. 1:AVCC is lower than 2.5V.	0x0
9	-	-	Reserved.	0
8	VDCINDROP	R	VDCIN power-down status. 0:VDCIN is higher than threshold voltage without power-down. 1:VDCIN is lower than threshold voltage withpower-down.	0x0
7	VDDALARM	R	VDDALARM output of VDD power supply. 0: The VDD power supply voltage is higher than the value set by VDDPVDSEL. 1: The VDD power supply voltage is lower than the value set byVDDPVDSEL.	0x0
6:4	-	-	Reserved.	0
3	CMP2	R	Comparator 2 output	0x0

2	CMP1	R	Comparator 1 output	0x0
1	LOCKL	R	PLLL locked status, the locked time is around 1ms. 0:PLLL is not locked. 1:PLLL is locked.	0x0
0	LOCKH	R	PLLH locked status, the locked time is around 15μs. 0:PLLH is not locked. 1:PLLH is locked.	0x0

8.5.22 ANA_ADCSTATE Register

Table 8-23 ANA_ADCSTATE Register

Bit	Name	Type	Contents	Default
31:5	-	-	Reserved	0x0
4	RESET	R	The bit shows the RESET status in ADC interface.	0x0
3	ADC_EN	R	The bit shows the ADC_EN status in ADC interface.	0x0
2:0	ADCSTATE	R	These bits show the status of ADC controller. 0:idle 2:automatic conversion for ADC multi-channel 4:manual conversion for ADC multi-channel Others:reserved	0x0

8.5.23 ANA_INTSTS Register

Table 8-24 ANA_INTSTS Register

Bit	Name	Type	Contents	Default
31:22	-	-	Reserved.	0
21	INTSTS21	R/C	ADC_THD3 data is greater than the UPPER_THD3 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0

20	INTSTS20	R/C	ADC_THD3 data is smaller than the LOWER_THD3 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
19	INTSTS19	R/C	ADC_THD2 data is greater than the UPPER_THD2 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
18	INTSTS18	R/C	ADC_THD2 data is smaller than the LOWER_THD2 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
17	INTSTS17	R/C	ADC_THD1 data is greater than the UPPER_THD1 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
16	INTSTS16	R/C	ADC_THD1 data is smaller than the LOWER_THD1 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
15	INTSTS15	R/C	ADC_THD0 data is greater than the UPPER_THD0 threshold interrupt flag bit.	0x0

			Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	
14	INTSTS14	R/C	ADC_THD0 data is smaller than the LOWER_THD0 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
13	INTSTS13	R/C	TADC threshold interrupt flag bit. When TADC is rising or falling, and the change value from the previous cycle is greater than the threshold (TADCTH), the interrupt flag bit will be set. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
12	INTSTS12	R/C	Analog control register ANA_REGx error flag bit. The chip automatically performs the checksum check and parity check to all analog registers ANA_REGx. When external interference causes the analog register ANA_REGx to be incorrectly written, the flag bit will be set to 1. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
11	INTSTS11	R/C	When VDCINDROP is 0, enter the interrupt flag bit of sleep mode (VDCIN is greater than the threshold value). When VDCINDROP is 0 andthe system goes to sleep is detected, the interrupt flag bit wil be set. User can enable the interrtupflag bit (INTEN11) to wake	0x0

			system up from the sleep or deep-sleep mode(VDCINDROP is 0). Read 0:did not enter the sleep mode (VDCINDROP=0) Read 1:entered the sleep mode (VDCINDROP=0) Write 0:no effect Write 1:clear the bit	
10	INTSTS10	R/C	AVCCLV low-voltage interrupt flag bit. Read 0:did not occur Read 1:occured Write 0:no effect Write 1:clear the bit	0x0
9	-	-	Reserved.	0
8	INTSTS8	R/C	The interrupt flag bit of VDCINDROP. The interrupt will occur when VDCINDROP is rising or falling. Read 0:did not occur Read 1:occured Write 0:no effect Write 1:clear the bit	0x0
7	INTSTS7	R/C	The interrupt flag bitof VDDALARM. The interruptwill occur when VDDALARM is rising or falling. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
6:4	-	-	Reserved	0
3	INTSTS3	R/C	The interrupt flag bit of CMP2. The interrupt condition is controlled by CMP2SEL. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0

2	INTSTS2	R/C	The interrupt flag bit of CMP1. The interrupt condition is controlled by CMP1SEL. Read 0:did not occur Read 1: CMP1 interrupt occurred Write 0:no effect Write 1:clear the bit	0x0
1	INTSTS1	R/C	Interrupt flag bit for ADC automatic switch is completed. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
0	INTSTS0	R/C	Interrupt flag bit for ADC automatic switch is completed by manual control. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0

8.5.24 ANA_INTEN Register

Table 8-25 ANA_INTEN Register

Bit	Name	Type	Contents	Default
31:22	-	-	Reserved	0
21	INTEN21	R/W	Interrupt enable control when ADC_THD3 data is greater than UPPER_THD3 threshold. 0:disable 1:enable	0x0
20	INTEN20	R/W	Interrupt enable control when ADC_THD3 data is smaller than LOWER_THD3 threshold . 0:disable 1:enable	0x0

19	INTEN19	R/W	Interrupt enable control when ADC_THD2 data is greater than UPPER_THD2 threshold. 0:disable 1:enable	0x0
18	INTEN18	R/W	Interrupt enable control when ADC_THD2 data is smaller than LOWER_THD2 threshold. 0:disable 1:enable	0x0
17	INTEN17	R/W	Interrupt enable control when ADC_THD1 data is greater than UPPER_THD1 threshold. 0:disable 1:enable	0x0
16	INTEN16	R/W	Interrupt enable control when ADC_THD1 data is smaller than LOWER_THD1 threshold. 0:disable 1:enable	0x0
15	INTEN15	R/W	Interrupt enable control when ADC_THD0 data is greater than UPPER_THD0 threshold. 0:disable 1:enable	0x0
14	INTEN14	R/W	Interrupt enable control when ADC_THD0 data is smaller than LOWER_THD0 threshold. 0:disable 1:enable	0x0
13	INTEN13	R/W	TADC interrupt and wake-up enable (the change of TADC output value is greater than or equal to the threshold). 0:Disable TADC interrupt and wake-up. 1:Enable TADC interrupt and wake-up.	0x0
12	INTEN12	R/W	The analog register ANA_REGx status error interrupt wake-up enable control bit. 0:disable	0x0

			1:enable	
11	INTEN11	R/W	When VDCINDROP is 0, the event of entering sleep mode is detected, and the interrupt and wake-up enable control of the event. 0:When VDCINDROP is 0, the sleep mode is detected and the interrupt or wake-up event is disabled. 1: When VDCINDROP is 0, sleep mode is detected and the interrupt or wake-up event is enabled	0
10	INTEN10	R/W	AVCCLV interrupt and wake-up enable control. 0:Disable AVCCLV interrupt and wake-up 1:Enable AVCCLV interrupt and wake-up	0x0
9	-	-	Reserved	0
8	INTEN8	R/W	VDCINDROP interrupt and wake-up enable control. 0:Disable VDCIN interrupt and wake-up 1:Enable VDCIN interrupt and wake-up	0x0
7	INTEN7	R/W	VDDALARM interrupt and wake-up enable control. 0:Disable VDDALARM interruptand wake-up 1:Enable VDDALARM interrupt and wake-up	0x0
6:4	-	-	Reserved	0
3	INTEN3	R/W	CMP2 interrupt and wake-up enable control. 0:Disable CMP2 interrupt and wake-up 1:Enable CMP2 interrupt and wake-up	0x0
2	INTEN2	R/W	CMP1 interrupt and wake-up enable control. 0:Disable CMP1 interrup and wake-up control. 1:Enable CMP1 interrupt and wake-up control.	0x0
1	INTEN1	R/W	Interrupt enable control for ADC automatic conversion completed. 0:Disable ADC automatic conversion interrupt 1:Enable ADC automatic conversion interrupt	0x0
0	INTEN0	R/W	Interrupt enable control for ADC manual conversion completed. 0: Disable ADC manual conversion interrupt.	0x0

			1: Enable ADC manual conversion interrupt.	

8.5.25 ANA_ADCCTRL0 Register

Table 8-26 ANA_ADCCTRL0 Register

Bit	Name	Type	Contents	Default
31	MTRIG	R/W	Manually control ADC conversion. Write 0: no effect Write 1: enable manual ADC conversion one time Read 0: manual ADC conversion currently has been completed Read 1: manual ADC conversion currently is not completed	0x0
30:22	-	-	Reserved	0
21:20	-	R/W	Reserved, the register must be set 0x03.	0
19	STOP	R/W	Force the ADC conversion process to stop. Write 1 to this bit and keep it for a ADCCLK period to stop the current ADC conversion. Write 0 to this bit before the next ADC conversion starts.	0x0
18:16	AEN	R/W	ADC automatic conversion enable control register. 0:Disable ADC automatic conversion 1: ADC automatic conversion is triggered by RTC_ITV and RTC_SITV. 2: ADC automatic conversion is triggered by RTC_WKUSEC. 3: ADC automatic conversion is triggered by RTC_ALARM. 4: ADC automatic conversion is triggered by the overflow of Timer 0. 5:ADC automatic conversion is triggered by the overflow of Timer 1. 6:ADC automatic conversion is triggered by the overflow of Timer 2.	0x0

			7:ADC automatic conversion is triggered by the overflow of Timer 3.	
15:13	-	-	Reserved	0
12	CLKSRCSEL	R/W	ADC clock source selection. When this bit is changed, the hardware logic will stop, and the stop time is 3 ADC clocks. At this time, any ADC operation will be ignored by the hardware. So, user should not operate ADC during this period. 0:6.5M RCH 1:6.5M PLLL	0x0
11:0	-	-	Reserved	0

8.5.26 ANA_ADCDATAx Register

Table 8-27 ANA_ADCDATAx Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	ADCDATAx	R	ADC conversion result data register DATA0:Store the conversion result for ADC channel 0 DATA1:Store the conversion result for ADC channel 1. … DATA15:Store the conversion result for ADC channel 15.	0x--

8.5.27 ANA_CMPCNTx Register

Table 8-28 ANA_CMPCNTx Register

Bit	Name	Type	Contents	Default
31:0	CNT	R/C	This register is used to store the counter of the number of occurrences of the comparator x event. This register can be cleared by writing 0, but this operation is only valid when CMPxPDN=1 (x=1,2).	0x0000000

8.5.28 ANA_MISC Register

Table 8-29 ANA_MISC Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0x0
5:4	TADCTH	R/W	TADC threshold setting. This register controls the threshold for TADC to generate an interrupt. TADC clock selects internal 32K RC as the clock source to sample external signals. When the TADC interrupt is enabled, and the difference between the sampled values of two consecutive cycles is greater than the threshold, INTSTS13 will be set 1 and an interrupt will be generated.	0x0
3:0	-	-	Reserved.	0x0

8.5.29 ANA_ADCDOS Register

Table 8-30 ANA_ADCDOS Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved	0
8:0	DOS	R	ADC automaticcalibration register DOS	0

8.5.30 ANA_ADCDCPN Register

Table 8-31 ANA_ADCDCPN Register

Bit	Name	Type	Contents	Default
31:27	DCPN4	R	ADC automatic calibration register DCPN4	
26:18	DCPN3	R	ADC auto-matic calibration register DCPN3	
17:9	DCPN2	R	ADC automatic calibration register DCPN2	
8:0	DCPN1	R	ADC automatic calibration register DCPN1	

8.5.31 ANA_ADCDCNM0 Register

Table 8-32 ANA_ADCDCNM0 Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved	0
8:0	NM0	R	ADC automatic calibration register NM0	0

8.5.32 ANA_ADCDATADMA Register

Table 8-33 ANA_ADCDATADMA Register

Bit	Contents	Type	Contents	Default
31:16	-	-	Reserved	0x0
15:0	ADCDATA_DMA	R	ADC data source for DMA	0x0

8.5.33 ANA_ADCCTRL1 Register

Table 8-34 ANA_ADCCTRL1Register

Bit	Name	Type	Contents	Default
31:16	RESDIV_CHx	R/W	Each bit controls the enable and disable of the resistance divider corresponding to the ADC channel. 0:disable to voltage divider 1:enable to voltage divider RESDIV_CH15~0 correspond to ADC channels 15~0 respectively.	0x0
15	UPPER_THD3_EN	R/W	UPPER_THD3 threshold detect control 0:disable 1:enable	0x0
14	LOWER_THD3_EN	R/W	LOWER_THD3 threshold detect control 0:disable 1:enable	0x0
13	UPPER_THD2_EN	R/W	UPPER_THD2 threshold detect control 0:disable 1:enable	0x0
12	LOWER_THD2_EN	R/W	LOWER_THD2 threshold detect control 0:disable 1:enable	0x0
11	UPPER_THD1_EN	R/W	UPPER_THD1 threshold detect control 0:disable 1:enable	0x0
10	LOWER_THD1_EN	R/W	LOWER_THD1 threshold detect control	0x0

			0:disable 1:enable	
9	UPPER_THD0_EN	R/W	UPPER_THD0 threshold detect control 0:disable 1:enable	0x0
8	LOWER_THD0_EN	R/W	LOWER_THD0 threshold detect control 0:disable 1:enable	0x0
7:0	-	R/W	Reserved, user must set to 0xC2.	0XC0

8.5.34 ANA_ADCCTRL2 Register

Table 8-35 ANA_ADCCTRL2 Register

Bit	Name	Type	Contents	Default
31:16	SCAN_CHx	R/W	Each bit represents the enable or disable of corresponding channel in multi-channel ADC scan mode. 0:disable 1:enable SCAN_CH15~0 correspond to ADC channels 15~0 respectively.When SCAN_CHx is all 0, the multi-channel ADC scan is full scan of the first 12 channels.	0x0
15	-	R/W	Reserved, user must set to 1.	0x0
14:12	-	R/W	Reserved, user must set to 0.	0x0
11	CONV_ERR	R	ADC conversion error flag bit. It represents whether the error occurrence during the conversion. 0:No error occurred during the conversion time 1:An error occurred during the conversion time.	0x0
10	CAL_ERR	R	ADC automatic calibration error flag bit. It represents whether the error occurrence during the automatic calibration . 0:No error occurred during the automatic calibration.	0x0

			1:An error occurred during the automatic calibration.	
9	CONV_ERR_CLR	R/C	Write 1 to the bit to reset CONV_ERR to 0. Write 0 to the bit to clear it.	0x0
8	CAL_ERR_CLR	R/C	Write 1 to the bit to reset CAL_ERR to 0. Write 0 to the bit to clear it.	0x0
7	ADC_CAL_DONE	R	ADC self-calibration completed flag bit. 1: ADC self-calibration is completed. 0: ADC self-calibration is not completed. This bit is cleared to 0 after DPORST (PMU_STS[6]) reset or ADC RESET (ANA_ADCCTRL2[1]) occurs.	0x0
6	ADC_EN_TRG_CAL	R/W	ADC automatic -calibration enable control bit 1: Write 1 to ADC_EN(ANA_ADCCTRL2[0]) to trigger ADC automatic calibration. 0: Write 0 to ADC_EN(ANA_ADCCTRL2[0]) to not trigger ADC automatic calibration.	0x0
5	BUSY	R	The flag bit for whether ADC is busy. 1: ADC is busy, ADC is automatic calibration, sampling or conversion now. 0: ADC is not busy. ADC automatic calibration, sampling or conversion are idle.	0x0
4	-	R/W	Reserved, user must set to 1.	0x0
3:2		R/W	Reserved, user must set to 0.	0x0
1	RESET	R/W	In addition to the automatic calibration register, this bit also resets the ADC digital circuit. 0: normal work 1: Reset	0x0
0	ADC_EN	R/W	ADC is enabled and sampled by the falling edge of MCLK. 0: Disable ADC, ADC is in low-power shutdown status, and the automatic calibration register is not reset. 1: Enable ADC.	0x0

			ADC can be enabled until ADC_EN is enabled duration of 4 ADC clocks.	

8.5.35 ANA_ADCDATATHD1_0 Register

Table 8-36 ANA_ADCDATATHD1_0 Register

Bit	Name	Type	Contents	Default
31:24	UPPER_THD1	R/W	When the ADC data is shifted to the right 8 bits and the data is higher than this setting value, the UPPER_THD1_TRGED status will be updated. BIT7 is the sign bit.	0x0
23:16	LOWER_THD1	R/W	When the ADC data is shifted to the right 8 bits and the data is lower than this setting value, the LOWER_THD1_TRGED status will be updated. BIT7 is the sign bit.	0x0
15:8	UPPER_THD0	R/W	When the ADC data is shifted to the right 8 bits and the data is higher than this setting value, the UPPER_THD0_TRGED status will be updated. BIT7 is the sign bit.	0x0
7:0	LOWER_THD0	R/W	When the ADC data is shifted to the right 8 bits and the data is lower than this setting value, the LOWER_THD0_TRGED status will be updated. BIT7 is the sign bit.	0x0

8.5.36 ANA_ADCDATATHD3_2 Register

Table 8-37 ANA_ADCDATATHD3_2 Register

Bit	Name	Type	Contents	Default
31:24	UPPER_THD3	R/W	When the ADC data is shifted to the right 8 bits and the data is higher than this setting value, the UPPER_THD3_TRGED status will be updated. BIT7 is the sign bit.	0x0
23:16	LOWER_THD3	R/W	When the ADC data is shifted to the right 8 bits and the data is lower than this setting value, the LOWER_THD3_TRGED status will be updated. BIT7 is the sign bit.	0x0
15:8	UPPER_THD2	R/W	When the ADC data is shifted to the right 8 bits and the data is higher than this setting value, the	0x0

			UPPER_THD2_TRGED status will be updated. BIT7 is the sign bit.	
7:0	LOWER_THD2	R/W	When the ADC data is shifted to the right 8 bits and the data is lower than this setting value, the LOWER_THD2_TRGED status will be updated. BIT7 is the sign bit.	0x0

8.5.37 ANA_ADCDATATHD_CH Register

Table 8-38 ANA_ADCDATATHD_CH Register

Bit	Name	Type	Contents	Default
31	UPPER_THD3_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD3_CH channel is higher than the threshold value set in UPPER_THD3 0:No 1:Yes	0x0
30	LOWER_THD3_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD3_CH channel is lower than the threshold value set in LOWER_THD3. 0:No 1:Yes	0x0
29	UPPER_THD2_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD2_CH channel is higher than the threshold value set in UPPER_THD2. 0:No 1:Yes	0x0
28	LOWER_THD2_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD2_CH channel is lower than the threshold value set in UPPER_THD2. 0:No 1:Yes	0x0
27	UPPER_THD1_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD1_CH channel is higher than the threshold value set in UPPER_THD1. 0:No 1:Yes	0x0

26	LOWER_THD1_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD1_CH channel is lower than the threshold value set in UPPER_THD1. 0:No 1:Yes	0x0
25	UPPER_THD0_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD0_CH channel is higher than the threshold value set in UPPER_THD0. 0:No 1:Yes	0x0
24	LOWER_THD0_TRGED	R	The bit indicates whether the high 8-bit ADC data of the THD0_CH channel is lower than the threshold value set in UPPER_THD0. 0:No 1:Yes	0x0
23:22	THD3_SEL	R/W	Set the trigger condition for UPPER_THD3 and LOWER_THD3 . 0:THD flag bit is 1. 1:THD flag bit is from 0 to 1. 2:THD flag bit is from 1 to 0. 3:THD flag bit has changed.	0x0
21:20	THD2_SEL	R/W	Same as THD3_SEL	0x0
19:18	THD1_SEL	R/W	Same as THD3_SEL	0x0
17:16	THD0_SEL	R/W	Same as THD3_SEL	0x0
15:12	THD3_CH	R/W	The channel selection of LOWER_THD3 and UPPER_THD3 channel selection. The data from 0 to 15 represents ADC to channel 0 to channel 15.	0x0
11:8	THD2_CH	R/W	Same as THD3_CH	0x0
7:4	THD1_CH	R/W	Same as THD3_CH	0x0
3:0	THD0_CH	R/W	Same as THD3_CH	0x0

8.5.38 ANA_CMPCTL Register

Table 8-39 ANA_CMPCTL Register

Bit	Name	Type	Contents	Default
31:24	PWR_DEB_SEL	R/W	The digital filtering control register for VDDALARM, VDCIN and AVCCDET. 0:no filtering 1:2 x RTCCLK filtering 2:3 x RTCCLK filtering 3:4 x RTCCLK filtering 4:5 x RTCCLK filtering … 255:256 x RTCCLK filtering	0x00
23:22	VDDALARM_CHK_FRQ_SEL	R/W	VDDALARM detects the hardware intermittent enable control. When bit7 of ANA_REG9 is configured to 1, the hardware control takes effect. 0: Never enable, no detection 1:Always enable the detection by the RTCCLK clock frequency. 2: The detection is enabled every 7.8125ms, and it will be disabled automatically after the detection is completed. 3: reserved	0x0
21	CMP2_IO_NODEB	R/W	Comparator 2 output IO (CMP2_O) whether outputs the signal which controlled by filtering. 0: Comparator outputs which after controlled by filtering. 1: Original signal output	0x0
20	CMP2_INT_MASK_EN	R/W	When the CMP2_CNT value exceeds the CMP2_THR threshold and CMP2_THR_EN = 1, it is a selection whether to generate a or more interrupts. 0: An interrupt is generated every time a subtraction occurs 1: An interrupt	0x0

18:19	-	-	Reserved	-
17	CMP1_IO_NODEB	R/W	Comparator 1 output IO (CMP1_O) whether outputs the signal which controlled by filtering. 0: Comparator outputs which after controlled by filtering. 1: Original signal output	0x0
16	CMP1_INT_MASK_EN	R/W	When the CMP1_CNT value exceeds the CMP1_THR threshold and CMP1_THR_EN = 1, it is a selection whether to generate a or more interrupts. 0:An interrupt is generated each time a subtraction occurs. 1:An interrupt	0x0
15:12	CMP2_CHK_NUM	R/W	CMP2 output result judgment window setting Consecutive CMP2_CHK_NUM to 1 for CMP2 original output, and comparator output result to 1. Consecutive CMP2_CHK_NUM to 0 for CMP2 original output, and the comparator output result to 0. Otherwise, the comparator output result remains the same. 0~15:1to 16 times.	0x0
11	CMP2_THR_EN	R/W	CMP2 counter subtracts CMP2_THR enable. 0: Comparator 2 keeps accumulation 1: If the counter value of comparator 2 exceeds CMP2_THR, the counter value is equal to the counter value subtracts CMP2_THR until the counter value is smaller than CMP2_THR.	0x0
10:8	CMP2_CHK_FRQ	R/W	CMP2 data detective frequency. 0: Each RTCCLK cycle to detect once. 1:Each 7.8125ms to detect once. 2:Each 125ms to detect once.	0x0

			3:Each 250ms to detect once. 4:Each 500ms to detect once. 5:reserved 6:reserved 7:reserved	
7:4	CMP1_CHK_NUM	R/W	CMP1 output result judgement window setting. Consecutive CMP1_CHK_NUM to 1 for CMP1 original output, and comparator output result to 1. Consecutive CMP1_CHK_NUM to 0 for CMP1 original output, and the comparator output result to 0. Otherwise, the comparator output result remains the same. 0~15:1 to16 times.	0x0
3	CMP1_THR_EN	R/W	CMP1 counter subtracts CMP1_THR enable. 0: Comparator 1 keeps accumulation 1: If the counter value of comparator 1 exceeds CMP1_THR, the counter value is equal to the counter value subtracts CMP1_THR until the counter value is smaller than CMP1_THR.	0x0
2:0	CMP1_CHK_FRQ	R/W	CMP1 data detective frequency. 0: RTCCLK clock cycle to detect once. 1:Every 7.8125ms to detect once. 2:Every 125ms to detect once. 3:Every 250ms to detect once. 4:Every 500ms to detect once. 5:Reserved. 6:reserved. 7:reserved.	0x0

8.5.39 ANA_CMPTHR Register

Table 8-40 ANA_CMPTHR Register

Bit	Name	Type	Contents	Default
31:16	CMP2_THR	R/W	CMP2 interrupt threshold setting. 0: Every time the counter value of Comparator 2 adds 1, the interrupt flag bit will be set. 1~65535: When the counter value for comparator 2 is greater than threshold, the interrupt flag bit will be set 1.	0x0000
15:0	CMP1_THR	R/W	CMP1 interrupt threshold setting. 0: Every time the counter value of Comparator 1 adds 1, the interrupt flag bit will be set. 1~65535: When the counter value for comparator 1 is greater than threshold, the interrupt flag bit will be set 1.	0x0000

9. ADC Controller

9.1 Introduction

A 12-bit SAR ADC is integrated in the chip, which supports 16-channel input signals. The sampling range of all channels is 0~1.2V without voltage division. In the case of the voltage division, the measurement range of the common channel is 1.2V~3.3V, and the measurement range of the BAT channel is 1.2V~5.2V. ADC sampling channel includes GND, temperature, BAT1, BATRTC voltage and external input signal. ADC clock comes from 6.5536M RCH or PLLL which supports two clock frequencies of 6.5MHz and 400KHz, and the conversion rate is ADC clock frequency/(19+8). The ADC works in the main domain, so the register settings related to the ADC can be maintained in deep sleep mode and it will not be reset.

Note:the ADC clock and the system clock are asynchronous and can be configured independently. When operating the ADC related registers, user needs to wait for at least one ADC clock time to take effect.

9.2 Features

--Supports ADC manual and automatic conversion modes;

--Supports interrupt for ADC conversion completed;

--Supports 16-channel or multi-channel scan function.

9.3 ADC Functional Block Diagram

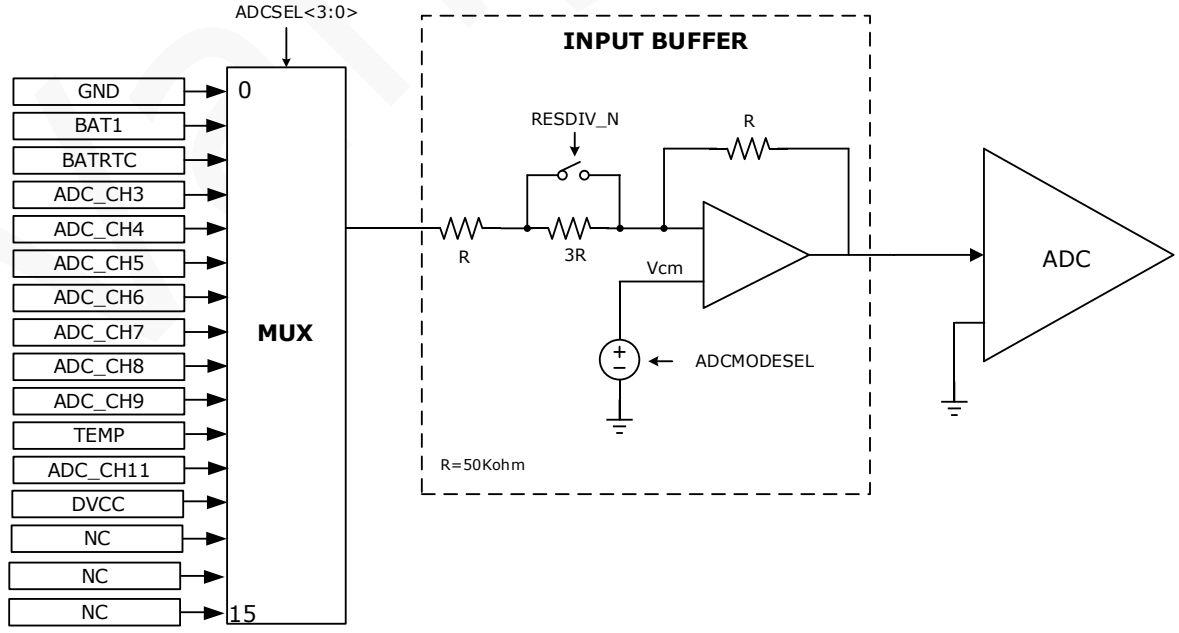


Figure 9-1 ADC Functional Block Diagram

9.4 Register Address

Table 9-1 ANA Control Register (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00
ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG11	W	0x0044	Analog register 11	--
ANA_ADCSTATE	R	0x005C	ADC status register	--
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL0	R/W	0x0068	ADC control register 0	0x00000000
ANA_ADCDATA0	R	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	R	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	R	0x0084	ADC channel 5 data register	--
ANA_ADCDATA6	R	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC channel 9 data register	--
ANA_ADCDATA10	R	0x0098	ADC channel 10 data register	--
ANA_ADCDATA11	R	0x009C	ADC channel 11 data register	--
ANA_ADCDATA12	R	0x00A0	ADC channel 12 data register	--
ANA_ADCDATA13	R	0x00A4	ADC channel 13 data register	--
ANA_ADCDATA14	R	0x00A8	ADC channel 14 data register	--
ANA_ADCDATA15	R	0x00AC	ADC channel 15 data register	--
ANA_ADCDOS	R	0x00C0	ADC self-calibration register DOS	0
ANA_ADCDCPN	R	0x00CC	ADC automatic-calibration register DCPN	0

ANA_ADCDCNM0	R	0x00D8	ADC automatic calibration register DCNM0	0
ANA_ADCDATADMA	R/W	0x00E0	ADC data source for DMA	--
ANA_ADCCTRL1	R/W	0x00E8	ADC control register 1	0x000000C0
ANA_ADCCTRL2	R/W	0x00EC	ADC control register 2	0x00000000
ANA_ADCDATATHD1_0	R/W	0x00F4	ADC threshold control register	0x00000000
ANA_ADCDATATHD3_2	R/W	0x00F8	ADC threshold control register	0x00000000
ANA_ADCDATATHD_CH	R/W	0x00FC	ADC threshold status register	0x00000000

Table 9-2 RTC Controller (RTC Base Address:0x40014800)

Name	Type	Address	Contents	Default
RTC_ADCUCALK	R/W	0x00E8	ADC Ucal K coefficients register with write protection.	0x546A546A
RTC_ADCMACTL	R/W	0x00EC	ADC average control register with write protection	0x70000000
RTC_ADCDTCTL	R/W	0x00F0	ADC data control register	0x80000000

9.5 Register Definition

9.5.1 ANA_REG0 Register

Table 9-3 ANA_REG0 Register

Bit	Name	Type	Contents	Default
7:0	-	R/W	Reserved, and it must be set 0x30.	0

9.5.2 ANA_REG1 Register

Table 9-4 ANA_REG1 Register

Bit	Name	Type	Contents	Default
7	ADCMODESEL	R/W	ADC mode selection When RESDIV_CHx=1, this control bit is valid. 0: Test channel input is not AC cycle 1: Test channel input AC cycle (i.e. ±300mV signal)	0

9.5.3 ANA_REG3 Register

Table 9-5 Functional Descritpion of Each Bit of ANA_REG3

Bit	Name	Type	Contents	Default
3	BGPPD*[1]	R/W	BGP power-down control 0:enable BGP 1:disable BGP	0
4	RCHPD	R/W	High frequency RCH(6.5536M RC) enable/disable control signal 0:enable RCH 1:disable RCH	0

*[1]: RCH, PLL, and ADC are related to BGP. Before enabling RCH, PLL, and ADC, BGP must be enabled. If BGP is not used in the system, user can disable BGP through the BGPPD bit; if BGP is used, user cannot disable BGP through BGPPD at this time. Because the system has a protect function and it will enable BGP again. In sleep or deep sleep mode, user can disable BGP regardless of whether it is used.

9.5.4 ANA_ADCSTATE Register

Table 9-6 ANA_ADCSTATE Register

Bit	Name	Type	Contents	Default
31:5	-	-	Reserved.	0x0
4	RESET	R	The bit represents "RESET" status in ADC interface.	0x0
3	ADC_EN	R	The bit represents "ADC_EN" status in ADC interface.	0x0
2:0	ADCSTATE	R	These bits represent the status for ADC . 0:idle 2:ADC multi-channel automatic conversion 4:ADC multi-channel manual conversion Others:reserved	0x0

9.5.5 ANA_INTSTS Register

Table 9-7 ANA_INTSTS Register

Bit	Name	Type	Contents	Default
21	INTSTS21	R/C	ADC_THD3 data is greater than UPPER_THD3 threshold interrupt flag bit. Read 0:did not occur	0x0

			Read 1:occurred Write 0:no effect Write 1:clear the bit	
20	INTSTS20	R/C	ADC_THD3 data is smaller than LOWER_THD3 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
19	INTSTS19	R/C	ADC_THD2 data is greater than UPPER_THD2 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
18	INTSTS18	R/C	ADC_THD2 data is smaller than LOWER_THD2 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
17	INTSTS17	R/C	ADC_THD1 data is greater than UPPER_THD1 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
16	INTSTS16	R/C	ADC_THD1 data is smaller than LOWER_THD1 threshold interrupt flag bit. Read 0:did not occur Read 1:occurred	0x0

			Write 0:no effect Write 1:clear the bit	
15	INTSTS15	R/C	ADC_THD0 data is greater than UPPER_THD0 threhosld interrupt flag bit. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
14	INTSTS14	R/C	ADC_THD0 data is smaller than LOWER_THD0 threshold interrupt flag bit. Read 0:did not occurr Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
1	INTSTS1	R/C	Interrupt flag bit for ADC automatic conversion is completed. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0
0	INTSTS0	R/C	Interrupt flag bit for ADC automatic conversion is completed by manual control. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0

9.5.6 ANA_INTEN Register

Table 9-8 ANA_INTEN Register

Bit	Name	Type	Contents	Default
21	INTEN21	R/W	ADC_THD3 data is greater than UPPER_THD3 threhosld interrupt enable control.	0x0

			0:disable 1:enable	
20	INTEN20	R/W	ADC_THD3 data is smaller than LOWER_THD3 threshold interrupt enable control. 0:disable 1:enable	0x0
19	INTEN19	R/W	ADC_THD2 data is greater than UPPER_THD2 threshold interrupt enable control. 0:disable 1:enable	0x0
18	INTEN18	R/W	ADC_THD2 data is smaller than LOWER_THD2 threhosld interrupt enable control. 0:disable 1:enable	0x0
17	INTEN17	R/W	ADC_THD1 data is greater than UPPER_THD1 threhosld interrupt enable control. 0:disable 1:enable	0x0
16	INTEN16	R/W	ADC_THD1 data is smaller than LOWER_THD1 threshold interrupt enable control. 0:disable 1:enable	0x0
15	INTEN15	R/W	ADC_THD0 data is greater than UPPER_THD0 threshold interrupt enable control. 0:disable 1:enable	0x0
14	INTEN14	R/W	ADC_THD0 data is smaller than LOWER_THD0 threshold interrupt enable control. 0:disable 1:enable	0x0

1	INTEN1	R/W	Interrupt enable control for ADC automatic conversion completed. 0:Disable 1:Enable	0x0
0	INTEN0	R/W	Interrupt enable control for ADC manual conversion completed. 0: Disable. 1: Enable.	0x0

9.5.7 ANA_ADCCTRL0 Register

Table 9-9 ANA_ADCCTRL0 Regiser

Bit	Name	Type	Contents	Default
31	MTRIG	R/W	ADC manual conversion control. Write 0:no effect Write 1:Enable ADC manual conversion ong time Read 0: Currently ADC manual conversion is completed. Read 1:Currently ADC manual conversion is not completed.	0x0
30:22	-	-	Reserved	0x0
21:20	-	R/W	Reserved, user must set 0x03.	0x0
19	STOP	R/W	Force the ADC conversion to stop. Write 1 in the bit and keeps a ADCCLK time in order to stop the current ADC conversion. Write 0 in the bit before the next ADC conversion starts.	0x0
18:16	AEN	R/W	ADC automatic conversion enable control register 0:Disable ADC automatic conversion 1: ADC automatic conversion is triggered by RTC_ITV and RTC_SITV. 2:ADC automatic conversion is triggered by RTC WKUSEC. 3:ADC automatic conversion is triggered by RTC ALARM. 4: ADC automatic conversion is triggered by the overflow of Timer 0. 5: ADC automatic conversion is triggered by the overflow of Timer 1.	0x0

			6: ADC automatic conversion is triggered by the overflow of Timer 2. 7: ADC automatic conversion is triggered by the overflow of Timer 3.	
15:13	-	-	Reserved.	0x0
12	CLKSRCSEL	R/W	ADC clock source selection. When this register is changed, the hardware logic will stop, and the stop time is 3 ADC clocks. At this time, any ADC operation will be ignored by the hardware. So, user should not operate ADC during this period. 0: 6.5M RCH 1: PLLL	0x0
11:0	-	-	Reserved.	0x0

Table 9-10 ADC Sampling Channel

Channel No.	Measurement Signal
0	GND
1	BAT1
2	BATRTC
3~9	ADC_CHx
10	Temperature
11	ADC_CH11
12	DVCC
13~15	GND

Note: When the temperature channel is selected, the temperature sensor is automatically enabled; when other channels are selected, the temperature sensor is automatically disabled. Through SCAN_CHx to configure channels, ADC supports the single-channel measurement and multi-channels simultaneous scanning.

The setup time of ADC temperature measurement channel needs 2us. When multi- channels are converted to ADC, the temperature measurement channel cannot be included, and the temperature measurement channel must be operated separately.

9.5.8 ANA_ADCCTRL1 Register

Table 9-11 ANA_ADCCTRL1 Register

Bit	Name	Type	Contents	Default
31:16	RESDIV_CHx	R/W	Each bit controls the enable and disable of the resistance divider corresponding to the ADC channel. 0: Disable the resistance divider 1: Enable the resistance divider RESDIV_CH15~0 corresponds to ADC channel 15 to 0 respectively.	0x0
15	UPPER_THD3_EN	R/W	UPPER_THD3 threshold detect control 0:disable 1:enable	0x0
14	LOWER_THD3_EN	R/W	LOWER_THD3 threshold detect control 0:disable 1:enable	0x0
13	UPPER_THD2_EN	R/W	UPPER_THD2 threshold detect control 0:disable 1:enable	0x0
12	LOWER_THD2_EN	R/W	LOWER_THD2 threshold detect control 0:disable 1:enable	0x0
11	UPPER_THD1_EN	R/W	UPPER_THD1 threshold detect control 0:disable 1:enable	0x0
10	LOWER_THD1_EN	R/W	LOWER_THD1 threshold detect control 0:disable 1:enable	0x0
9	UPPER_THD0_EN	R/W	UPPER_THD0 threshold detect control 0:disable 1:enable	0x0
8	LOWER_THD0_EN	R/W	LOWER_THD0 threshold detect control 0:disable 1:enable	0x0

7:0	-	R/W	Reserved, user must set to 0x02.	0XC0

9.5.9 ANA_ADCCTRL2 Register

Table 9-12 ANA_ADCCTRL2 Register

Bit	Name	Type	Contents	Default
31:16	SCAN_CHx	R/W	Each bit represents the enable or disable of the corresponding channel in the multi-channel ADC scan mode. 0: Disable 1: Enable SCAN_CH15~0 corresponds to ADC channels 15~0 respectively. When SCAN_CHx is all 0, the multi-channel ADC scan channel is the full scan of the first 12 channels.	0x0
15	-	R/W	Reserved, user must set 1.	0x0
14:12	-	R/W	Reserved, user must set 0.	0x0
11	CONV_ERR	R	ADC conversion error flag bit. It represents whether the error occurs during the conversion. 0:No error occurred during the conversion time 1:An error occurred during the conversion time.	0x0
10	CAL_ERR	R	ADC automatic calibration error flag bit. It represents whether the error occurs during the automaticcalibration. 0:No error occurred during the self-calibration time. 1:An error occurred during the automatic calibration.	0x0
9	CONV_ERR_CLR	R/C	Write 1 in the bit to reset CONV_ERR to 0. Write 0 in the bit to clear it.	0x0
8	CAL_ERR_CLR	R/C	Write 1 in the bit to reset CONV_ERR to 0. Write 0 in the bit to clear it.	0x0

7	ADC_CAL_DONE	R	The flag bit for ADC automatic calibration is completed. 1: ADC automatic calibration is completed.. 0: ADC automatic calibration is not completed. This bit is cleared to 0 after DPORST (PMU_STS[6]) reset or ADC RESET (ANA_ADCCTRL2[1]) occurs.After ADC self-calibration is enabled, user needs to wait for at least one ADC clock to query the flag bit to ensure that there is enough time to refresh the bit.	0x0
6	ADC_EN_TRG_CAL	R/W	ADC automatic calibration enable control bit 1: Write 1 in ADC_EN(ANA_ADCCTRL2[0]) to trigger the ADC automaticcalibration. 0: Write 0 in ADC_EN(ANA_ADCCTRL2[0]) will not trigger the ADC automatic calibration.	0x0
5	BUSY	R	The flag bit for whether ADC is busy. 1: ADC is busy, ADC is automatic calibration, sampling or converting now. 0: ADC is not busy. ADC is idle forautomatic calibration, sampling or conveting now.	0x0
4	-	R/W	Reserved, user must set 1.	0x0
3:2	-	R/W	Reserved, user must set 0.	0x0
1	RESET	R/W	In addition to the automatic calibration register, reset the ADC digital circuit and maintain 1 ADCCLK time. 0: normal work 1: Reset	0x0
0	ADC_EN	R/W	ADC is enabled and sampled by the falling edge of MCLK. 0: Disable the ADC, the ADC is in a low-power shutdown status, and the automatic calibration register is not reset. 1: Enable ADC. After ADC is configured, because it takes time to establish the analog buffer. So, after enabling the	0x0

			ADC, the software needs to wait for 100us before operating the ADC conversion. To disable ADC, that is, write 0 in ADC_EN, please follow the procedure below. a) Before writing 0 in ADC_EN, make sure that ADC_State is idle. b) After ADC_State is idle, write 0 in ADC_EN. c) Ensure that the ADC_EN status of the ADC_State register is 0.	

9.5.10 ANA_ADCDATATHD1_0 Register

Table 9-13 ANA_ADCDATATHD1_0 Register

Bit	Name	Type	Contents	Default
31:24	UPPER_THD1	R/W	When the ADC data is signed to the right by 8 bits and the data is higher than this set value, the UPPER_THD1_TRGED status is updated. BIT7 is the sign bit.	0x0
23:16	LOWER_THD1	R/W	When the ADC data is signed to the right by 8 bits and the data is lower than this setting value, the LOWER_THD1_TRGED status is updated. BIT7 is the sign bit.	0x0
15:8	UPPER_THD0	R/W	When the ADC data is signed to the right by 8 bits and the data is higher than this setting value, the UPPER_THD0_TRGED status is updated. BIT7 is the sign bit.	0x0
7:0	LOWER_THD0	R/W	When the ADC data is signed to the right by 8 bits and the data is lower than this setting value, the LOWER_THD0_TRGED status is updated. BIT7 is the sign bit.	0x0

9.5.11 ANA_ADCDATATHD3_2 Register

Table 9-14 ANA_ADCDATATHD3_2 Register

Bit	Name	Type	Contents	Default
31:24	UPPER_THD3	R/W	When the ADC data is signed to the right by 8 bits and the data is higher than this setting value, the	0x0

			UPPER_THD3_TRGED status is updated. BIT7 is the sign bit.	
23:16	LOWER_THD3	R/W	When the ADC data is signed to the right by 8 bits and the data is lower than this setting value, the LOWER_THD3_TRGED status is updated. BIT7 is the sign bit.	0x0
15:8	UPPER_THD2	R/W	When the ADC data is signed to the right by 8 bits and the data is higher than this setting value, the UPPER_THD2_TRGED status is updated. BIT7 is the sign bit.	0x0
7:0	LOWER_THD2	R/W	When the ADC data is signed to the right by 8 bits and the data is lower than this setting value, the LOWER_THD2_TRGED status is updated. BIT7 is the sign bit.	0x0

9.5.12 ANA_ADCDATATHD_CH Register

Table 9-15 ANA_ADCDATATHD_CH Register

Bit	Name	Type	Contents	Default
31	UPPER_THD3_TRGED	R	Indicates whether the ADC data of the THD3_CH channel is higher than the UPPER_THD3 setting threshold. 0:No 1:Yes	0x0
30	LOWER_THD3_TRGED	R	Indicates whether the ADC data of the THD3_CH channel is lower than the LOWER_THD3 setting threshold. 0:No 1:Yes	0x0
29	UPPER_THD2_TRGED	R	Indicates whether the ADC data of the THD2_CH channel is higher than the UPPER_THD2 setting threshold. 0:No 1:Yes	0x0
28	LOWER_THD2_TRGED	R	Indicates whether the ADC data of the THD2_CH channel is lower than the LOWER_THD2 setting threshold.	0x0

			0:No 1:Yes	
27	UPPER_THD1_TRGED	R	Indicates whether the ADC data of the THD1_CH channel is higher than the UPPER_THD1 setting threshold. 0:No 1:Yes	0x0
26	LOWER_THD1_TRGED	R	Indicates whether the ADC data of the THD1_CH channel is lower than the LOWER_THD1 setting threshold. 0:No 1:Yes	0x0
25	UPPER_THD0_TRGED	R	Indicates whether the ADC data of the THD0_CH channel is higher than the UPPER_THD0 setting threshold. 0:No 1:Yes	0x0
24	LOWER_THD0_TRGED	R	Indicates whether the ADC data of the THD0_CH channel is lower than the LOWER_THD0 setting threshold. 0:No 1:Yes	0x0
23:22	THD3_SEL	R/W	Set the trigger condition for UPPER_THD3 and LOWER_THD3. 0:THD flag bit is 1 1:THD flag bit is from 0 to 1 2:THD flag bit is from 1 to 0 3:THD flag bit has changed	0x0
21:20	THD2_SEL	R/W	Same as THD3_SEL	0x0
19:18	THD1_SEL	R/W	Same as THD3_SEL	0x0
17:16	THD0_SEL	R/W	Same as THD3_SEL	0x0
15:12	THD3_CH	R/W	The channel selection of LOWER_THD3 and UPPER_THD3 channel selection.	0x0

			The data from 0 to 15 represents ADC to channel 0 to channel 15.	
11:8	THD2_CH	R/W	Same as THD3_CH	0x0
7:4	THD1_CH	R/W	Same as THD3_CH	0x0
3:0	THD0_CH	R/W	Same as THD3_CH	0x0

9.5.13 ANA_ADCDATAx Register

Table 9-16 ANA_ADCDATAx Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	-
15:0	ADCDATA	R	The ADC conversion result data register is 16's complement. DATA0: Store the conversion result of ADC channel 0. DATA1: Store the conversion result of ADC channel 1. … DATA15: Store the conversion result of ADC channel 15.	0x--

9.5.14 ANA_ADCDOS Register

Table 9-17 ANA_ADCDOS Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved	0
8:0	DOS	R	ADC automatic calibration register DOS	

9.5.15 ANA_ADCDCPN Register

Table 9-18 ANA_ADCDCPN Register

Bit	Name	Type	Contents	Default
31:27	DCPN4	R	ADC automatic calibration register DCPN4	
26:18	DCPN3	R	ADC automatic calibration register DCPN3	
17:9	DCPN2	R	ADC automatic calibration register DCPN2	
8:0	DCPN1	R	ADC automatic calibration register DCPN1	

9.5.16 ANA_ADCDCNM0 Register

Table 9-19 ANA_ADCDCNM0 Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved	0
8:0	NM0	R	ADC automatic calibration register NM0	0

9.5.17 ANA_ADCDATADMA Register

Table 9-20 ANA_ADCDATADMA Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	ADCDATA_DMA	R	ADC data source for DMA	0

9.5.18 RTC_ADCUCALK Register

Table 9-21 RTC_ADCUCALK Register

Bit	Name	Type	Contents	Default
31:16	UCAL_K3	R/W	Temperature measurement channel UCAL K3, user must set 0x599A.	0x546A
15:0	UCAL_K1	R/W	Temperature measurement channel UCAL K1, user must set 0x599A.	0x546A

9.5.19 RTC_ADCMACTL Register

Table 9-22 RTC_ADCMACTL Register

Bit	Name	Type	Contents	Default
31:28	-	-	Reserved	0x7
27	-	R/W	Reserved, user must set 0.	0x0
26:24	-	-	Reserved	00
23:20	SKIP_SAMPLE	R/W	The register is used to ignore the number of ADC output sampling points at the beginning. SKIP_SAMPLE [3:0] = x: ignore the number of (x) sampling points at the beginning. 0:Igonre 0 sampling point 4:Ignore 4 sampling points	0x0

			8:Ignore 8 sampling points 12:Ignore 12 sampling points Others:Reserved	
19	-	-	Reserved	0x0
18:16	AVERAGE_SAMPLE	R/W	The number of average sampling points 0:2 points average 1:4 points average 2:8 points average 3:16 points average 4:32 points average 5:64 points average 6:reserved 7:reserved	0x0
15:0	AVERAGE_CHx	R/W	Each bit separately controls the average enable of the corresponding channel 1:enable 0:disable AVERAGE_CH15~0 corresponds to ADC channel 15~0.	0x0

9.5.20 RTC_ADCDTCTL Register

Table 9-23 RTC_ADCDTCTL Register

Bit	Name	Type	Contents	Default
31:30	ENDED_IN2ADC_CONVERT	R/W	Must set 2	0x2
29:0	-	-	Reserved	-

9.6 ADC Self-Calibration Instructions

- ADC Self-calibration Description:

1. ADC self-calibration requires 4096 ADC clock.
2. When DPORST (PMU_STS[6]) reset occurs, and ADC RESET (ANA_ADCCTRL2[1]) and AVCC voltage is lower than 2.2V, the self-calibration data will be lost, that is, ANA_ADCDOS or ADC_CAL_DONE becomes 0. After returning to normal state, it also needs to be operated the self-calibration again.

3. ADC is powered by AVCC, and the normal working voltage should not be lower than 2.2V. It is recommended to query the AVCC voltage (ANA_CMPOUT[10]) before the self-calibration to determine whether the conditions are met.
4. Before starting the ADC self-calibration work, it is recommended to fill in the recommended default value of the ADC peripheral register once.

- Process flow for ADC self-calibration:

1. Set ADC clock
   a) Select a 6.5M ADC clock.
   b) Maintain at least a ADC clock.
2. Disable ADC functions.
   a) Set ADC_EN = 0, and maintain at least a ADC clock.
   b) Set CAL_ERR_CLR=1, and maintain at least a ADC clock.
   c) Set CAL_ERR_CLR=0, and maintain at least a ADC clock.
3. Stop the current ADC conversion
   a) Wait MTRIG = 0, wait the current ADC conversion is completed by manual control.
   b) Set STOP = 1, and maintain at least a ADC clock.
   c) Set STOP = 0, and maintain at least a ADC clock.
4. Reset ADC
   a) Set RESET = 1, and maintain at least a ADC clock.
   b) Set RESET = 0, and maintain at least a ADC clock.
5. Enable ADC self-calibration
   a) Set ADC_EN_TRG_CAL = 1, and at least maintain a ADC clock.
   b) Set ADC_EN = 1, and at least maintain a ADC clock.
6. Wait ADC self-calibration to complete.
   a) Wait at least a ADC clock.
   b) Wait at least ADC_CAL_DONE is 1.
7. Disable ADC self-calibration
   a) Set ADC_EN_TRG_CAL = 0, and maintain at least a ADC clock.
   b) Set ADC_EN = 0, and maintain at least a ADC clock.
8. Detect CAL_ERR
   a) If 0, self-calibration is completed

b) If 1, self-calibration is failed:

Set CAL_ERR_CLR=1 to reset CAL_ERR to 0, and maintain at least a ADC clock.

Set CAL_ERR_CLR=0, and maintain at least a ADC clock.

From the step 3, to restart the self-calibration.

- The related registers description:

ADC_EN = ANA_ADCCTRL2[0];

CAL_ERR_CLR = ANA_ADCCTRL2[8];

MTRIG = ADCCTRL0[31]

STOP = ADCCTRL0[19]

RESET = ADCCTRL2[1]

ADC_EN_TRG_CAL = ANA_ADCCTRL2[6];

ADC_CAL_DONE = ANA_ADCCTRL2[7];

CAL_ERR = ANA_ADCCTRL2[10].

9.7 BAT and Periphals Voltage Measurement

In V85XXP, ADC can measure the external signal via external input pins, and it also can measure the voltage of signals such as BAT1 and BATRTC.ADC operation mode: automatic or manual trigger the ADC converstion.

ADC sampling channel selection: single or multiple channels.

ADC voltage division mode: no or resistance division. There is additional consumption for resistance division, and the power is consumed by this circuit:

$$P = U_D \times I_D = (V_{IN} - V_{CM}) \times \frac{V_{IN} - V_{CM}}{R_1 + 3R_1} \qquad \textbf{Equation 9-1}$$

Among, V_{CM}=1.2V, R_1=50Kohm.

Measure the external voltage (ADC_CHx) including the channel 3, 4, 5, 6, 7, 8, 9, 11.

Measure the voltage channel of battery, that is, BAT1, BATRTC (channel 1 and 2.)

Table 9-24 The Configuration Range for ADC Input Signal of Different Ranges

Singal Input			
Configuration	**Min.**	**Max.**	**Description**
Channel voltage is smaller than 1.2V.	0.0	1.2	ADC_CHx is smaller than 1.2V.
Channel voltage is greater than1.2V.	1.2	3.3	ADC_CHx is greater than 1.2V.
Battery (BAT1/BATRTC)	1.2	5.2	Battery (BAT1/BATRTC)

Channel input AC cycle (i.e. signal±300mV)	-0.3	0.4	Channel input AC cycle (i.e. signal±300mV)

Table 9-25 Configuration for DC and BAT Voltage

Register	Set	Description
ADCMODESEL	0	Is the AC mode or not?
SKIP_SAMPLE		Ignore points, it is recommended to ignore 4 points.
AVERAGE_SAMPLE		The average points
RESDIV_CHx		Is the resistance division or not?
SCAN_CHx		Scan channel selection

Table 9-26 Configuration for AC Voltage

Register	Set	Description
ADCMODESEL	1	Is the AC mode or not?
SKIP_SAMPLE		Ignore points, it is recommended to ignore 4 points.
AVERAGE_SAMPLE		The average points
RESDIV_CHx	1	Is the resistance division or not?
SCAN_CHx		Scan channel selection

Table 9-27 Voltage Mesurement and Formula

Channel	Divider Mode	Signal range (V)	Formula
ADC_CHx	No divider	-0.2~1.2	$V_{DC} = a1 * X \div 100000000 + b1 \div 100000000$+offset1÷1000
	Resistive	1.2~3.3	$V_{DC} = a2 * X \div 100000000 + b2 \div 100000000$+offset2÷1000
BAT1 channels	Resistive	2.5~5.2	$V_{DC} = a3 * X \div 100000000 + b3 \div 100000000$+offset3÷1000
BATRTC channels	Resistive	0.7~5.2	$V_{DC} = a4 * X \div 100000000 + b4 \div 100000000$+offset4÷1000

ADC coefficients a and b are stored in the Info information area with double backups. User needs to check whether the a, b, and offset storage area parameters used to store the ADC coefficients are legal. The calculation formula is shown in **Table 9-27 Voltage Mesurement and Formula**. The a, b, and offset of the ADC coefficients selects the data at different locations according to different power systems. Please refer to **Table 4-21 Info Message Register**, and the address range is 0x00080C00~0x00080CD8.

The calculation formula as below:

$$X = ADC\_DATAx \qquad \textbf{Equation 9-2}$$

Among: ADCDATAx is the value in (0x40014270+4x)(16bit) address. X is the corresponding channel number 0-15.

9.8 Temperature Measurement

CH10 is the temperature measurement channel, the measurement range: -40~+85°C.

Table 9-28 Temperature Measurement

Register	Set	Description
ADCMODESEL	0	AC mode selected
SKIP_SAMPLE		Ignore points, it is recommended to ignore 4 points.
AVERAGE_SAMPLE	>0	The average points:4 and 4 points above
RESDIV_CH10	0	Whether the resistance division in channel 10

The steps for temperature measurement are as below:

1. Make sure that the ADC has successfully completed at least one calibration. Set manual or automatic to trigger ADC.
2. Set ADC

   The ADC clock selection is 6.5M RCH, and the internal average should be at least 4 points. If the temperature difference is within 0.1℃, it is recommended to set the internal 64-point average, and use the software to calculate the 64 averages. Select channel 10 and enable the ADC. Manual trigger/auto to trigger the ADC conversion.
3. When waiting the value of INTSTS0 (manual trigger)/INTSTS1 (automatic trigger) of the ANA_INTSTS (0x40014260) register is 1, read the value of the register ANA_ADCDATA10 (0x40014298).Calculation Temperature(T): (unit: 1/256°C). T is a 16's complement, the actual temperature value is equal to T/256.0. For example, 0x1880 represents 24.5°C.

Formula:

$$T = (P0 * ((X_m * X_m) >> 16) + P1 * X_m + P2) >> 8 \qquad \textbf{Equation 9-3}$$

X_m is a ADC value in calibration point (such as 25℃).

P0 is a value in 0x80D10(16bit) address.

P1 is a value in 0x80D12(16bit) address.

P2 is a value which calculated by the following formula:

$$P2 = P2' + (T_r - T_m) * 256 \qquad \textbf{Equation 9-4}$$

P2' is a value in 0x80D14(32-bit) address.

T_r is a value in 0x80D80(32b-it) address.

T_m is a value in 0x80D84(32-bit) address.

10. Comparator

10.1 Introduction

V85XXP is gathered in two comparators which is used to compare the magnitude of analog signal. There are some following modes:

- The positive terminal of the comparator is connected to pin CMP_P, and the negative terminal signal is connected to pin CMP_N.
- The positive terminal of the comparator is connected to pin CMP_P, and the negative terminal signal is connected to BGPREF or VREF;
- The positive terminal of the comparator is connected to pin CMP_N, and the negative terminal signal is connected to BGPREF or VREF;
- The positive terminal of the comparator is connected to pins BAT1/BATRTC, and the negative terminal signal is connected to BGPREF or VREF.

Each comparator has 20mV voltage Hysteresis.

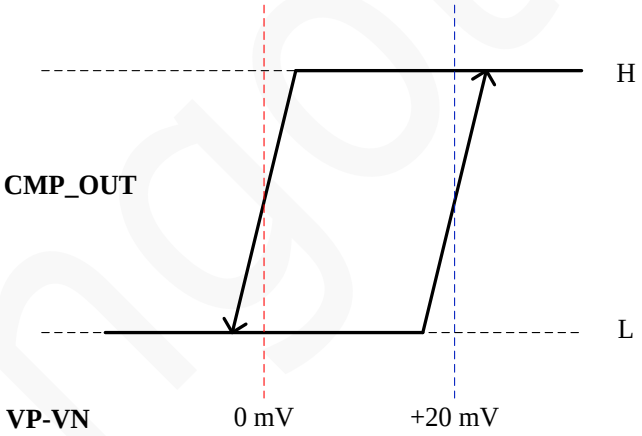


Figure 10-1 The Hysteresis for Comparator

10.2 Features

--Interrupt/ wake up function;

--Multiple comparison modes;

--Counter for comparator;

--It can also work in the sleep mode.

10.3 Functional Block Diagram

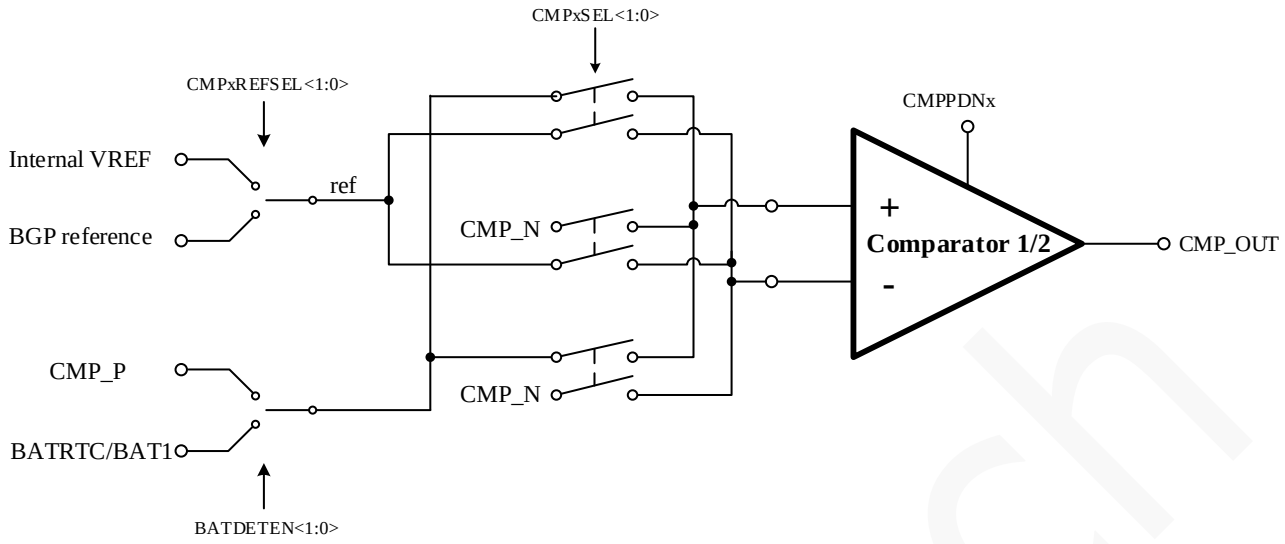


Figure 10-2 Functional Block Diagram for Comparator

10.4 Register Address

Table 10-1 ANA Register (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REGF	R/W	0x003C	Analog register F	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Compare result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x00
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x00
ANA_CMPCTL	R/W	0x006C	Compare control register	0x00000000
ANA_CMPCNT1	R/C	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter	0x00000000
ANA_CMPTHR	R/W	0x00E4	CMP1/CMP2 threshold register	0x0000

10.5 Register Definition

10.5.1 ANA_REG2 Register

Table 10-2 ANA_REG2 Register

Bit	Name	Type	Contents	Default
1:0	CMP1SEL[1:0]	R/W	CMP1 signal source selection 00:CMP1_P and REF 01:CMP1_N and REF 1*:CMP1_P and CMP1_N	0
3:2	CMP2SEL[1:0]	R/W	CMP2 signal source selection 00:CMP2_P and REF 01:CMP2_N and REF 1*:CMP2_P and CMP2_N	0
4	CMP1REFSEL	R/W	REF selection of CMP1 0:VREF 1:BGPREF	0
5	CMP2REFSEL	R/W	REF selection of CMP2 0:VREF 1:BGPREF	0

10.5.2 ANA_REG3 Register

Table 10-3 ANA_REG3 Register

Bit	Name	Type	Contents	Defaul
1	CMP1PDN	R/W	CMP1 power-down control signal 0:disable CMP1 1:enable CMP1	0
2	CMP2PDN	R/W	CMP2 power-down control signal 0:disable CMP2 1:enable CMP2	0
3	BGPPD*[1]	R/W	BGP power-down control signal 0:enable BGP 1:disable BGP	0
*[1]:RCH, PLL, and ADC are related to BGP. Before enabling RCH, PLL, and ADC, BGP must be enabled. If BGP is not used in the system, user can disable BGP through the BGPPD bit; if BGP is used, user cannot disable BGP through BGPPD at this time. Because the system has a protection function and it will enable BGP again. In sleep or deep sleep mode, user can disable BGP regardless of whether it is used.				

10.5.3 ANA_REG5 Register

Table 10-4 ANA_REG5 Register

Bit	Name	Type	Contents	Default
1:0	CMP1IT[1:0]	R/W	Bias current selection of CMP1 00:20nA; 01:100nA; 1*:500nA;	0
3:2	CMP2IT[1:0]	R/W	Bias current selection of CMP2 00:20nA; 01:100nA; 1*:500nA;	0
Note: When CMP bias current is smaller, the power consumption is lower and the propagation delay time is longer; when CMP bias current is larger, the power consumption is higher and the propagation delay time is shorter.				

10.5.4 ANA_REGF Register

Table 10-5 ANA_REGF Register

Bit	Name	Type	Contents	Default
1	BATRTCDETEN	R/W	BATRTC is connected to the positive input of comparator 2. 0: no connect; 1:connect	0
0	BAT1DETEN	R/W	BAT1 is connected to the positive input terminal of comparator 1 0:no connects; 1:connect	0

10.5.5 ANA_CTRL Register

Table 10-6 ANA_CTRL Register

Bit	Name	Type	Contents	Default
23:22	CMP2DEB	R/W	Comparator 2 debounce control register. 0:no de-bounce 1:2 x RTCCLK cycle debounce. 2:3 x RTCCLK cycle debounce. 3:4 x RTCCLK cycle debounce. When the debounce is enabled, the input signal is valid only when the signal has not changed in multiple cycles of the RTCCLK clock. In addition, the response time of wake-up and interrupt will be delayed until the signal is valid. The circuit can work in all modes, including the sleep and deep sleep mode.	0x0
21:20	CMP1DEB	R/W	Comparator 1 debounce control register. 0:no de-bounce 1:2 x RTCCLK cycle debounce. 2:3 x RTCCLK cycle debounce. 3:4 x RTCCLK cycle debounce. When the debounce is enabled, the input signal is valid only when the signal has not changed within multiple cycles of the RTCCLK clock. In addition, the response time of wake-up and interrupt will	0x0

			be delayed until the signal is valid. The circuit can work in all modes, including the sleep and deep sleep mode.	
19:18	-	-	Reserved	0x0
3:2	CMP2SEL	R/W	The register is used to control the counter accumulation of comparator 2. 0:disable 1:Rising edge of comparator 2 output 2:Falling edge of comparator 2 output 3:Both edges of comparator 2 output.	0x0
1:0	CMP1SEL	R/W	The register is used to control the counter accumulation of comparator 1. 0:disable 1:Rising edge of comparator 1 output 2:Falling edge of comparator 1 output 3:Both edges of comparator 1 output.	0x0

10.5.6 ANA_CMPOUT Register

Table 10-7 ANA_CMPOUT Register

Bit	Name	Type	Contents	Default
3	CMP2	R	The bit shows the result of comparator 2.	0x0
2	CMP1	R	The bit shows the result of comparator 1.	0x0

10.5.7 ANA_INTSTS Register

Table 10-8 ANA_INTSTS Register

Bit	Name	Type	Contents	Default
3	INTSTS3	R/C	The interrupt flag bit of CMP2, the interrupt generative condition is controlled by ANA_CTRL, ANA_CMPCTL and ANA_CMPTHR. Read 0:did not occur Read 1:occurred Write 0:no effective Write 1:clear the bit	0x0

2	INTSTS2	R/C	The interrupt flag bit of CMP1, the interrupt generative condition is controlled by ANA_CTRL, ANA_CMPCTL and ANA_CMPTHR. Read 0:did not occur Read 1:occurred Write 0:no effective Write 1:clear the bit	0x0

10.5.8 ANA_INTEN Register

Table 10-9 ANA_INTEN Register

Bit	Name	Type	Contents	Default
3	INTEN3	R/W	CMP2 interrupt and wake-up enable control. 0:Disable CMP2 interrupt and wake-up 1:Enable CMP2 interrupt and wake-up.	0x0
2	INTEN2	R/W	CMP1 interrupt and wake-up enable control. 0:Disable CMP1 interrupt and wake-up. 1:Enable CMP1 interruptand wake-up.	0x0

10.5.9 ANA_CMPCNTx Register

Table 10-10 ANA_CMPCNTx Register

Bit	Name	Type	Contents	Default
31:0	CNT	R/C	According to the setting of CMPxSEL, this register stores the number of occurrences of comparator X events. For example, when CMPxSEL is set to 1, when the CMPx output changes from 0 to 1, then this counter will add 1. This register can be cleared by writing 0, but it is only valid when the corresponding CMPPDNx is set to 1 (that is, when the corresponding comparator is also enabled).	0x0000000

10.5.10 ANA_CMPCTL Register

Table 10-11 ANA_CMPCTL Register

Bit	Name	Type	Contents	Default

21	CMP2_IO_NODEB	R/W	The comparator 2 output IO (CMP2_O) whether outputs a signal that has been controlled by filter. 0: Comparator output after filtering. 1: Original signal output.	0x0
20	CMP2_INT_MASK_EN	R/W	When CMP2_CNT values exceeds CMP2_THR threshold and CMP2_THR_EN = 1, it is generated one or multiple interrupts. 0:An interrupt is generated each time a subtraction occurs 1:An interrupt	0x0
18:19	-	-	Reserved	
17	CMP1_IO_NODEB	R/W	The comparator 1 output IO (CMP1_O) whether outputs a signal that has been controlled by filter. 0: Comparator output after filtering. 1: original signal output	0x0
16	CMP1_INT_MASK_EN	R/W	When CMP1_CNT values exceeds CMP1_THR threshold and CMP1_THR_EN = 1, it is generated one or multiple interrupts. 0:An interrupt is generated each time a subtraction occurs 1:An interrupt	0x0
15:12	CMP2_CHK_NUM	R/W	CMP2 output result judgement window setting. Consecutive CMP2_CHK_NUM to 1 for CMP2 original output, and comparator output result to 1. Consecutive CMP2_CHK_NUM to 0 for CMP2 original output, and the comparator output result to 0. Otherwise, the comparator output result remains the same.	0x0

			0~15:1to 16 times.	
11	CMP2_THR_EN	R/W	CMP2 counter subtracts CMP2_THR enable. 0: Comparator 2 keeps accumulation 1: If the counter value of comparator 2 exceeds CMP2_THR, the counter value is equal to the counter value subtracts CMP2_THR until the counter value is smaller than CMP2_THR.	0x0
10:8	CMP2_CHK_FRQ	R/W	CMP2 data detective frequency. 0: Each RTCCLK cycle to detect once. 1:Each 7.8125ms to detect once. 2:Each 125ms to detect once. 3:Each 250ms to detect once. 4:Each 500ms to detect once. 5:reserved. 6:reserved. 7:reserved.	0x0
7:4	CMP1_CHK_NUM	R/W	CMP1 output result judgement window setting. Consecutive CMP1_CHK_NUM to 1 for CMP1 original output, and the comparator output result to 1. Consecutive CMP1_CHK_NUM to 0 for CMP1 original output, and the comparator output result to 0. Otherwise, the comparator output result remains the same. 0~15:1 to 16 times.	0x0
3	CMP1_THR_EN	R/W	CMP1 counter subtracts CMP1_THR enable. 0: Comparator 1 keeps accumulation 1: If the counter value of comparator 1 exceeds CMP1_THR, the counter	0x0

			value is equal to the counter value subtracts CMP1_THR until the counter value is smaller than CMP1_THR.	
2:0	CMP1_CHK_FRQ	R/W	CMP1 data detect frequency. 0: RTCCLK cycle to detect once. 1:Each 7.8125ms to detect once. 2:Each 125ms to detect once. 3:Each 250ms to detect once. 4:Each 500ms to detect once.	0x0

10.5.11 ANA_CMPTHR Register

Table 10-12 ANA_CMPTHR Register

Bit	Name	Type	Contents	Default
31:16	CMP2_THR	R/W	CMP2 interrupt threshold setting. 0: Every time the counter value of Comparator 2 adds 1, the interrupt flag bit will be set. 1~65535: When the counter value for comparator 2 is greater than threshold, the interrupt flag bit will be set 1.	0x0000
15:0	CMP1_THR	R/W	CMP1 interrupt threshold setting. 0: Every time the counter value of Comparator 1 adds 1, the interrupt flag bit will be set. 1~65535: When the counter value for comparator 1 is greater than threshold, the interrupt flag bit will be set 1.	0x0000

11. TinyADC Controller

11.1 Introduction

TinyADC (2-bit ADC) controller is used to control TinyADC function of V85XXP which is low-precision analog-to-digital converter. TinyADC is powered by AVCC, and it is located in the main power domain. So, it also can work normally even in the deep-sleep mode.

11.2 Features

--To generate TinyADC interrupt.

11.3 Functional Block Diagram

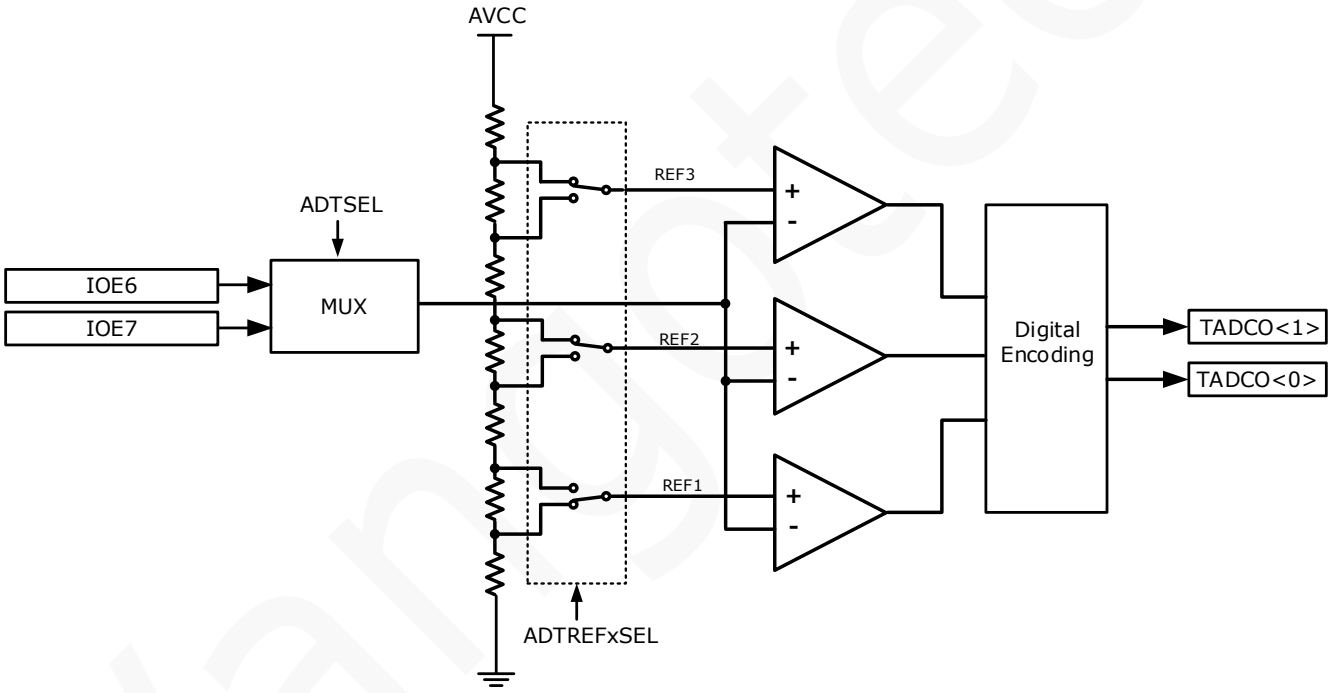


Figure 11-1 Functional Block Diagram of Analog Controller

11.4 Register Address

Table 11-1 ANA Controller (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REGF	R/W	0x003C	Analog control register 15	0x00
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000

ANA_MISC	R/W	0x00B8	Analog misc control register	0x00

11.5 Register Definition

11.5.1 ANA_REGF Register

Table 11-2 ANA_REGF Register

Bit	Name	Type	Contents	Default
3	ADTPDN	R/W	TADC switch control 0:power-down 1:power-on	0
4	ADTSEL	R/W	TADC signal input source selection 0:from IOE6 input 1:from IOE7 input	0
5	ADTREF1SEL	R/W	TADC reference voltage 1 0:0.9V 1:0.7V	0
6	ADTREF2SEL	R/W	TADC reference voltage 2 0:1.8V 1:1.6V	0
7	ADTREF3SEL	R/W	TADC reference voltage 3 0:2.7V 1:2.5V	0

11.5.2 ANA_CMPOUT Register

Table 11-3 ANA_CMPOUT register is related to TADC

Bit	Name	Type	Contents	Default
15:14	TADCO	R	TADC output. For example, if the three bits of ADTREFxSEL are configured as 0, then: Signal<0.9V, TADCO output 0. Signal >0.9V && <1.8V, TADCO output 1.	-

			Signal >1.8V && <2.7V, TADCO output 2. Signal >2.7V, TADCO output 3.	

11.5.3 ANA_INTSTS Register

Table 11-4 ANA_INTSTS register is related to TADC

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved	0
13	INTSTS13	R/C	TADC threshold interrupt flag bit. When TADC is rising or falling, and the change value from the previous cycle is greater than the threshold (TADCTH), the interrupt flag bit will be set. Read 0:did not occur Read 1:occurred Write 0:no effect Write 1:clear the bit	0x0

11.5.4 ANA_INTEN Register

Table 11-5 ANA_INTEN Register

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved	0
13	INTEN13	R/W	TADC interrupt and wake-up enable (TADC changes exceed threshold.) 0:Disable TADC interrupt and wake-up. 1:Enable TADC interrupt and wake-up.	0x0

11.5.5 ANA_MISC Register

Table 11-6 ANA_MISC Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0
5:4	TADCTH	R/W	TADC threshold setting. This register controls the threshold for TADC to generate an interrupt. TADC clock selects internal 32K RC as the clock source to sample external signals.	0x0

			When the interrupt of TADC is enabled and the difference between the sampled values of two consecutive cycles is greater than the threshold, INTSTS13 will be set to 1 and an interrupt will be generated.	
3:0	*[1]	-	Reserved	0

***[1]**:ANA_MISC register bit [3:0]must write 0.

12. Watchdog

12.1 Introduction

V85XXP integrates a 16-bit watchdog (WDT) circuit, and the WDT clock source is RTCCLK. When a program runaway occurs, the timer will overflow and generate a system reset. The reset flag is checked through BIT7 of the PMU_STS register, please refer to **Table 6-7**. The WDT reset level is the same as the POR reset level, which can provide a reset inside the chip.

12.2 Features

--WDT cycle reset can be selected to: 2 sec /4 sec /8 sec /16 sec;

--WDT possessed passwords protective function in order to avoid the illegal access of WDT.

12.3 WDT Status in Different Mode

The enable or disable of the WDT is controlled by hardware or software in different modes. The following table shows the status control of the WDT when MODE=1 (PMU_STS bit24). When MODE=0, the WDT is invalid in any mode.

Table 12-1 WDT Status in Different Modes (MODE=1)

WDT	Power Mode				
	RTC only	Deep-sleep mode	Sleep Mode	IDLE	Work
enable/disable	invalid	ON(WDTEN=1) OFF(WDTEN=0)	ON(WDTEN=1) OFF(WDTEN=0)	ON(WDTEN=1) OFF(WDTEN=0)	ON(WDTEN=1) OFF(WDTEN=0)

WDT	Exit RTC only mode	Wake-up from the Different Modes		
		Deep-sleep Mode	Sleep Mode	IDLE
Enable /disable	ON	ON	ON	ON(WDTEN=1) OFF(WDTEN=0)

12.4 Register Address

Table 12-2 PMU_WDT Controller (PMU Base Address:0x40014000)

Name	Type	Address	Contents	Default
PMU_WDTPASS	R/W	0x0040	Watchdog unlocked register	0x00000000
PMU_WDTEN	R/W	0x0044	Watchdog timer enable register	0x1

PMU_WDTCLR	R/C	0x0048	Watchdog clear register	0x0000

12.5 Register Definition

12.5.1 PMU_WDTPASS Register

Table 12-3 PMU_WDTPASS Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved	0
0	UNLOCK	R	This bit indicates that the WDT enable register has been unlocked and the WDT enable control register is ready to be set. Writing 0xAA5555AA to this register will set the flag bit UNLOCK to 1. Any write operation to the PMU control register (including ICE) will clear this bit. Therefore, the user should set PMU_WDTEN immediately after the UNLOCK bit is set, otherwise the unlocking steps should only be continued again.	0x0

12.5.2 PMU_WDTEN Register

Table 12-4 PMU_WDTEN Register

Bit	Name	Type	Contents	Default
31:4	-	-	Reserved	0
3:2	WDTSEL	R/W	Set the counting period for WDT. 0:2 sec 1:4 sec 2:8 sec 3:16 sec Before setting the register, the UNLOCK bit should be set to 1(in PMU_WDTPASS).	0x0
1	-	-	Reserved	0
0	WDTEN	R/W	The bit represents the WDT timer enable. Before setting the register, the UNLOCK bit should be set to 1(in PMU_WDTPASS).	0x1

12.5.3 PMU_WDTCLR Register

Table 12-5 PMU_WDTCLR Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	WDTCNT	R/C	This register represents the current count value of the WDT timer. When the timer count reaches the limit value set by WDTSEL, a WDT system reset will be occurred. Therefore, users should clear this timer regularly to prevent the WDT reset. Write 0x55AAAA55 to this bit to clear this register. This register is automatically cleared to 0 in debug mode, that is, WDT reset will not occur in debug mode.	0x0

13. RTC Controller

13.1 Introduction

RTC Controller is used to control time calculation, manual calibration, real-time clock wake-up, and alarm wake-up functions. Time calibration function realizes the automatic calculation and leap year detection by year, month, week, day, hour, minute and seconds. Manual calibration can detect temperature and adjust seconds clock cycle to compensate the clock offset which is caused by temperature variation. There are also multi-second, multi-mintues, multi-hours and automatic wake-up timer which is embedded in RTC engine.

13.2 Features

--Support BCD time calculation from second to year.

--Automatic leap year detection.

--Support frequency compensation for crystal clock.

--Programmable multiple wake-up source.

--Initialize calibration by manual for customer.

--RTC division reaches the low-power consumption in sleep mode/ deep-sleep mode.

--Support alarm function.

--Support millisecond function.

13.3 Functional Block Diagram

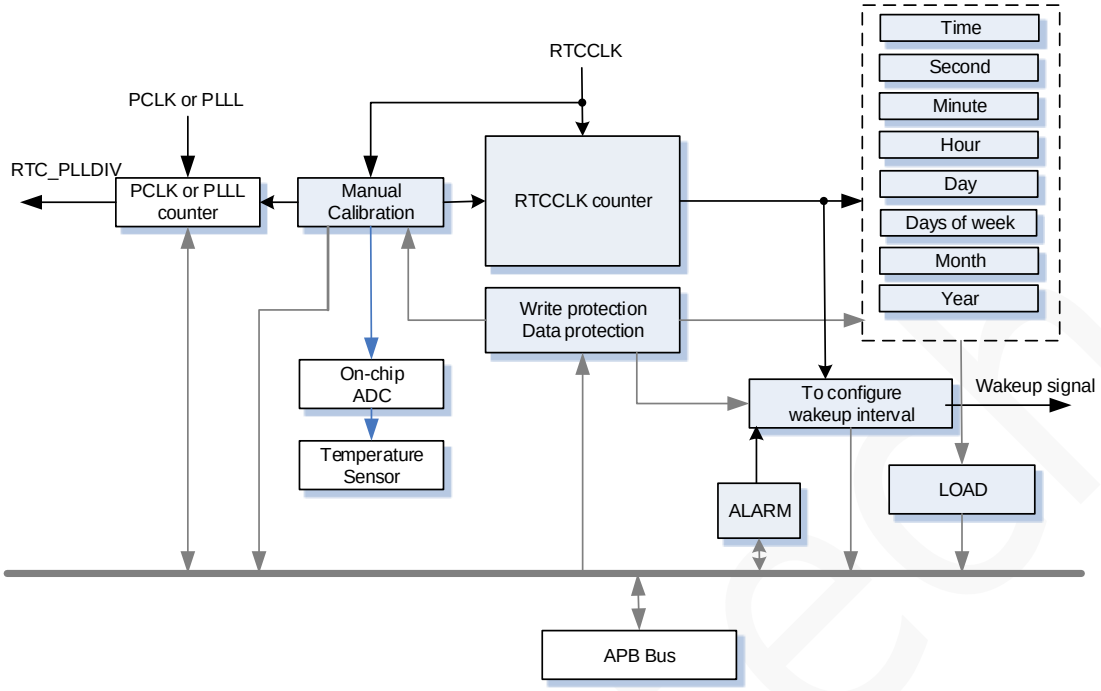


Figure 13-1 Functional Block Diagram for RTC Controller

13.4 RTC Reading and Writing Mode

13.4.1 RTC Writing Operation

In V85XXP, some RTC controller are protected by writing operation including RTC time controller, RTC calibration register and other registers. The details please refer to **Table 13-1**.

MCU should follow below steps to complete the writing operation for RTC register:

1. User must wait BSY (bit 1 of RTC_CE register) to 0 in order to ensure RTC idle status.
2. Write 0x5AA55AA5 in RTC_PWD regiser, enable the access for RTC_CE register.
3. Write 0xA55AA55B in RTC_CE register, enable the writing operation for write protective register.
4. Configure the write protective register. The time register from RTC_SEC to RTC_YEAR should be configured together (RTC_TIME should be configured together at the same time.)
5. Write 0x5AA55AA5 in RTC_PWD register, enable the access for RTC_CE.
6. Write 0xA55AA55A in RTC_CE register, clear CE(bit0 of RTC_C register) flag bit. When CE is cleared from 1 to 0, BSY (bit 1 of RTC_CE register) set 1. When CE is cleared to 0, the value of write protective register will update to RTC core. The updating steps should be 3x32 cycles, around 100μs.

7. After step 6, user should wait BSY (bit 1 of RTC_CE register) automatic clear 0 in order to ensure the updating completely.

RTC registers which are not protected by writing operation, MCU can directly do the writing operation.

13.4.2 Reading Operation for RTC

RTC timing register is protected by reading operation, the details please refer to **Table 13-1**.

MCU should follow below steps to complete reading protection for RTC timing register:

1. User should wait BSY (bit 1 of RTC_CE register) to 0 in order to ensure RTC to idle statuse.
2. MCU reads RTC_LOAD register, the reading operation of RTC_LOAD register starts, and BSY (bit 1 of RTC_CE register) will immediately set 1. After the reading operation, BSY will automati clear 0. Reading operation should be 3x32 cycles, around 100μs.
3. After the reading operation of RTC_LOAD register is completed, the current time will be locked. User can read RTC_SEC~RTC_YEAR, RTC_TIME register to obtain the timing value.

RTC registers which are not protected by reading operation, MCU can directly process the reading operation.

13.5 Register Address

The following table shows the register address and location. "Writing Protection" means the register can write only when CE set 1. When CE clear 0, the value will br updated to RTC register. "Reading Protection" means after RTC_LOAD reading operation happened and BSY clear 0, these register values will be updated.

Table 13-1 RTC Register (RTC Base Adress:0x40014800)

Name	Type	Address	Contents	Default	Writing Protection	Reading Protection
RTC_SEC	R/W	0x0000	RTC register in seconds	--	√	√
RTC_MIN	R/W	0x0004	RTC register in minutes	--	√	√
RTC_HOUR	R/W	0x0008	RTC register in hours	--	√	√
RTC_DAY	R/W	0x000C	RTC register in days	--	√	√
RTC_WEEK	R/W	0x0010	RTC register in weeks	--	√	√
RTC_MON	R/W	0x0014	RTC register in months	--	√	√
RTC_YEAR	R/W	0x0018	RTC register in years	--	√	√
RTC_TIME	R/W	0x001C	RTC register for milliseconds counter	--	√	√
RTC_WKUSEC	R/W	0x0020	RTC second wake-up register	0x00	√	

RTC_WKUMIN	R/W	0x0024	RTC minute wake-up register	0x00	√	
RTC_WKUHOUR	R/W	0x0028	RTC hour wake-up register	0x00	√	
RTC_WKUCNT	R/W	0x002C	RTC counter wake-up register	0x0000000	√	
RTC_CAL	R/W	0x0030	RTC calibration register	--	√	
RTC_DIV	R/W	0x0034	RTC_PLLDIV division register	0x0000000		
RTC_CTL	R/W	0x0038	RTC_PLLDIV divide control register	0x0		
RTC_ITV	R/W	0x003C	RTC ITV wake-up register	0x0	√	
RTC_SITV	R/W	0x0040	RTC SITV wake-up register	0x00	√	
RTC_PWD	R/W	0x0044	RTC password control register	0x00000000		
RTC_CE	R/W	0x0048	RTC write enable control register	0x0		
RTC_LOAD	R/W	0x004C	RTC read enable control register	--		
RTC_INTSTS	R/W	0x0050	RTC interrupt status register	0x000		
RTC_INTEN	R/W	0x0054	RTC interrupt status register	0x000		
RTC_PSCA	R/W	0x0058	RTC clock pre-scaler control register	0x0	√	
RTC_ACTI	R/W	0x0084	Crytstal vertex temperature register	0x1800	√	
RTC_ACF200	R/W	0x0088	RTC 200*frequency register	0x640000	√	
RTC_ACP0	R/W	0x0090	RTC parametric 0 register	0x0000	√	
RTC_ACP1	R/W	0x0094	RTC parametric 1 register	0x0000	√	
RTC_ACP2	R/W	0x0098	RTC parametric 2 register	0x0000	√	
RTC_ACP3	R	0x009C	RTC parametric 3 register	0x0000		
RTC_ACP4	R/W	0x00A0	RTC parametric 4 register	0x0000	√	
RTC_ACP5	R/W	0x00A4	RTC parametric 5 register	0x0000	√	
RTC_ACP6	R/W	0x00A8	RTC parametric 6 register	0x0000	√	
RTC_ACP7	R/W	0x00AC	RTC parametric 7 register	0x0000	√	
RTC_ACK0	R/W	0x00B0	RTC parametric k0 register	0x0000	√	
RTC_ACK1	R/W	0x00B4	RTC parametric k1 register	0x0000	√	
RTC_ACK2	R/W	0x00B8	RTC parametric k2 register	0x0000	√	

RTC_ACK3	R/W	0x00BC	RTC parametric k3 register	0x0000	√	
RTC_ACK4	R/W	0x00C0	RTC parametric k4 register	0x0000	√	
RTC_WKUCNTR	R	0x00CC	Record the current WKUCNT value	0x000000		
RTC_ACKTEMP	R/W	0x00D0	RTC control register for K coefficient temperature sections	0x3C2800EC	√	
RTC_ALARMSEC	R/W	0x00D8	RTC second register with alarm function	0x0000	√	
RTC_ALARMMIN	R/W	0x00DC	RTC minute register with alarm function	0x0000	√	
RTC_ALARMHOUR	R/W	0x00E0	RTC hour register with alarm function	0x0000	√	
RTC_ALARMCTL	R/W	0x00E4	RTC alarm control register	0x0000	√	
RTC_ADCUCALK	R/W	0x00E8	ADC Ucal K coefficient register	0x546A546A	√	
RTC_ADCMACTL	R/W	0x00EC	ADC average control register	0x70000000	√	
RTC_ADCDTCTL	R/W	0x00F0	ADC data control	0x80000000	√	

13.6 Register Definition

13.6.1 RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

The time register is BCD code, in which 7 to 4-bit represent the 10's digits, and 3 to 0-bit are the 1's digit. The value of these registers can be set only when CE is high, and only when CE is cleared from 1 to 0, it will it be updated to the RTC core. To read the current time, user should read the RTC_LOAD register and wait for BSY to be cleared, otherwise the invalid value of the register time read is invalid.

Table 13-2 RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0000	RTC_SEC, 0~59	-	S40	S20	S10	S8	S4	S2	S1
0x0004	RTC_MIN, 0~59	-	M40	M20	M10	M8	M4	M2	M1
0x0008	RTC_HOUR, 0~23	-	-	H20	H10	H8	H4	H2	H1
0x000C	RTC_DAY, 1~31	-	-	D20	D10	D8	D4	D2	D1
0x0010	RTC_WEEK, 0~6	-	-	-	-	-	W4	W2	W1
0x0014	RTC_MON, 1~12	-	-	-	Mo10	Mo8	Mo4	Mo2	Mo1

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0018	RTC_YEAR, 00~99	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
Default Value		X	X	X	X	X	X	X	X

"Week" can only be set by user, RTC will not detect it automatically. After initialization, RTC will add "Week" counting automatically. For example, when user set 2010/01/01 as Friday, RTC will detect 2010/01/02 as Saturday. W4/W2/W1:000, Sunday; 001, Monday; 010, Tuesday; 011, Wednesday; 100, Thursday; 101, Friday; 110, Saturday.

System only can set the last two digits of year; for example, in 2020, RTC_YEAR should be set 0b00010000.

13.6.2 RTC_TIME Register

Table 13-3 RTC_TIME Register

Bit	Name	Type	Contents	Default
31:22	-	-	Reserved	-
21:0	TIME	R/W	millisecond counter value	0x0

13.6.3 RTC_WKUSEC Register

Table 13-4 RTC_WKUSEC Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0
5:0	WKUSEC	R/W	The register is used to seconds wake-up function. The wake-up cycle is (WKUSEC+1)*1 sec. When INTEN[2] is 1 and the internal second wake-up count is reaching the target, INTSTS[2] will be set 1, and the wake-up signal will be effective to PMU controller. For the first interrupt which generated by WKUSEC, it may have＜1 second error if the new WKUSEC value is not equal to the current WKUSEC value. If the new WKUSEC is equal to current WKUSEC, the first interrupt time may have 0~(WKUSEC+1) variation. To avoid this problem, set an alternative value (such as 0) to this register and update it with RTC_CE operation. Then, set the correct value to it.	0x00

13.6.4 RTC_WKUMIN Register

Table 13-5 RTC_WKUMIN Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0
5:0	WKUMIN	R/W	The register is used to minutes wake-up function. The wake-up cycle is (WKUSEC+1)*1 min. When INTEN[3] is 1 and the internal minute wake-up count is reaching the target, INTSTS[3] will be set 1, and the wake-up signal will be effective to PMU controller. For the first interrupt which generated by WKUMIN, it may have＜1 minute error if the new WKUSEC value is not equal to the current WKUSEC value. If the new WKUMIN is equal to current WKUMIN, the first interrupt time may have 0~(WKUMIN+1) variation. To avoid this problem, set an alternative value (such as 0) to this register and update it with RTC_CE operation. Then, set the correct value to it.	0x00

13.6.5 RTC_WKUHOUR Register

Table 13-6 RTC_WKUHOUR Register

Bit	Name	Type	Contents	Default
31:5	-	-	Reserved	0
4:0	WKUHOUR	R/W	The register is used to hours wake-up function. The wake-up cycle is (WKUHOUR+1)*1 min. When INTEN[4] is 1 and the internal hour wake-up count is reaching the target, INTSTS[4] will be set 1, and the wake-up signal will be effective to PMU controller. For the first interrupt which generated by WKUHOUR, it may have＜1 minute error if the new WKUHOUR value is not equal to the current WKUHOUR value. If the new WKUHOUR is equal to current WKUHOUR, the first interrupt time may have 0~(WKUHOUR+1) variation. To avoid this problem, set an alternative value (such as 0) to this register and update it with RTC_CE operation. Then, set the correct value to it.	0x00

13.6.6 RTC_WKUCNT Register

Table 13-7 RTC_WKUCNT Register

Bit	Name	Type	Contents	Default

31:26	-	-	Reserved	0
25:24	CNTSEL	R/W	The register is used to configure WKUCNT counter clock. When PSCA is 0: 0:Counter clock is 32768Hz. 1:Counter clock is 2048Hz. 2:Counter clock is 512Hz. 3:Counter clock is 128Hz. When PSCA is 1: 0:Counter clock is 8192Hz. 1:Counter clock is 2048Hz. 2:Counter clock is 512Hz. 3:Counter clock is 128Hz.	0x0
23:0	WKUCNT	R/W	The register is used to control 32K counter wake-up function. The wake-up time is (WKUCNT+1)*counter clock cycle. The counter clock is controlled by CNTSEL. When INTEN[6] is 1 and the internal wake-up count is reaching WKUCNT target, it will generate WKUCNT cycle counter interrupt or wake-up signal.	0x000000

13.6.7 RTC_CAL Register

Table 13-8 RTC_CAL Register

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved	0
13:0	CAL	R/W	RTC 32768 calibration register. This register is a 14 bits complement. RTC will calibrate every 30 seconds. The internal counter will count from 1st to 29th seconds and count as [32768-(CAL-1)] at the 30th second, so that the average 1-second pulse within 30 seconds can be accurate 1 second pulse. The PPM resolution of the CAL register is 1.02ppm, and the adjustable range is ±8332.3ppm (±12 minutes/day). When manually calibrating, the value of this register needs to be updated manually.	--

13.6.8 RTC_DIV Register

Table 13-9 RTC_DIV Register

Bit	Name	Type	Contents	Default
31:26	-	-	Reserved.	0
25:0	RTCDIV	R/W	The register is used to configure the output frequency of RTC_PLLDIV. Set IOA3(PMU_IOASEL bit3 is set to 1) or IOA7(PMU_IOASEL bit7 is set to 1) is the output function of RTC_PLLDIV. At the same time, it set RTC_PLLDIV output enable (RTC_CTL bit2), and the corresponding IOA output the division pulse. The output frequency is CLK/(2*(RTCDIV+1)). When RTC is manually calibrated, the register also should be manually updated, too. The source of CLK is PCLK or PLLLwhich is configured by RTCPLLCLKSEL (RTC_CTL bit4).	0x0000000

13.6.9 RTC_CTL Register

Table 13-10 RTC_CTL Register

Bit	Name	Type	Contents	Default
31:5	-	-	Reserved.	0
4	RTCPLLCLKSEL	R/W	RTC_PLLDIV clock source selection 0：PCLK 1：PLLL	0x0
3	-	-	Reserved.	0
2	RTCPLLOE	R/W	RTC_PLLDIV output enable. The register is used to control RTC_PLLDIV divider output. 0:disable RTC_PLLDIV output. 1:enable RTC_PLLDIV output. RTC_PLLDIV output pin is IOA[3] or IOA[7], it should be set IOA3 (PMU_IOASEL bit3 set 1) or IOA7 (PMU_IOASEL bit7 set 1) which enable RTC_PLLDIV output.	0x0
1:0	-	-	Reserved.	0x0

13.6.10 RTC_ITV Register

Table 13-11 RTC_ITV Register

Bit	Name	Type	Contents	Default
31:3	-	-	Reserved.	
2:0	ITV	R/W	The register is used to control RTC wake-up and interrupt interval. The register operates idenoendently with RTC_WKUSEC, RTC_WKUMIN, RTC_WKUHOUR and RTC_WKUCNT, the setting of time interval is triggered by seconds, minutes, hours and days. Therefore, the first interrupt trigger may have a certain error. For example, ITV is set to 2, it wil bel triggerred once/hour. The current time of chip is 10:58, then chip will be triggered after 2 minutes (11:00 o'clock) rather than triggered at 11:58. After, it will be triggered at 12:00, 13:00 o'clock, each o'clock will trigger the register once. 000: 1 sec; 001: 1 minute; 010: 1 hour; 011: 1 day(00:00 o'clock); 100: 500 milliseconds; 101: 250 milliseconds; 110: 125 milliseconds; 111: 62.5 milliseconds (When SITVEN of RTC_SITV register is 0.)	0x0

13.6.11 RTC_SITV Register

Table 13-12 RTC_SITV Register

Bit	Name	Type	Description	Default
31:7	-	-	Reserved.	-
6	SITVEN	R/W	Set RTC_ITV register to 0x07, then set the flag bit 1, then it can set the wake-up interval via the register bit [5:0].	0x0
5:0	SITV	R/W	Set wake-up interval in seconds. The actual wake-up interval is (bit[5:0]+1) sec.	0x00

13.6.12 RTC_PWD Register

Table 13-13 RTC_PWD Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0

0	PWDEN	R	The register is used to protect the access of RTC_CE register. Before accessing RTC_CE, please write the password 0x5AA55AA5 in RTC_PWD register. Therefore, PWDEN will set 1. Any writing operation for RTC_CE register will automatic clear 0 to PWDEN. It means before accessing RTC_CE register next time, user should write 0x5AA55AA5 in this register again.	0x0

13.6.13 RTC_CE Register

Table 13-14 RTC_CE Register

Bit	Name	Type	Contents	Default
31:2	-	-	Reserved.	0
1	BSY	R	This bit is set to 1 immediately after CE is cleared from 1 to 0 or when the RTC_LOAD register is read by the CPU, indicating that the RTC updating process or RTC read process is in progress, and this bit is automatically cleared after the read or write operation is completed. User can query this bit to check whether the RTC updating is completed. The updating or read operation requires about 3 x 32K cycles, about 100μs.	0x0
0	CE	R	This register is used to unlock access to the RTC register. This bit can only be set after PWDEN is set to 1 and 0xA55AA55B is written in the RTC_CE register. After the bit is set to 1, the RTC register can be programmed, but the register value will only be updated when the bit is cleared. To clear this bit, set PWDEN to 1, and write 0xA55AA55A to the RTC_CE register.	0x0

13.6.14 RTC_LOAD Register

Table 13-15 RTC_LOAD Register

Bit	Name	Type	Contents	Default
31:0	LOAD	R	After user reads the register, the current time will be stored in the time register. User can read the data from RTC_SEC to RTC_YEAR and RTC_TIME register. The reading operation will take 3x32K cycles, and user can check whether the reading operation is completed via BSY (RTC_CE bit1). The data read from the	--

			register is invalid.	

13.6.15 RTC_INTSTS Register

Table 13-16 RTC_INTSTS Register

Bit	Name	Type	Contents	Default
31:11	-	-	Reserved.	--
10	INTSTS10	R/C	alarm interrupt flag bit	0x0
9	-	-	Reserved.	0x0
8	INTSTS8	R/C	Interrupt status 8. When the illegal writing RTC_CE register, the bit set 1. The illegal writing means when BSY set 1, CE(RTC_CE bit0) will be set 1 or read RTC_LOAD register. Write 1 to clear the bit.	0x0
7	-	-	Reserved	0x0
6	INTSTS6	R/C	Interrupt status 6. When 32K counter reaches the setting cycle by WKUCNT, the bit set 1. Write 1 to clear the bit.	0x0
5	INTSTS5	R/C	Interrupt status 5. When time arrived midnight(00:00), the bit set 1. Write 1 to clear the bit.	0x0
4	INTSTS4	R/C	Interrupt status 4. When time arrived the interrupt cycle in hours which set by WKUHOUR, the bit set 1. Write 1 to clear the bit.	0x0
3	INTSTS3	R/C	Interrupt status 3. When time arrived the interrupt cycle in minutes which set by WKUMIN, the bit set 1. Write 1 to clear the bit.	0x0
2	INTSTS2	R/C	Interrupt status 2. When time arrived the interrupt cycle in seconds, the bit set 1. Write 1 to clear the bit.	0x0
1	INTSTS1	R/C	Interrupt status 1. When the illegal time is wrote in RTC register, the bit set 1. Write 1 to clear the bit.	0x0
0	INTSTS0	R/C	Interrupt status 0. When time arrived the interrupt cycle which is set by ITV and SITV, the bit set 1. Write 1 to clear the bit.	0x00

13.6.16 RTC_INTEN Register

Table 13-17 RTC_INTEN Register

Bit	Name	Type	Contents	Default
31:11	-	-	Reserved.	0
10	INTEN10	R/W	Interrupt enable 10. When the bit is 1 and INTSTS10 is set 1,an alaram interrupt will be generated..	0x0
9	-	-	Reserved.	--
8	INTEN8	R/W	Interrupt enable 8. When the bit is 1 and INTSTS 8 is set 1, it will generate illegal access interruption.	0x0
7	-	-	Reserved.	0x0
6	INTEN6	R/W	Interrupt enable 6. When the bit is 1 and INSTS 6 is set 1, it will generate WKUCNT cycle counting interrupt or wake-up signal.	0x0
5	INTEN5	R/W	Interrupt status 5. When the bit is 1 and INTSTS 5 is set 1, it will generate midnight counting interrupt or wake-up signal.	0x0
4	INTEN4	R/W	Interrupt enable 4. When the bit is 1 and INSTS 4 is set 1, a multi-hour interrupt or wake-up signal will be generated.	0x0
3	INTEN3	R/W	Interrupt enable 3. When the bit is 1 and INSTS 3 is set 1, it will generate interrupt or wake-up signal in minutes.	0x0
2	INTEN2	R/W	Interrupt enable 2. When the bit is 1 and INTSTS 2 is set 1, it will generate interrupt or wake-up signal in seconds.	0x0
1	INTEN1	R/W	Interrupt enable 1. When the bit is 1 and INTSTS 1 is set 1, the illegal format time write the interrupt or the wake-up signal will be generated	0x0
0	INTEN0	R/W	Interrupt enable 0. When the bit is 1 and INTSTS0 is set 1, an interrupt or wake-up signal set by ITV and SITV will be generated.	0x00

13.6.17 RTC_PSCA Register

Table 13-18 RTC_PSCA Register

Bit	Name	Type	Contents	Default
31:2	-	-	Reserved.	0
1:0	PSCA	R/W	The register is used to control RTCCLK prescaler.	0x0

			When RTCCLK clock frequency is slow down, the power consumption in sleep or deep sleep mode can be significantly reduced. 0: without prescaler, RTCCLK is 32768Hz. 1: 1/4 prescaler, RTCCLK is 9182Hz. 2~3: reserved. When the register is set 1, all module which used RTCCLK will be affected. The hardware will automatically adjust the RTC counter clock and LCD frame rate, sothere is no need to manually modify the settings. However, the input clock of RTC_WKUCNT will be changed, user should modify the related setting. UART32K baud rate register needs to be calculated again according to the newset RTCCLK.	

13.6.18 RTC_ACTI Register

Table 13-19 RTC_ACTI Register

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved.	0
13:0	ACTI	R/W	ACTI represents the Ti value of the crystal central temperature during RTC calibration. The value needs to be downloaded from Info. The register is a 16's complementwhere the upper 8 bits represents the integer numbers and the lower 8 bits represents the decimal numbers. For example, 0x1880 represents 24.5℃: 24.5*256=6272=0x1880; 0xE780 represents -24.5℃: ~0x1880+1=0xE780. The register is protected by RTC writing operation and should be a fixed value when ACEN is 1.	0x1800

13.6.19 RTC_ACF200 Register

Table 13-20 RTC_ACF200 Register

Bit	Name	Type	Contents	Default
31:26	-	-	Reserved.	0
25:0	F200	R/W	The register is used to calculate the value of	0x640000

			PLLDIV.i.e. user uses PCLK as the clock source of RTCPLLDIV, that is, PCLK/2. When PCLK is 13107200, PCLK/2=6553600=0x640000. i.e. user uses PLLL as the clock source of RTCPLLDIV, that is, PLLL/2. When PLLL is 26214400, PLLL/2=13107200=0xC80000.	

13.6.20 RTC_ACP0 Register

Table 13-21 RTC_ACP0 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Sign extension bit.	-
15:0	P0	R/W	P0 is a 16 bits complement which is used to control temperature. Need to download data from Info. The details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x0000

13.6.21 RTC_ACP1 Register

Table 13-22 RTC_ACP1 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Sign extension bit.	-
15:0	P1	R/W	P1 is a 16 bits complement which is used to control temperature.Needs to download from Info. The details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x0000

13.6.22 RTC_ACP2 Register

Table 13-23 RTC_ACP2 Register

Bit	Name	Type	Contents	Default
31:0	P2	R/W	P2 is a 32 bits complement which is used to control temperature. Needs to download data from Info. The details please refer to **Table 13-39**. The register calculation formula is as below, P2=P2'+(Tr-Tm)*256 P2' is 0x80D14 address value in Info. Tr is 0x80D80 address value in Info. Tm is 0x80D84 address value in Info.	0x00000000

			The register is protected by RTC writing operation.	

13.6.23 RTC_ACP3 Register

Table 13-24 RTC_ACP3 Register

Bit	Name	Type	Contents	Default
31:0	P3	R	P3 is a 16 bits complement which is used to frequency calibration. Needs to download data from Info. The details please refer to **Table 13-39**. There are 4 temperature value separated to 5 sections in RTC_ACKTEMP register, match the section where the corrected temperature T is, determine the temperature section coefficient RTC_ACKx (x=0~4) and store the coefficient in the RTC_ACP3 register. The register is protected by RTC writing operation.	0x00000000

13.6.24 RTC_ACP4 Register

Table 13-25 RTC_ACP4 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Sign extension.	-
15:0	P4	R/W	P4 is crystal offset in room temperature which is a 16 bits complement. It needs to download data from Info, the details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x0000

13.6.25 RTC_ACP5 Register

Table 13-26 RTC_ACP5 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Sign extension.	-
15:0	P5	R/W	P4 is a 16 bits complement which is used to calibrate values in RTC_CAL register. Needs to download data from Info, the details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x0000

13.6.26 RTC_ACP6 Register

Table 13-27 RTC_ACP6 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Sign extension.	-
15:0	P6	R/W	P6 is a 16 bits complement which is used to calculate values in RTC_DIV register. P6 calculation formula is as below: P6=a*P6', P6' is a downloading value in Info. Detais please refer to **Table 13-39**. i.e. user uses PCLK as the clock source of RTCPLLDIV, a = PCLK/6553600. i.e. user uses PLLL as the clock source of RTCPLLDIV, a = PLLL/6553600. The register is protected by RTC writing operation.	0x0000

13.6.27 RTC_ACP7 Register

Table 13-28 RTC_ACP7 Register

Bit	Name	Type	Contents	Value
31:16	-	-	Sign extension.	-
15:0	P7	R/W	P7 is a 16 bits complement which is used to frequency calibration .Needs to download data from Info. The details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x0000

13.6.28 RTC_ACKx Register

Table 13-29 RTC_ACKx Registe

Bit	Name	Type	Contents	Default
31:16	-	-	Sign extension.	-
15:0	ACK	R/W	RTC_ACK0~RTC_ACK4 is a 16 bits complement which is used to frequency calibration. Needs to download data from Info. The details please refer to **Table 13-38**. For RTC manual tempearature compensation, user should according to the calculation "T" to manually match RTC_ACKx (x=0~4) , and calibrate the frequency in accordance with RTC_ACKx. It no needs to store value in RTC_ACP3 register. The register is protected by RTC writing operation. RTC_ACK0:T< KTEMP1。	0x0000

			RTC_ACK1:KTEMP1≤T< KTEMP2。 RTC_ACK2:KTEMP2≤T< KTEMP3。 RTC_ACK3:KTEMP3≤T< KTEMP4。 RTC_ACK4:T≥KTEMP4。	

13.6.29 RTC_WKUCNTR Register

Table 13-30 RTC_WKUCNTR Register

Bit	Name	Type	Contents	Default
31:24	-	-	Reserved.	0
23:0	WKUCNTR	R	Record the current value from WKUCNT. Value increase, the data range: 0~WKUCNT. It will accumulate from 0 until reaches the setting value of WKUCNT. After the setting value, it will start from 0 to accumulate again.	--

13.6.30 RTC_ACKTEMP Register

Table 13-31 RTC_ACKTEMP Register

Bit	Name	Type	Contents	Default
31:24	KTEMP4	R/W	KTEMP4 is a 8-bit complement which is used to control the temperature section 4. Needs to download from Info, the details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x3C
23:16	KTEMP3	R/W	KTEMP3 is a 8-bit complement which is used to control the temperature section 3. Needs to download from Info, the details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x28
15:8	KTEMP2	R/W	KTEMP2 is a 8-bit complement which is used to control the temperature section 2. Needs to download from Info, the details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0x00
7:0	KTEMP1	R/W	KTEMP1 is a 8-bit complement which is used to control the temperature section 1. Needs to download from Info, the details please refer to **Table 13-39**. The register is protected by RTC writing operation.	0xEC

13.6.31 RTC_ALARMSEC Register

Table 13-32 RTC_ALARMSEC Register

Bit	Name	Type	Contents	Default
31:7	-	-	Reserved.	-
6:0	ALARMSEC	R/W	The register is used to set seconds of alarm.	0x0

13.6.32 RTC_ALARMMIN Register

Table 13-33 RTC_ALARMMIN Register

Bit	Name	Type	Contents	Default
31:7	-	-	Reserved.	-
6:0	ALARMMIN	R/W	The register is used to set minutes of alarm.	0x0

13.6.33 RTC_ALARMHOUR Register

Table 13-34 RTC_ALARMHOU Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved.	-
5:0	ALARMHOUR	R/W	The register is used to set hours of alarm.	0x0

13.6.34 RTC_ALARMCTL Register

Table 13-35 RTC_ALARMCTL Register

Bit	Name	Type	Contents	Default
31:3	-	-	Reserved.	-
2	TIME_CNT_EN	R/W	The register is used to control whether millisecond counter is enabled. 0: disable millisecond counter 1: enable millisecond counter	0x0
1	-	R/W	Reserved, user must set to 1.	0x0
0	ALARM_EN	R/W	The register is used to control whether alarm function is enabled. 0:disable alarm 1:enable alarm	0x0

13.6.35 RTC_ADCUCALK Register

Table 13-36 RTC_ADCUCALK Register

Bit	Name	Type	Contents	Default
31:16	UCAL_K3	R/W	The temperature testing channel UCAL K3. User must set 0x599A.	0x546A
15:0	UCAL_K1	R/W	The temperature testing channel UCAL K1. User must set 0x599A.	0x546A

13.6.36 RTC_ADCMACTL Register

Table 13-37 RTC_ADCMACTL Register

Bit	Name	Type	Contents	Default
31:28	-	-	Reserved.	0x7
27	-	R/W	Reserved, user must set 1.	0
26:24	-	-	Reserved.	0
23:20	SKIP_SAMPLE	R/W	The register is used to ignore the starting numbers of ADC output sampling points. SKIP_SAMPLE[3:0] = x:ignore the starting x sampling points. 0:ignore 0 sampling point. 4:ignore 4 sampling points. 8:ignore 8 sampling points. 12:ignore 12 sampling points. Others:reserved	0x0
19	-	-	Reserved	0x0
18:16	AVERAGE_SAMPLE	R/W	Average the number of sampling points. 0:average for 2 points 1:average for 4 points 2:average for 8 points 3:average for 16 points 4:average for 32 points 5:average for 64 points 6:reserved 7:reserved	0x0

15:0	AVERAGE_CHx	R/W	Each bit is controlled the corresponding channel, the average enable. 1:enable 0:disable AVERAGE_CH15~0 the corresponding ADC channel 15~0.	0x0

13.6.37 RTC_ADCDTCTL Register

Table 13-38 RTC_ADCDTCTL Register

Bit	Name	Type	Contents	Default
31:30	ENDED_IN2ADC_CONVERT	R/W	It must set 2.	0x2
29:0	-	-	Reserved.	-

13.7 Info Parameter Register (related to RTC temperature compensation)

Info information is stored in the area from 0x00080400 as the initial address, which can only be read but not written. All information has double backups The first data in the table is represented by 1, and the second data is represented by 2. Each pieces of data comes with a checksum. The checksum algorithm: add the data of the data items in each piece, and invert the result of the addition.Address data 0x00080800~0x0008085C is written by special programming tool (offline programming and RTC calibration function is enabled). Other data has been written before the product is completed.

Table 13-39 Info Message Register (related to RTC temperature compensation)

Address	Sign	Message	Contents
0x00080800	P4	Crystal offset 1 in room temperature	unit(0.1ppm), lower 16-bit to download to RTC_ACP4 register, such as 0.
0x00080804		Checksum1	INV(SUM(0x80800, 0x80800))
0x00080808	P4	Crystal offset 2 in room temperature	unit(0.1ppm), lower 16-bit to download to RTC_ACP4 register, such as 0.
0x0008080C		Checksum2	INV(SUM(0x80808, 0x80808))
0x00080810	K0	Crystal K0 coefficient 1	Load to RTC_ACK0 register, K0 the calculation formula is as below: K0=B0/1000000*65536, B0 is the segament coefficient of the quadratic function of crystal oscillator curve. For example, the K0 value is 20827.

0x00080814	K1	Crystal K1 coefficient 1	Load to RTC_ACK1 register, K1 the calculation formula is as below: K0=B1/1000000*65536, B1 is the segament coefficient of the quadratic function of crystal curve. For example, the K1 value is 21496.
0x00080818	K2	Crystal K2 coefficient 1	Load to RTC_ACK2 register, K2 the calculation formula is as below: K2=B2/1000000*65536, B0 is the segament coefficient of the quadratic function of crystal curve. For example, the K2 value is22020.
0x0008081C	K3	Crystal K3 coefficient 1	Load to RTC_ACK3 register, K3 the calculation formula is as below: K3=B3/1000000*65536, B3 is the segament coefficient of the quadratic function of crystal curve. For example, the K3 value is24517.
0x00080820	K4	Crystal K4 coefficient 1	Load to RTC_ACK4 register, K4 the calculation formula is as below: K4=B4/1000000*65536, B4 is the segament coefficient of the quadratic function of crystal curve. For example, the K4 value is25257.
0x00080824		Checksum1	INV(SUM(0x80810, 0x80820))
0x00080828	K0	Crystal K0 coefficient 2	Load to RTC_ACK0 register, K0 the calculation formula is as below: K0=B0/1000000*65536, B0 is the segament coefficient of the quadratic function of crystal curve. For example, the K0 value is20827.
0x0008082C	K1	Crystal K1 coefficient 2	Load to RTC_ACK1 register, K1 the calculation formula is as below: K1=B1/1000000*65536, B1 is the segament coefficient of the quadratic function of crystal curve. For example, the K1 value is21496.
0x00080830	K2	Crystal K2 coefficient 2	Load to RTC_ACK2 register, K2 the calculation formula is as below: K2=B2/1000000*65536, B2 is the segament coefficient of the quadratic function of crystal curve. For example, the K2 value is22020.

0x00080834	K3	Crystal K3 coefficient 2	Load to RTC_ACK3 register, K3 the calculation formula is as below: K3=B3/1000000*65536, B3 is the segament coefficient of the quadratic function of crystal curve. For example, the K3 value is24517.
0x00080838	K4	Crystal K4 coefficient 2	Load to RTC_ACK4 register, K4 the calculation formula is as below: K4=B4/1000000*65536, B4 is the segament coefficient of the quadratic function of crystal curve. For example, the K4 value is25257.
0x0008083C		Checksum2	INV(SUM(0x80828, 0x80838))
0x00080840	ACTI	Crystal apex temperature 1	Load to RTC_ACTI register, such as 0x1800.
0x00080844		Checksum1	INV(SUM(0x80840, 0x80840))
0x00080848	ACTI	Crystal the highest temperature 2	Load to RTC_ACTI register, such as 0x1800.
0x0008084C		Checksum2	INV(SUM(0x80848, 0x80848))
0x00080850	KTEMPx(x=4~1)	Crystal K coefficient temperature segment 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC.
0x00080854	—	Checksum1	INV(SUM(0x80850, 0x80850))
0x00080858	KTEMPx(x=4~1)	Crystal K coefficient temperature segment 2	Load to RTC_ACKTEMP register such as 0x3C2800EC.
0x0008085C		Checksum2	INV(SUM(0x80858, 0x80858))
…	-	-	Reserved
0x00080D10	P1/P0	RTC_ACP1/0 set 1	The upper 16 bits are loaded to the RTC_ACP1 register, such as 1060; the lower 16 bits are loaded to the RTC_ACP0 register, such as -214.
0x00080D14	P2’	RTC_ACP2 set 1	The stored value of this address is recorded as P2', for example: -19746971. According to the formula: P2=P2’+(Tr-Tm)*256, load P2 to the RTC_ACP2 register.

0x00080D18	P5	RTC_ACP5 set 1	The upper 16 bits are loaded to the RTC_ACP5 register, for example: 6444; the lower 16 bits are discarded.
0x00080D1C	P7/P6’	RTC_ACP7/6 set 1	The upper 16 bits are loaded to the RTC_ACP7 register, for example: 0; the lower 16 bits are loaded to P6'. For example: 1342. According to the formula P6=a*P6', load P6 to the RTC_ACP6 register.
0x00080D20		Checksum1	INV(SUM(0x80D10, 0x80D1C))
0x00080D24	P1/P0	RTC_ACP1/0 set 2	Same as backup 1
0x00080D28	P2’	RTC_ACP2 set 2	
0x00080D2C	P5	RTC_ACP5 set 2	
0x00080D30	P7/P6’	RTC_ACP7/6 set 2	
0x00080D34		Checksum2	
0x00080D38		AVCC gain 1	Pre-trim result/3.3 * 10000
0x00080D3C		DVCC gain 1	Pre-trim result/1.5 * 10000
0x00080D40		BGP gain 1	Pre-trim result/1.2 * 10000
0x00080D44		RCL gain 1	Pre-trim result/32768 * 10000
0x00080D48		RCH gain 1	Pre-trim result/6553600 * 10000
0x00080D4C		Checksum1	INV(SUM(0x80D38, 0x80D48))
0x00080D50		AVCC gain 2	Same as backup 1
0x00080D54		DVCC gain 2	
0x00080D58		BGP gain 2	
0x00080D5C		RCL gain 2	
0x00080D60		RCH gain 2	
0x00080D64		Checksum2	
0x00080D68		ID word 0, Backup 1	
0x00080D6C		ID word 1, Backup 1	
0x00080D70		Checksum1	INV(SUM(0x80D68, 0x80D6C))
0x00080D74		ID word 0, Backup 2	Same as backup 1

0x00080D78		ID word 1, Backup 2	
0x00080D7C		Checksum2	
0x00080D80		Actual temperature Tr 1 (from tmp275)	According to formula: P2=P2'+(Tr-Tm)*256, download P2 to RTC_ACP2 register.
0x00080D84		Tempertature testing Tm 1(from ADC)	According to formula: P2= P2'+(Tr-Tm)*256, download P2 to RTC_ACP2 register.
0x00080D88		Checksum1	INV(SUM(0x80D80, 0x80D84))
0x00080D8C		Actual temperature Tr 2 (from tmp275)	Same as backup 1
0x00080D90		Temperature testing Tm2 (ADC)	
0x00080D94		Checksum2	
…			Reserved.

13.8 Calibration

13.8.1 Temperature Calibration

According to the following temperature formula, *T* is the acutal temperature* 256.

$$T = ((P0 * ((X * X) >> 16)) + P1 * X + P2) >> 8 \qquad \textbf{Equation 13-1}$$

Among, *X* is the temperature sampling value of ADC which is a 16's complement.

P0~P2 is register stored value of RTC_ACP0~RTC_ACP2, and it is used to temperature calibration.

The actual temperature result: $T' = T / 256$

13.8.2 Frequency Error Calibration

（1）The calculation formula of chip frequency error is as below:

$$Delta = (P3 * ((T - Ti)^2 >> 16)) >> 16 + P4 \qquad \textbf{Equation 13-2}$$

Among them, Delta is a deviation rate of the 32K crystal rate (unit: 0.1ppm).

T is the temperature calculation value, which is calculatedaccording to **Equation 13-1**.

Ti is a value of the crytstal central temperature during RTC calibration, which is a value stored in RTC_ACTI register.

P4 is a deviation value of the crystal at room temperature.

P3 is a K coefficient of the temperature range where the current temperature T is. When RTC manual temperature compensation, user should according to *T* to manually match ACKx (x=0~4), and calibrate frequency in accordance with ACKx. There is no needs to store the value in RTC_ACP3 register.

（2）The calculation formula of frequency calibration is as below:

$$RTC\_CAL = (Delta * P5) >> 16 + 1$$ **Equation 13-3**

$$P5 = 65536/10/Px$$

Among, *Px* is the PPM resolution of the register RTC_CAL. Px = $\frac{1}{30} * \frac{CLK}{32768}$. CLK is RTCCLK division, there are separated to 1 division and 4 divisions.

（3）The calculation formula of PLL division in second pulse output is as below:

$$RTC\_DIV = \frac{CLK}{2} - (Delta * P6) >> 12 - 1$$ **Equation 13-4**

$$P6 = CLK * 2.048 * 10^{-4}$$ **Equation 13-5**

CLK is a division value before RTCPLLDIV is divided from PCLK or PLLL,which is configured by RTCPLLCLKSEL.

13.8.3 RTC Manually Compensation

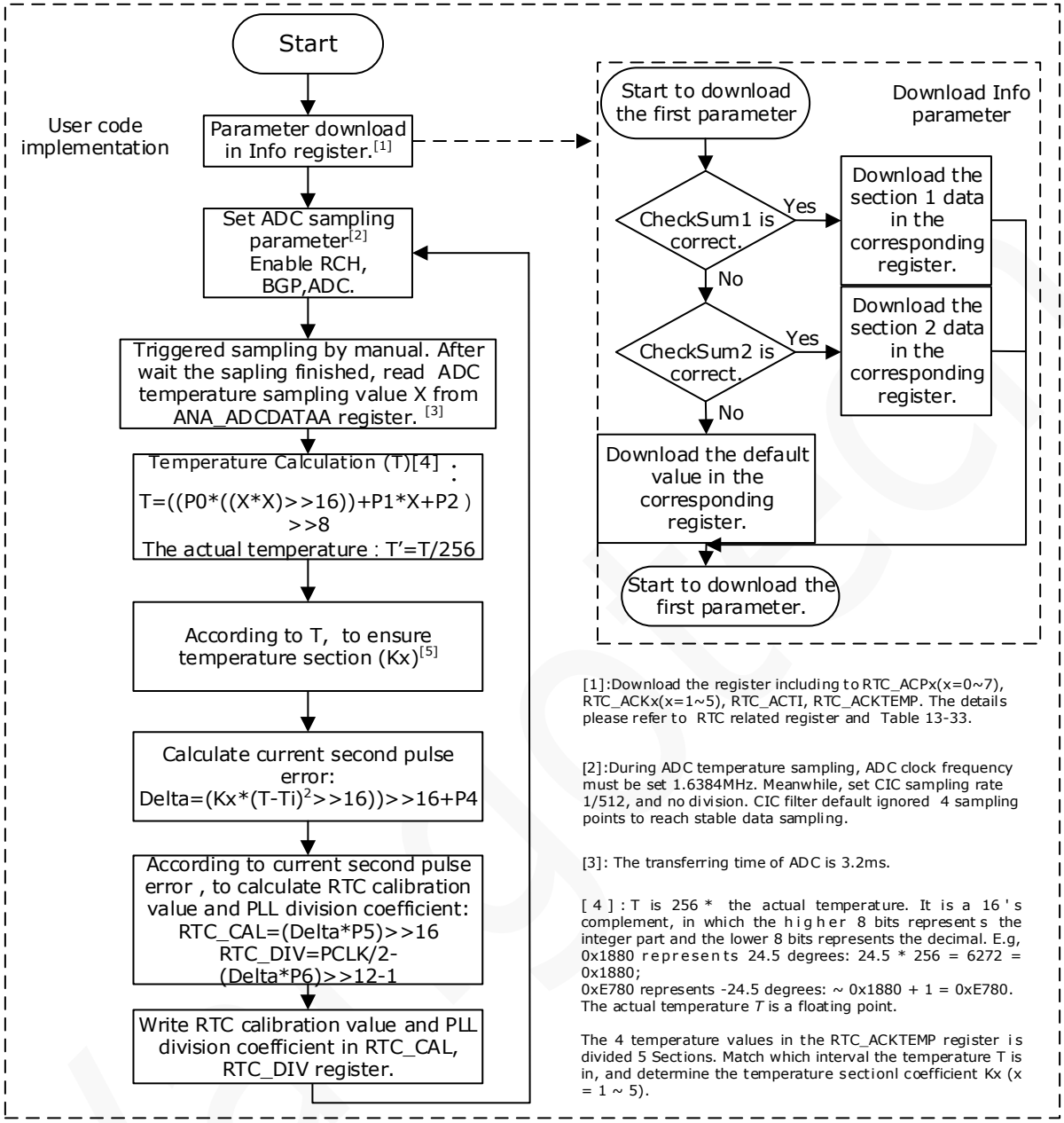


Figure 13-2 RTC Manually Temperature Compensation

14. FLASH Controller

14.1 Introduction

The FLASH controller is used to control the read/write program of embedded flash. It supports byte/half-word/word program and sector/chip erase. Programmable timing can be controlled by CYCLE_1US in MISC2 controller. The setting in FLASH controller will be reset after wake-up from sleep or deep-sleep mode, user should restore the setting manually after wake-up from these two states.

14.2 Features

--Support byte/half-word/ word programming.

--Support sector/chip erase.

--Support standby mode. When MCU does not accesss flash, flash automatically enters standby mode. Any access for Flash will wake it up from standby mode, and the wake-up time is 0.

--Support deep-standby mode. When MCU enters in sleep or deep-sleep mode, Flash automatically enters in deep-standby mode. Meanwhile, it supports FLASH_DSTB register of configured by manual to enter deep-standby mode. Any access for Flash will wake it up from standby mode, and the wake-up time is 10 x 1μstick.

--When program operates in FLASH and FLASH is not ready, MCU will automatic suspend. When FLASH is ready, MCU will automatic operate from idle status.

--Support read operation in Info sections.

--Support register read/write operation which set in FLASH.

--Programmable speed.

--Support automatic checking and comparison in hardware, and support checksum error interrupt.

--Support read, write, ICE protection.

14.3 Functional Block Diagram

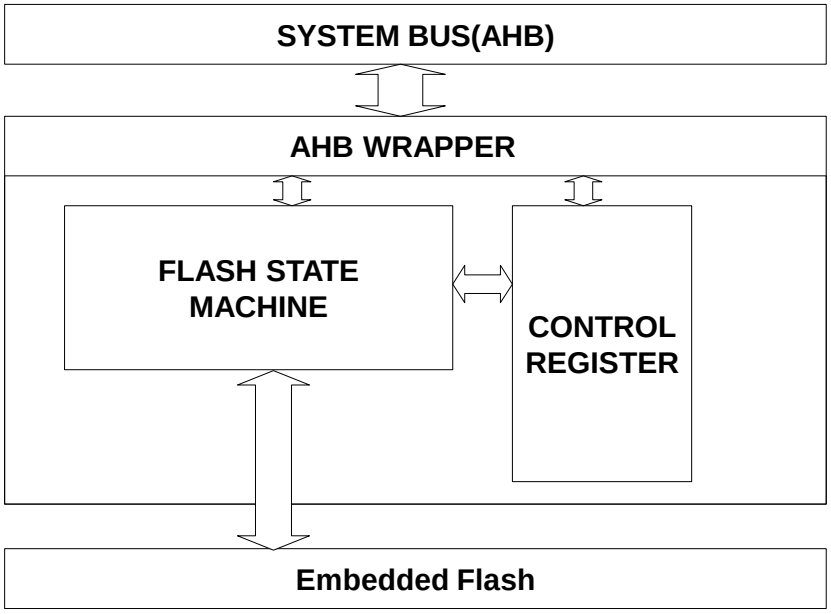


Figure 14-1 Flash Functional Block Diagram

14.4 Register Address

Table 14-1 FLASH Register Address (FLASH Register Base Address:0x00000000)

Name	Type	Address	Contents	Default
FLASH_ICEPROT	R/W	0xFFFA8	ICE protect register	--
FLASH_RDPROT	R	0xFFFAC	Flash read protective status register	0x00000000
FLASH_WRPROT	R/W	0xFFFB0	Flash write protective control register	0x00000000
FLASH_STS	R	0xFFFBC	FLASH program status register	0x00
FLASH_INTSTS	R/C	0xFFFCC	FLASH checksum interruptvie register	0x0
FLASH_CSSADDR	R/W	0xFFFD0	FLASH checksum start address	0x00000
FLASH_CSEADDR	R/W	0xFFFD4	FLASH checksum end address	0xFFFF
FLASH_CSVALUE	R	0xFFFD8	FLASH checksum calculation register	--
FLASH_CSCVALUE	R/W	0xFFFDC	FLASH checksum expected value register	0x00000000
FLASH_PASS	R/W	0xFFFE0	FLASH password register	0x00
FLASH_CTRL	R/W	0xFFFE4	FLASH control register	0x00
FLASH_PGADDR	R/W	0xFFFE8	FLASH program address register	0x00000
FLASH_PGDATA	R/W	0xFFFEC	FLASH program word-data register	--
FLASH_PGB0	R/W	0xFFFEC	FLASH program byte-data register 0	--

FLASH_PGB1	R/W	0xFFFED	FLASH program byte-data register 1	--
FLASH_PGB2	R/W	0xFFFEE	FLASH program byte-data register 2	--
FLASH_PGB3	R/W	0xFFFEF	FLASH program byte-data register 3	--
FLASH_PGHW0	R/W	0xFFFEC	FLASH program nibble data register 0	--
FLASH_PGHW1	R/W	0xFFFEE	FLASH program nibble data register 1	--
FLASH_SERASE	R/W	0xFFFF4	FLASH sector earse control register	0x00
FLASH_CERASE	R/W	0xFFFF8	FLASH chip erase control register	0x00
FLASH_DSTB	R/W	0xFFFFC	FLASH deep-standby control register	0x00

Table 14-2 MISC2 Address (MISC2 Base Address :0x40013E00)

Name	Type	Address	Contents	Default
MISC2_FLASHWC	R/W	0x0000	FLASH wait cycle register	0x2100

14.5 Register Address

14.5.1 FLASH_PASS Register

Table 14-3 FLASH_PASS Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0
0	UNLOCK	R	UNLOCK is used to indicate whether FLASH has been unlocked or not. To set this bit, user should write 0x55AAAA55 in the register. The bit will keep high until user write others value in the register. If the UNLOCK bit is 0, all program, erase or set operation in FLASH will be disabled.	0x0

14.5.2 FLASH_CTRL Register

Table 14-4 FLASH_CTRL Register

Bit	Name	Type	Contents	Default
31:3	-	-	Reserved.	0
2	CSINTEN	R/W	The register is used to control the interrupt enable of checksum error. 0:Disble checksum error interrupt. 1:Enable checksum error interrupt.	0x0

1:0	CSMODE	R/W	The register is used to control the checksum calculation and comparison. 0:Disable checksum mode. 1:Checksum calculation and comparison will always operate. 2:Operate one time checksum and comparison when each Timer 2 overflows. 3:Operate one time checksum and comparison when each rising edge of RTC second pulse.	0x0

14.5.3 FLASH_PGADDR Register

Table 14-5 FLASH_PGADDR Register

Bit	Name	Type	Contents	Default
31:18	-	-	Reserved.	0
17:0	PGADDR	R/W	Flash programming address. This is FLASH IP address. The detail message for each mode address, please refer to **Table 14-6**. When programming completed, the address will be increased automatically.	0x000000

Table 14-6 PGADDR and Write Data Register

Mode	PGADDR[17:2]	PGADDR[1:0]	Writing data register
"Word" Program Mode	0x0000~0xFFFF	0	FLASH_PGDATA
"Byte" Program Mode	0x0000~0xFFFF	0	FLASH_PGB0
		1	FLASH_PGB1
		2	FLASH_PGB2
		3	FLASH_PGB3
"Nibble" Program Mode	0x0000~0xFFFF	0	FLASH_PGHW0
		2	FLASH_PGHW1
Page Erase	0x0000~0xFFFF	0	FLASH_SERASE

14.5.4 FLASH_PGDATA Register

Table 14-7 FLASH_PGDATA Register

Bit	Name	Type	Contents	Default

31:0	PGDATA	R/W	The register is used to control "word" programming data. When UNLOCK is 1, writing to this register will automatically trigger a (4-byte) programming. In this time, DO NOT access the FLASH IP until the programming is completed. There are 32-byte FIFO inside FLASH. So user can perform the continuous programming without interrupt. However, if user needs to access the FLASH IP such as executing a program, the FLASH programming speed will slow down during this time because the FLASH IP needs more time to enable. It is recommended to put the programming in SRAM so that the maximum programming speed can be achieved.	

14.5.5 FLASH_PGBx Register

Table 14-8 FLASH_PGBx Register

Bit	Name	Type	Contents	Default
7:0	PGBx	R/W	The register is used to control "byte" programming data. When UNLOCK is 1, writing to this register and it will automatically trigger a byte programming. In this time, DO NOT access the FLASH IP until the programing is completed. There are 8-byte FIFO inside FLASH. So user can perform the continuous programming without interrupt. However, if user needs to access the FLASH IP such as executing a program, the FLASH programming speed will slow down during this time because the FLASH IP needs more time to enable. It is recommended to put the programming in SRAM so that the maximum programming speed can be achieved.	

14.5.6 FLASH_PGHWx Register

Table 14-9 FLASH_PGHWx Register

Bit	Name	Type	Contents	Default
15:0	PGHWx	R/W	The register is used to control "nibble" programming data. When UNLOCK is 1, writing to this register and it will automatically trigger a (2-byte) programming. In this time, DO NOT access the FLASH IP until the	

			programming is completed. There are 16-byte FIFO inside FLASH. So user can perform the continuous programming wihtout interrupt . However, if user needs to access the FLASH IP such as executing a program, the FLASH program speed will slow down during this time because the FLASH IP needs more time to enable. It is recommend to put the programming in SRAM so that the maximum programming speed can be achieved.	

14.5.7 FLASH_SERASE Register

Table 14-10 FLASH_SERASE Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0
0	SERASE	R	The bit is used to indicate whether the sector is earsing now. The sector size is 1024 bytes. When UNLOCK is 1 and user writes 0xAA5555AA in the register, the bit will be set 1. And it will be automatically clear 0 after the sector erasing is completed. The sector erasing address is controlled by PGADDR[17:2]. The sector erasing time is 4000*1μs.	0x0

14.5.8 FLASH_CERASE Register

Table 14-11 FLASH_CERASE Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0
0	CERASE	R	The bit is used to indicate whether the chip full-erase is doing now. When UNLOCK is 1 and user writes 0xAA5555AA in the register, the bit will be set 1. And it will be automatically clear 0 after the sector erase is completed. The chip erasing time is 30000*1μs.	0x0

14.5.9 FLASH_DSTB Register

Table 14-12 FLASH_DSTB Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0

0	DSTB	R	The bit is used to indicate whether the FLASH IP is accessing deep-standby mode. When UNLOCK is 1 and user writes 0xAA5555AA in the register, the bit will be set 1. FLASH IP access to the deep-standby mode. When FLASH IP wakes up from the deep-standby mode, the bit is automatically cleared 0. The deep-standby mode can beexited by any FLASH IP access. But, it takes 10 ticks x 1μs to restore the FLASH IP to the normal status. In this time, any access tp FLASH will be filterd until FLASH is ready. In sleep and deep-sleep mode, FLASH automatically accesses the deep-standby mode. In IDLE mode, user needs to run code in SRAM and manually configure this register.	0x0

14.5.10 FLASH_INTSTS Register

Table 14-13 FLASH_INTSTS Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved.	0
0	CSERR	R/C	Checksum error status bit. The flag bit is used to indicate the previous checksum error. That is, it is different from CSVALUE/CSCVALUE. When CSINTEN is 1, an interrupt will be generated to the CPU. Write 1 to clear the bit.	0x0

14.5.11 FLASH_CSSADDR Register

Table 14-14 FLASH_CSSADDR Register

Bit	Name	Type	Contents	Default
31:19	-	-	Reserved.	0
18:0	CSSADDR	R/W	Checksum start address register. The register is used to control the starting address of the checksum. The value is the byte address of the register, but the lowest 2 bits are always 0.	0x00000

14.5.12 FLASH_CSEADDR Register

Table 14-15 FLASH_CSEADDR Register

Bit	Name	Type	Contents	Default
31:19	-	-	Reserved.	0
18:0	CSEADDR	R/W	Checksum end address register. This register is used to control the end address of the checksum. This value is the byte address of the checksum end address, but the lowest 2 bits are always 0. The checksum range is (CSSADDR=<ADDR=<CSEADDR). Checksum end address register. The register is used to control the end address of the checksum. The value is the byte address of the checksum end address, but the lowest 2 bits are always 0. The checksum range is (CSSADDR=<ADDR=<CSEADDR).	0x7FFFC

14.5.13 FLASH_CSVALUE Register

Table 14-16 FLASH_CSVALUE Register

Bit	Name	Type	Contents	Default
31:0	CSVALUE	R	Checksum calculation value register. The register is used to indicate the checksum result automatically calculated by the current MCU.	0x00000000

14.5.14 FLASH_CSCVALUE Register

Table 14-17 FLASH_CSCVALUE Register

Bit	Name	Type	Contents	Default
31:0	CSCVALUE	R/W	Checksum expected value register. The register is used to set the expected checksum result. When checksum is completed but it is mismatched between MCU checksum value CSVALUE and user's setting value CSCVALUE, the CSERR flag bit will be set 1. The calculation methods with checksum and the expected value: accumulate all the values (CSSADDR=<ADDR=<CSEADDR) (32-bit data byte) in the range, and keep the lower 32-bit of the accumulation data result.	0x00000000

14.5.15 FLASH_STS Register

Table 14-18 FLASH_STS Register

Bit	Name	Type	Contenst	Default
31:5	-	-	Reserved.	0
4:0	STS	R	FLASH control status register. 1:FLASH operation done. Others:FLASH is busy or idel status. User can check the register to ensure before disable FLASH_PASS register, all FLASH operation is completed.	0x0

14.5.16 MISC2_FLASHWC Register

Table 14-19 MISC2_FLASHWC Register

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved.	0
13:8	CYCLE_1US	R/W	This register is used to calculate the 1μs tick with AHBClock by the FLASH. The setting is related to the wake-up time, and the erase and programming time of FLASH. FLASH wake-time = 1μs tick time* 10, and it must fulfill 1μstick>=1μs. 1μstick=(AHB clock cycle)*(CYCLE_1US+1). For example, the AHB clock frequency is 26.2144M. In order to ensure 1μs tick time and the minimum wake-up time, CYCLE_1US should be set 26. At this time, the wake-up time of FLASH is 27 / 26214400 * 10, which is around 10μs. For example, the AHB clock frequency is 32.768k. In order to ensure 1μs tick time and the minimum wake-up time, CYCLE_1US should be set 0. Meanwhile, the wake-up time of FLASH is 1/32768 * 10, which is around 305μs.	0x21
7:0	-	-	Reserved.	0

14.5.17 FLASH_RDPROT Register

Table 14-20 FLASH_RDPROT Register

Bit	Name	Type	Contents	Default
31:0	RDPORT	R	The register is used to indicate the specified area in ICE mode (MODE=0) whether is protected by reading. For each bit in the register, it indicates the protective status of 16Kbyte area in FLASH. Bit 0 is the first 16Kbyte area (0~0x3FFF), and bit 31 is the last 16Kbyte area (0x7C000~0x7FFFF). When the corresponding bit of the RDPORT register is set to 1, the read operation of this area will be ignored in ICE mode. 0:Without reading protection 1: Reading protection, DO NOT use reading operation. After power on or each reset, the FLASH will read the value of 0x7FC00 and reverse it to store in the register. After the address 0x7FC00 of FLASH is read, the register will also be updated. For example, when the data in 0x7FC00 is 0xFFFFFFFF, the register value is 0x00000000 which represents that there is no reading protective function. If any bit of RDPORT is set 1, then DO NOT execute the erasing operation for the corresponding sectior. Only full erase of chip can clear the reading protection. . When the reading operation of the command area is protected, it means that ICE debug is not allowed. For all protective areas in ICE mode, the reading value will become 0.	0x00000000

14.5.18 FLASH_WRPROT Register

Table 14-21 FLASH_WRPROT Register

Bit	Name	Type	Contents	Default
31:0	WRPORT	R/W	The register is used to control the specified FLASH sections which are influenced by erase or write operation. For the register each bit, it will protect 16Kbyte sections in FLASH. Bit 0 is the first 16Kbyte section (0x7C000~0x7FFFF), and bit 31 is the lastest 16Kbyte section (0x7C000~0x7FFFF). When the corresponding bit set 1, it will ignore the erase or program operation in this section.	0x00000000

			0:without erase/ writing protection. 1:erase/ writing protection. Erase or program operation is invalid.	

14.5.19 FLASH_ICEPROT Register

Table 14-22 FLASH_ICEPROT Register

Bit	Name	Type	Contents	Default
31:0	ICEPORT	R/W	The register is used to indicate whether set anti ICE mode. After powered on or reset, FLASH will read data from 0x7FC08 address. If the lower 4-bit is 0xA, ICE debug mode is invalid.	0x00000000

14.6 FLASH Protection

Table 14-23 FLASH Protection

Mode	Functions	Enable Methods and Description	Disable Methods
Read Protected	Under ICE mode, to prevent the specified code from being read.	Write 0 in FLASH 0x7FC00 address, then read it again. The read protected is effective. 32 bits, each bit protects FLASH in 16Kbyte section. Bit0 protects 0~0x3FFF. Bit31 protects 0x7C000~0x7FFFF. When MODE is 0, the protected section is 0. When MODE is 1, the read protected is invalid.	Only chip erase can cancel the read protected mode.
Write Protected	To prevent the specified code from being modified.	Write 1 in FLASH_WRPROT register to set the write protected. 32 bits, each bit protects FLASH in 16Kbyte section. Bit0 protects 0~0x3FFF. Bit31 protects 0x7C000~0x7FFFF. After set the write protected, it cannot program and erase the protective sections.	Write 0 in FLASH_WRPROT register to remove the write protected. After chip reset, FLASH_WRPROT register will be reset to 0, and remove the write protected.

ICE Protection	Prevent chips into ICE mode.	Write 0xA in FLASH 0x7FC08 address lower 4 bits. After chips reset, entering ICE protected mode which cannot debug.	The erase operation for the last sector in order to cancel ICE protection.

15. GPIO Controller

15.1 Introduction

There are 86 IOs at most in V85XXP. Among, 16 IOs (GPIOA) are controlled by PMU which can wake-up from sleep or deep-sleep mode. Others (GPIOB~GPIOF) are controlled by GPIO which cannot wake-up from sleep or deep-sleep mode. The register is kept under the sleep mode but not deep-sleep mode. After woke-up from deep-sleep mode, user should reset it by manual.

15.2 Features

--Each IO can be input or output mode.

--Each IO can be open-drain mode.

--All IOs no pull-high or pull-low resistance.

--GPIOA can wake-up from sleep or deep-sleep mode.

15.3 Functional Block Diagram

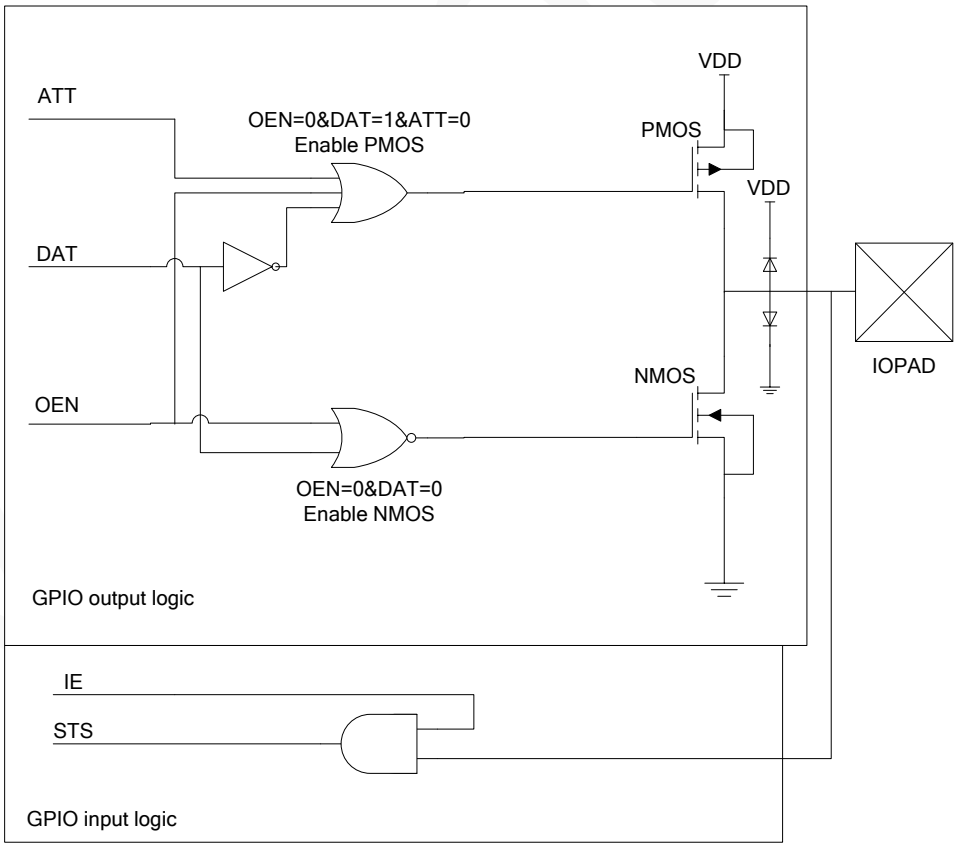


Figure 15-1 GPIO Functional Block Diagram

15.4 Register Address

Table 15-1 PMU_IOA (PMU Base Address:0x40014000)

Name	Type	Address	Contents	Default
PMU_IOAOEN	R/W	0x0010	IOA ouput enable register	0xFFFF
PMU_IOAIE	R/W	0x0014	IOA input enable register	0xFFFF
PMU_IOADAT	R/W	0x0018	IOA data register	0x0000
PMU_IOAATT	R/W	0x001C	IOA attribute register	0x0000
PMU_IOAWKUEN	R/W	0x0020	IOA wake-up enable register	0x00000000
PMU_IOASTS	R	0x0024	IOA input status register	--
PMU_IOAINTSTS	R/C	0x0028	IOA interrupt status register	0x0000
PMU_IOASEL	R/W	0x0038	IOA special function select register	0x0000
PMU_IOANODEG	R/W	0x0050	IOA no-deglitch circuit control	0x0000

Table 15-2 GPIO (GPIO Base Address:0x40000000)

Name	Type	Address	Contents	Default
IOB_OEN	R/W	0x0020	IOB output enable register	0xFFFF
IOB_IE	R/W	0x0024	IOB input enable register	0xFFFF
IOB_DAT	R/W	0x0028	IOB output data register	0x0000
IOB_ATT	R/W	0x002C	IOB attribute register	0x0000
IOB_STS	R	0x0030	IOB input status register	--
IOC_OEN	R/W	0x0040	IOC output enable register	0xFFFF
IOC_IE	R/W	0x0044	IOC input enable register	0xFFFF
IOC_DAT	R/W	0x0048	IOC output data register	0x0000
IOC_ATT	R/W	0x004C	IOC attribute register	0x0000
IOC_STS	R	0x0050	IOC input status register	--
IOD_OEN	R/W	0x0060	IOD output enable register	0xFFFF
IOD_IE	R/W	0x0064	IOD input enable register	0xFFFF
IOD_DAT	R/W	0x0068	IOD output data register	0x0000
IOD_ATT	R/W	0x006C	IOD attribute register	0x0000
IOD_STS	R	0x0070	IOD input status register	--
IOE_OEN	R/W	0x0080	IOE output enable register	0xFFFF

IOE_IE	R/W	0x0084	IOE input enable register	0xFFFF
IOE_DAT	R/W	0x0088	IOE output data register	0x0000
IOE_ATT	R/W	0x008C	IOE attribute register	0x0000
IOE_STS	R	0x0090	IOE input status register	--
IOF_OEN	R/W	0x00A0	IOF output enable register	0x7FFF
IOF_IE	R/W	0x00A4	IOF input enable register	0x7FFF
IOF_DAT	R/W	0x00A8	IOF output data register	0x0000
IOF_ATT	R/W	0x00AC	IOF attribute register	0x0000
IOF_STS	R	0x00B0	IOF input status register	--
IOB_SEL	R/W	0x00C0	IOB special function select register	0x00
IOE_SEL	R/W	0x00CC	IOE special function select register	0x00
IO_MISC	R/W	0x00E0	IO misc control register	0x00

15.5 Register Definition

15.5.1 PMU_IOAOEN Register

Table 15-3 PMU_IOAOEN Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOAOEN	R/W	Each bit controls IOA ouput signal. The details please refer to **Table 15-7**. 0:Enable IO output. 1:Disable IO output.	0xFFFF

15.5.2 PMU_IOAIE Register

Table 15-4 PMU_IOAIE Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOAIE	R/W	Each bit controls IOA input signal. The details please refer to **Table 15-7**. 0:Disable IOA input. 1:Enable IOA input.	0xFFFF

15.5.3 PMU_IOADAT Register

Table 15-5 PMU_IOADAT Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOADAT	R/W	Each bit controls the output data and pull-high/ pull-low of IOA. The details please refer to **Table 15-7**.	0x0000

15.5.4 PMU_IOAATT Register

Table 15-6 PMU_IOAATT Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOAATT	R/W	Each bit controls IOA attribute. The following table is the detail information of IO status in different settings. When a IO is set as output mode (GPIO or the special function), the bit is used to control IO to CMOS or open-drain mode. 0:CMOS mode. 1:open-drain mode (DO NOT PMOS output.)	0x0000

Table 15-7 IO Status in Different Settings

IOx Settings			IO Status
IOxOEN	IOxDAT	IOxATT	
1	0	0	Output prohibited
1	1	0	Output prohibited
1	0	1	Output prohibited
1	1	1	Output prohibited
0	0	0	'0' on the output register activates N-MOS, while '1' on the output register activates P-MOS.
0	1	0	
0	0	1	'0' on the output register activates N-MOS, while '1' on the output register places the port in the high resistance state (P-MOS is never activated).
0	1	1	

15.5.5 PMU_IOAWKUEN Register

Table 15-8 PMU_IOAWKUEN Register

Bit	Name	Type	Contents	Default
31:0	IOAWKUEN	R/W	Each 2 bits control interrupt and wake-up of IOA. Bit [1:0]:IOA0WKUEN[1:0] Bit [3:2]:IOA1WKUEN[1:0] ..... Bit [31:30]:IOA15WKUEN[1:0] The details about each wake-up mode, please refer to **Table** 15-9.	0x00000000

Table 15-9 IO Wake-up Mode

IOAyWKUEN[1:0]	IOAyDAT	Wake-up Events
0	X	Wake-up function prohibited
1	0	Rising-edge wake-up
	1	Falling-edge wake-up
2	0	High-level wake-up
	1	Low-level wake-up
3	X	Both-edge wake-up

Among, y=0…15 represents IOA0~15.

The hardware locks the state of the IOA at the last moment before entering the light sleep or deep sleep mode. When selecting the rising edge to wake-up, user must ensure that the IOA is low before entering to sleep mode, and ensure that the rising edge of the IOA is correctly detected; otherwise, IOA cannot wake-up normally. When the falling edge of wake-up mode is selected, user should ensure that the IOA state is high before entering the sleep mode, and ensure that the falling edge of the IOA is correctly detected; otherwise, IOA cannot wake-up normally.

There is no deburring circuit for level interrupts, including the normal interrupts and IOA level wakes up for sleep and deep sleep mode. The deburring circuit is only valid for the IOA edge wake-up signal in the sleep and deep-sleep mode, and the deburring time is about 4 RTCCLK clock cycles.

15.5.6 PMU_IOASTS Register

Table 15-10 PMU_IOASTS Register

Bit	Name	Type	Contents	Default

31:16	-	-	Reserved.	0
15:0	IOASTS	R	Each bit represents currently input data of IOA.	--

15.5.7 PMU_IOAINTSTS Register

Table 15-11 PMU_IOAINTSTS Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	INTSTS	R/C	Each bit of IO interrupt status register represents the interrupt status of IOA. When it check IOA wake-up events, the corresponding interrupt will set 1. Write 1 to clear 0 to the corresponding flag bit.	0x0000

15.5.8 PMU_IOASEL Register

Table 15-12 PMU_IOASEL Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved.	0
7	IOA_SEL7	R/W	IOA7 register for special function select. 0:GPIO 1:special function 1 (RTC_PLLDIV)	0x0
6	IOA_SEL6	R/W	IOA6 register for special function select. 0:GPIO 1:special function 1 (CMP2_O)	0x0
5:4	-	-	Reserved.	0
3	IOA_SEL3	R/W	IOA3 register for special function select. 0:GPIO 1:special function 1 (RTC_PLLDIV)	0x0
2:0	-	-	Reserved.	0

15.5.9 PMU_IOANODEG Register

Table 15-13 PMU_IOANODEGL Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	-

15:0	IOANODEG	R/W	Each bit controls whether the IOA edge wakeup signal has a debounce circuit. When this bit is set to 1, the debounce circuit of the corresponding IOA pin will be invalid, and the wake-up speed will become faster. The debounce circuit affects the edge wake-up signal in sleep and deep sleep modes. 0: IOA wake-up signal with the debounce circuit 1: IOA wake-up signal without the debounce circuit	0x0000

15.5.10 IOX_OEN Register

Table 15-14 IOX_OEN Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOXOEN	R/W	Each bit controls the output enable signal of IOX. About the details of IO bit, please refer to **Table 15-7**. 0: enable IO output 1: diable IO outuput	0xFFFF

15.5.11 IOX_IE Register

Table 15-15 IOX_IE Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOXIE	R/W	Each bit controls the input enable signal of IOX. About the details of IO status, please refer to **Table 15-7**. 0: disable IO input 1: enable IO input	0xFFFF

15.5.12 IOX_DAT Register

Table 15-16 IOX_DAT Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOXDAT	R/W	Each bit controls output data and pull-high/pull-down function. The details of IO bit, please refer to **Table 15-7**.	0x0000

15.5.13 IOX_ATT Register

Table 15-17 IOX_ATT Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOXATT	R/W	Each bit in the register is used to control the corresponding IO attribute. 0:CMOS output 1:open-drain output When an IO is configured as the special function, such as UART or SPI, user can configure the corresponding IOXATT to 1, and let it become open-drain mode via the external output high.	0x0000

15.5.14 IOX_STS Register

Table 15-18 IOX_STS Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:0	IOXSTS	R	Each bit shows the current IOX input data. It MUST enable input, then can read the external level status.	--

15.5.15 IOB_SEL Register

Table 15-19 IOB_SEL Register

Bit	Name	Type	Contents	Default
31:7	-	-	Reserved.	0
6	IOB_SEL6	R/W	IOB6 special function select register 0: GPIO or special function 1/2. 1: Special function 3 (RTCCLK output) when special function 1/2 is not enabled.	0x0
5:3	-	-	Reserved.	0
2	IOB_SEL2	R/W	IOB2 special function select register 0: GPIO or special function 1/2.	0x0

			1: Special function 3 (PLLL output) when special function 1/2 is not enabled.	
1	IOB_SEL1	R/W	IOB1 special function select register 0: GPIO or special function 1/2. 1: Special function 3 (PLLH divider output) when special function 1/2 is not enabled.	0x0
0	-	-	Reserved.	0

15.5.16 IOE_SEL Register

Table 15-20 IOE_SEL Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved.	0
7	IOE_SEL7	R/W	IOE7 special function select register 0: GPIO or high resistance 1: Special function 1 (CMP1_O)	0x0
6:0	-	-	Reserved.	0

15.5.17 IO_MISC Register

Table 15-21 IO_MISC Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved.	0
5	I2CIOC	R/W	The register is used to control IOB and IOC for I^2C function. 0:I^2C function with IOB13~IOB14 1:I^2C function with IOC4~IOC5	0x0
4:3	-	-	Reserved.	0
2:0	PLLHDIV	R/W	When IOB1 is selected as the special function 3, the register is used to control PLLH output division ratio. 0:/1 1:/2 2:/4 3:/8	0x0

			4:/16 Other: reserved	

15.6 Special Function IO

15.6.1 Special Function IOA

The following table shows when the spcial function IOA is enabled, the corresponding module functions.

Table 15-22 Special Function IOA

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOA0	SWDCLK (MODE = 0)	-	LCDSEG54	-
IOA1	SWDIO (MODE = 0)	-	LCDSEG53	-
IOA2	-	-	LCDSEG52	-
IOA3	RTC_PLLDIV	-	LCDSEG51	-
IOA4	-	-	LCDSEG66	CMP2_P
IOA5	-	-	LCDSEG67	CMP2_N
IOA6	CMP2_O	-	LCDSEG68	-
IOA7	RTC_PLLDIV	-	LCDSEG69	-
IOA8	-	-	LCDSEG50	ADC_CH3
IOA9	-	-	LCDSEG49	ADC_CH4
IOA10	-	-	LCDSEG48	ADC_CH5
IOA11	-	-	LCDSEG47	ADC_CH6
IOA12	UART0_RX	-	LCDSEG71	-
IOA13	UART1_RX	ISO7816_IO0	LCDSEG73	-
IOA14	UART2_RX	-	LCDSEG13	-
IOA15	UART3_RX	ISO7816_IO1	LCDSEG15	-

15.6.2 Special Function IOB

The following table shows the special function of IOB, the special function will be opened when the special function module is enabled. However, when the special function is LCD COM/SEG, ADC, CMP, X6_5M or

VDCIN, user should disable the corresponding GPIO input/output function by manual, and prohibited using other special functions in GPIO in order to ensure the correctness of these special functions.

Table 15-23 Special Function IOB

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOB0	UART4_RX	PWM0	-	LCDSEG43
IOB1	UART5_RX	-	PLLH divider	LCDSEG45
IOB2	UART0_TX	-	PLLL	LCDSEG70
IOB3	UART1_TX	ISO7816_CLK0	-	LCDSEG72
IOB4	UART2_TX	-	-	LCDSEG12
IOB5	UART3_TX	ISO7816_CLK1	-	LCDSEG14
IOB6	UART4_TX	PWM1	RTCCLK	LCDSEG44
IOB7	UART5_TX	-	-	LCDSEG46
IOB8	-	-	-	LCDSEG35
IOB9	SPI1CSN	-	-	LCDSEG36
IOB10	SPI1CLK	-	-	LCDSEG37
IOB11	SPI1MISO	-	-	LCDSEG38
IOB12	SPI1MOSI	-	-	LCDSEG39
IOB13	I2CSCL (I2CIOC=0)	PWM2	-	LCDSEG40
IOB14	I2CSDA (I2CIOC=0)	PWM3	-	LCDSEG41
IOB15	TIMER EXT CLK	-	-	LCDSEG42

15.6.3 Special Function IOC

The following table shows the special function of IOC, the special function will be opened when the special function module is enabled. However, when the special function is LCD COM/SEG, ADC, CMP, X6_5M or VDCIN, user should disable the corresponding GPIO input/output function by manual, and prohibited using other special functions in GPIO in order to ensure the correctness of these special functions.

Table 15-24 Special Function IOC

IO	Special Function 1	Special Function 2	Special Function 3
IOC0	SPI2CSN	-	LCDSEG16
IOC1	SPI2CLK	-	LCDSEG17
IOC2	SPI2MISO	-	LCDSEG18
IOC3	SPI2MOSI	-	LCDSEG19

IOC4	-	I2CSCL(I2CIOC=1)	LCDSEG20
IOC5	-	I2CSDA(I2CIOC=1)	LCDSEG21
IOC6	-	-	LCDSEG22
IOC7	-	-	LCDSEG23
IOC8	-	-	LCDSEG24
IOC9	-	-	LCDSEG25
IOC10	-	-	LCDSEG26
IOC11	-	-	LCDSEG27
IOC12	-	-	LCDSEG28
IOC13	-	-	LCDSEG29
IOC14	-	-	LCDSEG30
IOC15	-	-	LCDSEG31

15.6.4 Special Function IOD

The following table shows the special function of IOD, the special function will be opened when the special function module is enabled. However, when the special function is LCD COM/SEG, ADC, CMP, X6_5M or VDCIN, user should disable the corresponding GPIO input/output function by manual, and prohibited using other special functions in GPIO in order to ensure the correctness of these special functions.

Table 15-25 Special Function IOD

IO	Special Function 1	Special Function 2	Special Function 3
IOD0	LCDCOM0	-	-
IOD1	LCDCOM1	-	-
IOD2	LCDCOM2	-	-
IOD3	LCDCOM3	-	-
IOD4	LCDCOM4	LCDSEG0	SPI3CSN
IOD5	LCDCOM5	LCDSEG1	SPI3MISO
IOD6	LCDCOM6	LCDSEG2	SPI3MOSI
IOD7	LCDCOM7	LCDSEG3	SPI3CLK
IOD8	LCDSEG4	-	-
IOD9	LCDSEG5	-	-
IOD10	LCDSEG6	-	-
IOD11	LCDSEG7	-	-

IOD12	LCDSEG8	-	-
IOD13	LCDSEG9	-	-
IOD14	LCDSEG10	-	-
IOD15	LCDSEG11	-	-

15.6.5 Special Function IOE

The following table shows the special function of IOE, the special function will be opened when the special function module is enabled. However, when the special function is LCD COM/SEG, ADC, CMP, X6_5M or VDCIN, user should disable the corresponding GPIO input/output function by manual, and prohibited using other special functions in GPIO in order to ensure the correctness of these special functions.

Table 15-26 Special Function IOE

IO	Special Function 1	Special Function 2	Special Function 3
IOE0	-	LCDSEG74	-
IOE1	-	LCDSEG75	-
IOE2	-	LCDSEG76	-
IOE3	-	LCDSEG77	-
IOE4	-	LCDSEG63	ADC_CH7
IOE5	-	LCDSEG62	ADC_CH8
IOE6	-	LCDSEG61	ADC_CH9, Tiny ADC 0
IOE7	CMP1_O	LCDSEG60	ADC_CH11, Tiny ADC 1
IOE8	-	LCDSEG59	CMP1_P
IOE9	-	LCDSEG58	CMP1_N
IOE10	-	LCDSEG32	-
IOE11	-	LCDSEG33	-
IOE12	-	LCDSEG34	-
IOE13	-	LCDSEG55	-
IOE14	-	LCDSEG56	-
IOE15	-	LCDSEG57	-

15.6.6 Special Function IOF

The following table shows the special function of IOF, the special function will be opened when the special function module is enabled. However, when the special function is LCD COM/SEG, ADC, CMP, X6_5M or

VDCIN, user should disable the corresponding GPIO input/output function by manual, and prohibited using other special functions in GPIO in order to ensure the correctness of these special functions.

Table 15-27 Special Function IOF

IO	Special Function 1
IOF0	X6_5MI
IOF1	X6_5MO
IOF7	N/A
IOF8	N/A
IOF11	N/A
IOF12	N/A

16. DMA Controller

16.1 Introduction

The DMA module provides high-speed data transmission from memory to memory, memory to peripherals, and peripherals to memory. DMA controller intergrated AHB to APB bridge, so when DMA performs low-speed peripheral data transmission, advanced high performance bus (AHB) will not be affected by low-speed peripherals. In V85XXP, it intergrated 4 DMA channels, and the priority of 4 channels is cyclic. When system is woke-up from sleep or deep-sleep mode, DMA controller will be reseted. Therefore, after waking-up from these 2 modes, we should reset the related settings by manual.

16.2 Features

--Support transmission between memories;

--Support transmission from memories to peripherals;

--Support transmission from peripherals to memories;

--Software mode or hardware DMA request mode;

--Support fixed address, address cycle after single packet transmission or all packets transmission;

--Support IRQ generation when single packet transmitted/ all packets transmitted/ data transmission stop;

--Support bus data abort detected;

--Intergrate with AHB to APB bridge;

--Support HW AES-128/192/256.

16.3 Functional Block Diagram

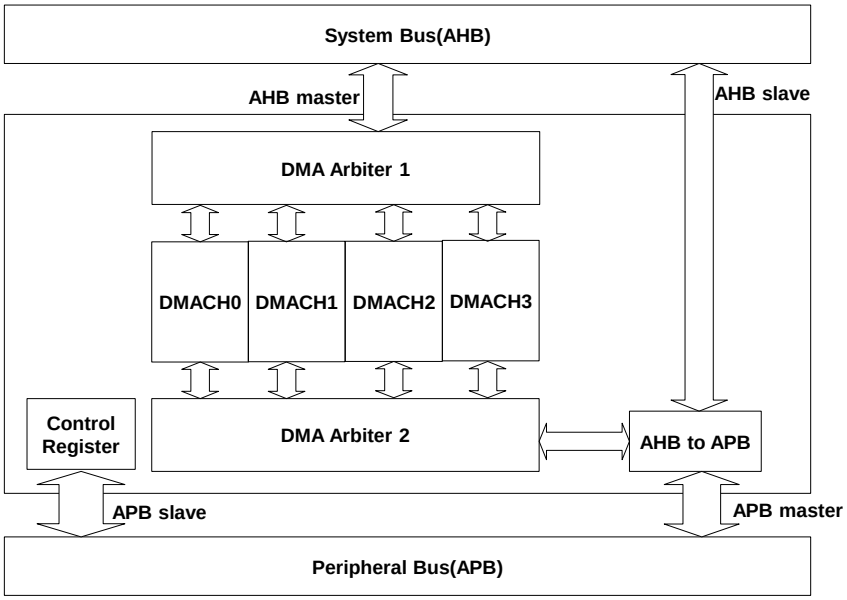


Figure 16-1 DMA Functional Block Diagram

16.4 Register Address

Table 16-1 DMA (DMA Base Address:0x40010000)

Name	Type	Address	Contents	Default
DMA_IE	R/W	0x0000	DMA interrupt enable register	0x000
DMA_STS	R/W	0x0004	DMA status register	0x0000
DMA_C0CTL	R/W	0x0010	DMA channel 0 control register	0x00000000
DMA_C0SRC	R/W	0x0014	DMA channel 0 source address register	0x00000000
DMA_C0DST	R/W	0x0018	DMA channel 0 destination address register	0x00000000
DMA_C0LEN	R	0x001C	DMA channel 0 transmit length register	0x0000
DMA_C1CTL	R/W	0x0020	DMA channel 1 control register	0x00000000
DMA_C1SRC	R/W	0x0024	DMA channel 1 source address register	0x00000000
DMA_C1DST	R/W	0x0028	DMA channel 1 destination address register	0x00000000
DMA_C1LEN	R	0x002C	DMA channel 1 transmit length	0x0000

			register	
DMA_C2CTL	R/W	0x0030	DMA channel 2 control register	0x00000000
DMA_C2SRC	R/W	0x0034	DMA channel 2 source address register	0x00000000
DMA_C2DST	R/W	0x0038	DMA channel 2 destination address register	0x00000000
DMA_C2LEN	R	0x003C	DMA channel 2 transmit length register	0x0000
DMA_C3CTL	R/W	0x0040	DMA channel 3 control register	0x00000000
DMA_C3SRC	R/W	0x0044	DMA channel 3 source address register	0x00000000
DMA_C3DST	R/W	0x0048	DMA channel 3 destination address register	0x00000000
DMA_C3LEN	R	0x004C	DMA channel 3 transmit length register	0x0000
DMA_AESCTL	R/W	0x0050	DMA AES control register	0x00000000
DMA_AESKEY0	R/W	0x0060	DMA AES-0 register	0x00000000
DMA_AESKEY1	R/W	0x0064	DMA AES-1 register	0x00000000
DMA_AESKEY2	R/W	0x0068	DMA AES-2 register	0x00000000
DMA_AESKEY3	R/W	0x006C	DMA AES-3 register	0x00000000
DMA_AESKEY4	R/W	0x0070	DMA AES-4 register	0x00000000
DMA_AESKEY5	R/W	0x0074	DMA AES-5 register	0x00000000
DMA_AESKEY6	R/W	0x0078	DMA AES-6 register	0x00000000
DMA_AESKEY7	R/W	0x007C	DMA AES-7 register	0x00000000

16.5 Register Definition

16.5.1 DMA_IE Register

Table 16-2 DMA_IE Register

Bit	Name	Type	Contents	Default
31:12	-	-	Reserved.	0
11	C3DAIE	R/W	Channel 3 data abort interrupt enable 0:disable	0x0

			1:enable	
10	C2DAIE	R/W	Channel 2 data abort interrupt enable 0:disable 1:enable	0x0
9	C1DAIE	R/W	Channel 1 data abort interrupt enable 0:disable 1:enable	0x0
8	C0DAIE	R/W	Channel 0 data abort interrupt enable 0:disable 1:enable	0x0
7	C3FEIE	R/W	Channel 3 all packets transmit interrupt enable 0:disable 1:enable	0x0
6	C2FEIE	R/W	Channle 2 all packets transmit interrupt enable 0:disable 1:enable	0x0
5	C1FEIE	R/W	Channel 1 all packets transmit interrupt enable 0:disable 1:enable	0x0
4	C0FEIE	R/W	Channel 0 all packets transmit interrupt enable 0:disable 1:enable	0x0
3	C3PEIE	R/W	Channel 3 single packet transmit interrupt enable 0:disable 1:enable	0x0
2	C2PEIE	R/W	Channel 2 single packet transmit interruptenable 0:disable 1:enable	0x0
1	C1PEIE	R/W	Channel 1 single packet transmit interrupt enable 0:disable 1:enable	0x0

0	C0PEIE	R/W	Channel 0 single packet transmit interrupt enable 0:disable 1:enable	0x0

16.5.2 DMA_STS Register

Table 16-3 DMA_STS Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15	C3DA	R/C	Channel 3 data interrupt bit. Write 1 to clear the bit.	0x0
14	C2DA	R/C	Channel 2 data interrupt bit. Write 1 to clear the bit.	0x0
13	C1DA	R/C	Channel 1 data interrupt bit. Write 1 to clear the bit.	0x0
12	C0DA	R/C	Channel 0 data interrupt bit. Write 1 to clear the bit.	0x0
11	C3FE	R/C	Channel 3 all packets transmit interrupt bit. Write 1 to clear the bit.	0x0
10	C2FE	R/C	Channel 2 all packets transmit interrupt bit. Write 1 to clear the bit.	0x0
9	C1FE	R/C	Channel 1 all packets transmit interrupt bit. Write 1 to clear the bit.	0x0
8	C0FE	R/C	Channel 0 all packets transmit interrupt bit. Write 1 to clear the bit.	0x0
7	C3PE	R/C	Channel 3 single packet transmit interrupt bit. Write 1 to clear the bit.	0x0
6	C2PE	R/C	Channel 2 single packet transmit interrupt bit. Write 1 to clear the bit.	0x0
5	C1PE	R/C	Channel 1 single packet transmit interrupt bit. Write 1 to clear the bit.	0x0
4	C0PE	R/C	Channel 0 single packet transmit interrupt bit. Write 1 to clear the bit.	0x0
3	C3BUSY	R	DMA channel 3 working status register 0:idle 1:work	0x0
2	C2BUSY	R	DMA channel 2 working status register 0:idle	0x0

			1:work	
1	C1BUSY	R	DMA channel 1 working status register 0:idle 1:work	0x0
0	C0BUSY	R	DMA channel 0 wokring status register 0:idle 1:work	0x0

16.5.3 DMA_CxCTL Register

Table 16-4 DMA_CxCTL Register is used to control DMA. The data will be locked in DMA channel after the register data starting to transmit. Therefore, any modification of the register will not affect DMA transmitting. Only STOP bit can stop DMA transmission immediately.

Table 16-4 DMA_CxCTL Register

Bit	Name	Type	Contents	Default
31:24	FLEN	R/W	Packet number register. All packets number in DMA transmit bit (FLEN+1). The total length of DMA transmission is (FLEN+1)* (PLEN+1).	0x0
23:16	PLEN	R/W	Packet length register. Single packet number is (PLEN+1). The total length of DMA transmission is (FLEN+1)* (PLEN+1).	0x0
15	STOP	R/W	Force to stop DMA transmission. Write 1 in the bit, it will force DMA chananl to the idle status. If another DMA transmission needs to distribute to the same channel, user should write 0 in the bit. 0:default the working status 1:force to stop DMA transmission	0x0
14	AESEN	R/W	Enable AES encryption/decryption function in DMA channel, and only DMA channel 3 supports AES function. When enable AES function, SIZE should be set 32-bit, SMODE and DMODE should be set 1 or 2. When enable AES function, PLEN should set integer multiple of 4. 0:disable 1:enable	0x0
13	CONT	R/W	Continuous mode. DMA transmission will continue until	0x0

			STOP bit set 1. After DMA completed all packets transmission each time, it will execute the continuous transmission from start. 0:without continuous mode 1:continuous mode	
12	TMODE	R/W	Transmit Mode Select Register 0:DMA request source. Only transmit one data in each trigger. 1:DMA request source. Only transmit one data in each packet.	0x0
11:7	DMASEL	R/W	DMA request source selection. The detail information in each DMA request source, please refer to **Table 16-5**.	0x0
6:5	DMODE	R/W	Destination address mode. 0:fixed 1:Automatic increase, but return the initial value after single packet transmitted. 2:Automatic increase, but return the initial value after all packets transmitted. 3:reserved	0x0
4:3	SMODE	R/W	Source address mode 0:fixed 1:Automatic increase, but return the initial value after single packet transmitted. 2:Automatic increase, but return the initial value after all packets transmitted. 3:reserved	0x0
2:1	SIZE	R/W	Transmit length mode 0:byte (8 bits) 1:half-word (16 bits) 2:word (32 bits) 3:reserved	0x0
0	EN	R/W	DMA channel enable register	0x0

			0: disable DMA channel (When CONT is 1, it is invalid.) 1:enable DMA channel. When CONT is 0, after DMA transmitted, the bit will be cleared 0 by hardware.	

Table 16-5 DMA Request Source Selection

DMASEL	Request Source	DMASEL	Request Souce	DMASEL	Request Source	DMASEL	Source
0	Software	8	UART3 TX	16	ISO78161 TX	24	UART 32K 0
1	ADC	9	UART3 RX	17	ISO78161 RX	25	UART 32K 1
2	UART0 TX	10	UART4 TX	18	TIMER 0	26	CMP1
3	UART0 RX	11	UART4 RX	19	TIMER 1	27	CMP2
4	UART1 TX	12	UART5 TX	20	TIMER 2	28	SPI3 TX
5	UART1 RX	13	UART5 RX	21	TIMER 3	29	SPI3 RX
6	UART2 TX	14	ISO78160 TX	22	SPI1 TX	30	SPI2 TX
7	UART2 RX	15	ISO78160 RX	23	SPI1 RX	31	SPI2 RX

16.5.4 DMA_CxSRC Register

Table 16-6 DMA_CxSRC Register

Bit	Name	Type	Contents	Default
31:0	SRC	R/W	DMA source address register. When Size in DMA_CxCTL is 1, the register must align with "half-word". When SIZE is 2, the register must align with "word". When SRC set 0x4001xxxx, it will automatic change to IO reading.	0x00000000

16.5.5 DMA_CxDST Register

Table 16-7 DMA_CxDST Register

Bit	Name	Type	Contents	Default

31:0	DST	R/W	DMA destination address register. When SIZE in DMA_CxCTL is 1, the register must align with "half-word". When SIZE in DMA_CxCTL is 2, the register must align with "word". When DST set 0x4001xxxx, it will automatic change to IO writing.	0x00000000

16.5.6 DMA_CxLEN Register

Table 16-8 DMA_CxLEN Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved.	0
15:8	CFLEN	R	Currently already transmitted packet number. The total length of DMA already transmitted: CFLEN * (PLEN +1) + CPLEN It will clear 0 after DMA finished all packets transmission.	0x00
7:0	CPLEN	R	Currently already transmitted data number in single. The length of DMA already transmitted: CFLEN * (PLEN +1) + CPLEN. It will clear 0 after DMA finished single packet transmission.	0x00

16.5.7 DMA_AESCTL Register

Table 16-9 DMA_AESCTL Register

Bit	Name	Type	Contents	Default
31:4	-	-	Reserved.	0
3:2	MODE	R/W	AES mode select register. 0:AES128 1:AES192 2:AES256 3:reserved	0x0
1	-	-	Reserved.	0
0	ENC	R/W	AES encode/decode select register 0:decode	0x0

			1:encode	

16.5.8 DMA_AESKEYx Register

Table 16-10 DMA_AESKEYx Register

Bit	Name	Type	Contents	Default
31:0	KEYx	R/W	AES key register: KEY0:bit 31~0 KEY1:bit 63~32 KEY2:bit 95~64 KEY3:bit 127~96 KEY4:bit 159~128 KEY5:bit 191~160 KEY6:bit 223~192 KEY7:bit 255~224 When mode is AES128, we only use bit 127~0. When mode is AES192, we only use bit 191~0. When mode is AES256, we only use bit 255~0.	0x00000000

Note: X=0~7;

17. UART Controller

17.1 Introduction

UART controller is used to pass UART protocol to transmit/ receive data. V85XXP has 6 UART controllers at most, each controller can independent program and with CPU interruption. UART controller can support without parity 8-bit data and with parity 9-bit data transmission. Both transmiter and receiver has a data buffer and a shift register. The setting of UART controller will reset after woke-up from sleep or dee-sleep mode. User should restore settings by manual after woke-up from these 2 modes. The supporting range of UART baud rate 300~819200bps.

17.2 Features

--Programmble baudrate generator;

--The data length is 8 bits;

--With or without parity check;

--Parity check error detection;

--The transmit/ receive interrupt flag bit;

-- The transmit/ receive overflow interrupt flag bit.

17.3 Functional Block Diagram

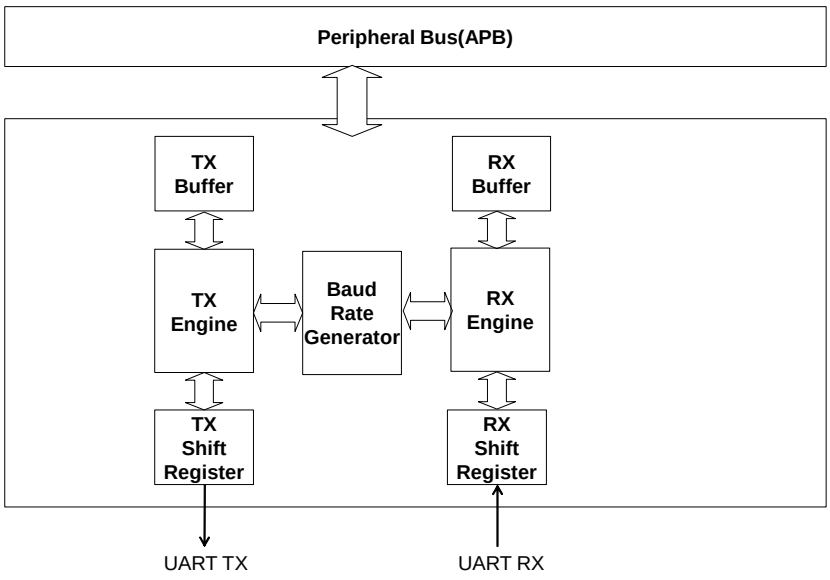


Figure 17-1 UART Functional Block Diagram

17.4 Register Address

Table 17-1 UART (UART Base Address:0x40011800)

Name	Type	Address	Contents	Default
UART0_DATA	R/W	0x0000	UART0 data register	0x00
UART0_STATE	R/C	0x0004	UART0 status register	0x00
UART0_CTRL	R/W	0x0008	UART0 control register	0x000
UART0_INTSTS	R/C	0x000C	UART0 interrupt status register	0x00
UART0_BAUDDIV	R/W	0x0010	UART0 baudrate divide register	0x00000
UART0_CTRL2	R/W	0x0014	UART0 control register 2	0x0
UART1_DATA	R/W	0x0020	UART1 data register	0x00
UART1_STATE	R/C	0x0024	UART1 status register	0x00
UART1_CTRL	R/W	0x0028	UART1 control register	0x000
UART1_INTSTS	R/C	0x002C	UART1 interrupt status register	0x00
UART1_BAUDDIV	R/W	0x0030	UART1 baudrate divide register	0x00000
UART1_CTRL2	R/W	0x0034	UART1 control register 2	0x0
UART2_DATA	R/W	0x0040	UART2 data register	0x00
UART2_STATE	R/C	0x0044	UART2 status register	0x00
UART2_CTRL	R/W	0x0048	UART2 control register	0x000
UART2_INTSTS	R/C	0x004C	UART2 interrupt status register	0x00
UART2_BAUDDIV	R/W	0x0050	UART2 baudrate divide register	0x00000
UART2_CTRL2	R/W	0x0054	UART2 control register 2	0x0
UART3_DATA	R/W	0x0060	UART3 data register	0x00
UART3_STATE	R/C	0x0064	UART3 status register	0x00
UART3_CTRL	R/W	0x0068	UART3 control register	0x000
UART3_INTSTS	R/C	0x006C	UART3 interrupt status register	0x00
UART3_BAUDDIV	R/W	0x0070	UART3 baudrate divide register	0x00000
UART3_CTRL2	R/W	0x0074	UART3 control register 2	0x0
UART4_DATA	R/W	0x0080	UART4 data register	0x00
UART4_STATE	R/C	0x0084	UART4 status register	0x00
UART4_CTRL	R/W	0x0088	UART4 control register	0x000

UART4_INTSTS	R/C	0x008C	UART4 interrupt status register	0x00
UART4_BAUDDIV	R/W	0x0090	UART4 baudrate divide register	0x00000
UART4_CTRL2	R/W	0x0094	UART4 control register 2	0x0
UART5_DATA	R/W	0x00A0	UART5 data register	0x00
UART5_STATE	R/C	0x00A4	UART5 status register	0x00
UART5_CTRL	R/W	0x00A8	UART5 control register	0x000
UART5_INTSTS	R/C	0x00AC	UART5 interrupt status register	0x00
UART5_BAUDDIV	R/W	0x00B0	UART5 baudrate divide register	0x00000
UART5_CTRL2	R/W	0x00B4	UART5 control register 2	0x0

Table 17-2 MISC1 (MISC1 Base Address:0x40013000)

Name	Type	Address	Contents	Default
MISC1_IREN	R/W	0x000C	IR enable control register	0x00
MISC1_DUTYL	R/W	0x0010	IR modulated wave register for low-level width control	0x0000
MISC1_DUTYH	R/W	0x0014	IR modulated wave register for high-level width control	0x0000

17.5 Register Definition

17.5.1 UARTx_DATA Register

Table 17-3 UARTx_DATA Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved.	0
7:0	DATA	R/W	Read: receive data Write: transmit data	0x0

17.5.2 UARTx_STATE Register

Table 17-4 UARTx_STATE Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved.	0
7	DMATXDONE	R/C	Transmsit completed flag bit for DMA mode. When passed DMA to transmit data with bathes, it will	0x0

			automatic set 1 after transmitted. User must wait DMA to transmist, then can read this flag bit. Write 1 to clear the bit.	
6	RXPSTS	R	Receive the parity check flag bit. The bit represents the last reciving data with parity check.	0x0
5	TXDONE	R/C	Transmitted flag bit. When the single byte data transmitted, the bit will be set 1. Write 1 in the bit, or write 1 in TXDONEIF of UARTx_INSTS register, the bit will be cleared 0.	0x0
4	RXPE	R/C	Receive parity error flag bit. When the parity data is different with the expected value, the bit will set 1. Write 1 in the bit, or write 1 in RXPEIF in UARTx_INTSTS register, the bit will be cleared 0.	0x0
3	RXOV	R/C	Receive buffer overflows flag bit. When RXFULL is 1 and received a data from RX, the bit wil be set 1. Write 1 in the bit, or write 1 in RXOVIF of UARTx_INTSTS, the bit will be cleared 0.	0x0
2	TXOV	R/C	Transmit buffer overflows flag bit. When UART transmission did not complete and there is a new data writing in UARTx_DATA register, the bit will be set 1. Write 1 in the bit, or write 1 in TXOVIF of UARTx_INTSTS register, the bit will be cleared 0.	0x0
1	RXFULL	R	Flag bit when receive buffer is full. 0: Receive buffer is empty 1: Receive buffer is full When UARTRX received the data, the bit will be set 1. After user read the data from UARTx_DATA, the bit will be cleared 0.	0x0
0	-	-	Reserved.	0

17.5.3 UARTx_CTRL Register

Table 17-5 UARTx_CTRL Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved	0x0
8	TXDONEIE	R/W	Transmit completed and interrupt enable	0x0

7	RXPEIE	R/W	Receive interrupt enable of parity error	0x0
6	-	-	Reserved	0x0
5	RXOVIE	R/W	Receive overflows interrupt enable	0x0
4	TXOVIE	R/W	Transmit overflow interrupt enable	0x0
3	RXIE	R/W	Receive interrupt enable	0x0
2	-	-	Reserved	0x0
1	RXEN	R/W	Receive data enable	0x0
0	TXEN	R/W	Transmit data enable	0x0

17.5.4 UARTx_INTSTS Register

Table 17-6 UARTx_INTSTS Register

Bit	Name	Type	Contents	Default
31:5	-	-	Reserved	0x0
5	TXDONEIF	R/C	Transmit completed flag bit. When transmitted single byte and TXDONEIE is 1, the bit will be set 1. Write 1 in the bit, or write 1 in UARTx_STATE register, the bit will be cleared 0.	0x0
4	RXPEIF	R/C	Receive data parity error flag bit. When the parity data is different with the expected value, the bit will be set 1. Write 1 in the bit, or write 1 in UARTx_STATE register, the bit will be cleared 0.	0x0
3	RXOVIF	R/C	Receive data buffer overflow flag bit. When RXOVIE is 1, RXFULL is 1 and received a new data from RX, the bit will be set 1. Write 1 in the bit, or write 1 in RXOV of UARTx_STATE register. The bit will be cleared 0.	0x0
2	TXOVIF	R/C	Transmit data buffer overflow flag bit. When TXOVIE is 1, UART transmission did not complete and write a new data in UARTx_DATA register, the bit will be set 1. Write 1 in the bit, or write 1 in TXOV of UARTx_STATE register, the bit will be set 1.	0x0
1	RXIF	R/C	Receive data interrupt flag bit. When UARTx_DATA register received a data, the bit will be set 1. Write 1 to clear the bit.	0x0
0	-	-	Reserved	0

17.5.5 UARTx_BAUDDIV Register

Table 17-7 UARTx_BAUDDIV Register

Bit	Name	Type	Contents	Default
31:20	-	-	Reserved	0
19:0	BAUDDIV	R/W	Buadrate divide register. Before enable UART, we must completely set the register. BAUDDIV=APBCLK/Baudrate. For example, when APBCLK=6.5536MHz, baud rate is 9600bps, the register value is equal to 6553600/9600=682.	0x0

17.5.6 UARTx_CTRL2 Register

Table 17-8 UARTx_CTRL2 Register

Bit	Name	Type	Contents	Default
31:4	-	-	Reserved	0
3:1	PMODE	R/W	UART data check mode control register 0:without parity bit, 1+8+1 mode. 1:even check 3:odd check 5:parity bit is always 0. 7:parity bit is always 1. Others: Reserved	0x0
0	MSB	R/W	Data bit transmit order control register 0:low-bit transmit first (LSB) 1:high-bit transmit first (MSB)	0x0

17.5.7 MISC1_IREN Register

Table 17-9 MISC1_IREN Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0
5:0	IREN	R/W	IR enable control register. Each bit of the register will	0x00

			correspond with 1 UARTTX channels. When IREN[x] set 1, it represents UARTX[x] output is infrared (IR) modem signal.	

17.5.8 MISC1_DUTYL Register

Table 17-10 MISC1_DUTYL Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	DUTYL	R/W	Infrared (IR) modulated wave register for low-level width control. Low pulse width will be (DUTYL+1)*APBCLK cycle.	0x0000

17.5.9 MISC1_DUTYH Register

Table 17-11 MISC1_DUTYH Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	DUTYH	R/W	Infrared (IR) modulated wave register for high-level width control. High puse width will be (DUTYH+1)*APBCLK cycle.	0x0000

18. UART32K Controller

18.1 Introduction

UART32K controller is used UART protocol to receive data. There are 2 independent UART32K controllers in V85XXP, and its input pins will be selected from input pins (RX0~RX3) of UART0~UART3. The operating frequency of UART32K controller is RTCCLK, so it can work in sleep or deep-sleep mode. The typical baud rate of UART32K is 9600bps, and the supporting data length is 8-bit which is without parity check 8-bit data, and with parity check 9-bit data transmission. There are 1 data buffer and 1 shift register in receiver. The supporting baud rate of UART32K is 300~14400bps.

18.2 Features

--Support sleep or deep-sleep mode in work;

--Support sleep or deep-sleep mode wake-up function;

--Support programmable buadrate generator;

--Support without parity check 8-bit data and with parity check 9-bit data transmission;

--Support parity error detected;

-- The Receive data interrupt flag bit;

--Receive parity error flag bit;

--Receive overflows interrupt flag bit;

18.3 Functional Block Diagram

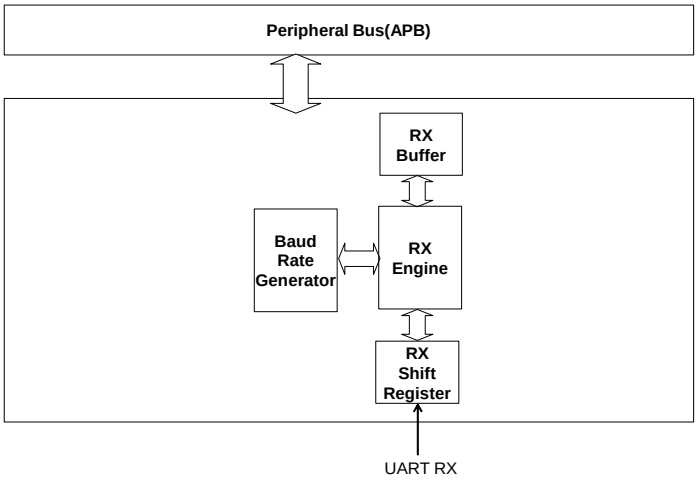


Figure 18-1 UART32K Functional Block Diagram

18.4 Register Address

Table 18-1 UART32K (UART32K0 Base Addres: 0x40014100)

Name	Type	Address	Contents	Default
U32K0_CTRL0	R/W	0x0000	UART32K0 control register 0	0x000
U32K0_CTRL1	R/W	0x0004	UART32K0 control register 1	0x00
U32K0_BAUDDIV	R/W	0x0008	UART32K0 baudrate divide register	0x4B00
U32K0_DATA	R	0x000C	UART32K0 receive data register	--
U32K0_STS	R/C	0x0010	UART32K0 interrupt status register	0x0

UART32K1 Base Address: 0x40014180

Name	Type	Address	Contents	Default
U32K1_CTRL0	R/W	0x0000	UART32K1 control register 0	0x00
U32K1_CTRL1	R/W	0x0004	UART32K1 control register 1	0x00
U32K1_BAUDDIV	R/W	0x0008	UART32K1 baudrate divide register	0x4B00
U32K1_DATA	R	0x000C	UART32K1 receive data register	--
U32K1_STS	R/C	0x0010	UART32K1 interrupt status register	0x0

18.5 Register Definition

18.5.1 U32Kx_CTRL0 Register

Table 18-2 U32Kx_CTRL0 Register

Bit	Name	Type	Contents	Default
31:9	-	-	Reserved	0
8	WKUMODE	R/W	Wake-up mode control. When RXIE=1, the register will be effective. 0:Only receive data, it will wake-up (no matter check is correct or not). 1:Only when parity bit and stop bit are correct, it will be wok -up.	0x0
7:6	DEBSEL	R/W	Debounce control. 0:no debounce 1:2x RTCCLKs cycle to debounce. 2:3x RTCCLKs cycle to debounce.	0x0

			3:4x RTCCLK cycle to debounce. When UART bus has interference, enable debounce function can decrease the interference when receving data. But data will be lost during debouncing period.	
5:3	PMODE	R/W	UART data check control register. 0:without parity bit, 1+8+1 mode. 1:even check 3:odd check 5:parity bit is always 0 7:parity bit is always 1 Others: reserved	0x0
2	MSB	R/W	Data bit received order control. 0:low-bit received first (LSB) 1:high-bit received first (MSB)	0x0
1	ACOFF	R/W	Auto-calibration control. In order to receive data correctly in RTCCLK, there is an auto-calibration mechanism in controller. In default condtion, hardware auto-calibration is enable, and write 1 in the bit to disable hardware auto-calibration mechanism. 0:enable auto-calibration 1:disable auto-calibartion	0x0
0	EN	R/W	UART32K enable. Set 1 to the bit, UART32K controller will start to receive data after 2 RTTCCLK cycles. Therefore, before set 1 to the bit, we must set the correct parameters in each U32K controller. 0:disable 1:enable	0x0

18.5.2 U32Kx_CTRL1 Register

Table 18-3 U32Kx_CTRL1 Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0
5:4	RXSEL	R/W	Receive data source control.	0x0

			0:from UART RX0(IOA12) 1: from UART RX1(IOA13) 2:from UART RX2(IOA14) 3:from UART RX3(IOA15)	
3	-	-	Reserved	0
2	RXOVIE	R/W	Receive overflows interrupt/wake-up enable	0x0
1	RXPEIE	R/W	Receive parity check error interrutptive/ wake-up enable	0x0
0	RXIE	R/W	Receive interrupt/wake-up enable. After enabled, when WKUMODE is 0, it will be woke-up once received serial port data; when WKUMODE is 1, it will be woke-up only when parity bit and stop bit correctly.	0x0

18.5.3 U32Kx_BAUDDIV Register

Table 18-4 U32Kx_BAUDDIV Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	BAUDDIV	R/W	Buadrate divide register. Before enable UART32K, we must set the register. BAUDDIV=65536*Baud_rate/RTCCLK。 For example, when baudrate is 9600bps, RTCCLK frequency is 32768, 65536*9600/32768=19200. When PSCA=1 in RTC_PSCA register, BAUDDIV should be calculated by frequency after RTCCLK divided.	0x4B00

18.5.4 U32Kx_DATA Register

Table 18-5 U32Kx_DATA Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	DATA	R	Read: receive data	--

18.5.5 U32Kx_STS Register

Table 18-6 U32Kx_STS Register

Bit	Name	Type	Contents	Default
31:3	-	-	Reserved	0
2	RXOV	R/C	Received buffer overflows flag bit. When FIFO was full and received a new data from RX, the bit set 1. Write 1 to clear the bit.	0x0
1	RXPE	R/C	Received parity error flag bit. When received the parity value error, the bit set 1. Write 1 to clear the bit.	0x0
0	RXIF	R/C	Received interrupt flag bit. When WKUMODE is 0, it will be set 1 once received serial data; when WKUMODE is 1, only when parity bit and stop bit coreeclty, it will set 1. Write 1 to clear the bit.	0x0

19. ISO7816 Controller

19.1 Introduction

ISO7816 is an enhanced UART protocol which can process half-duplex communication in 2 buses. V85XXP intergrated 2 independent programmable ISO7816 controller, and independent CPU interrupt. It is embedded a clock divider in IP in order to provide 1~5MHz clock to ISO7816 devices. After woke-up from sleep or deep-sleep mode, ISO7816 controller will be reset; therefore, we should restore the related settings after program be woke-up. The supporting range of ISO7816: 200~2625000bps.

19.2 Features

--Support programmable baudrate generator;

--Support half-duplex transmit/ receive;

--Support resend mechanism, and support resend numbers control;

--Support clock division.

19.3 Functional Block Diagram

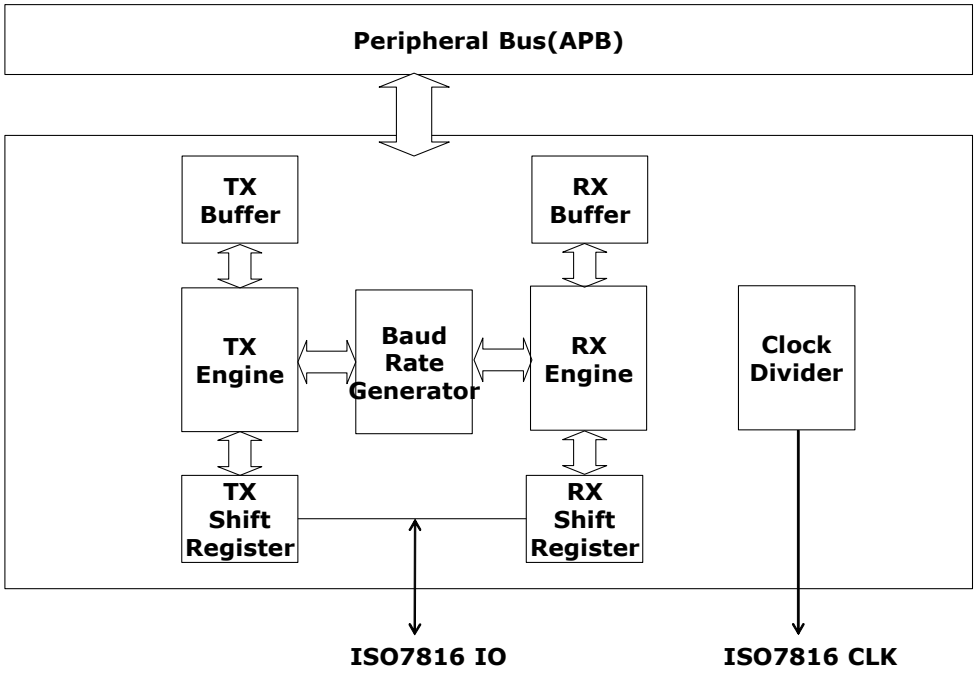


Figure 19-1 ISO7816 Functional Block Diagram

19.4 Register Address

Table 19-1 ISO7816 Address (ISO7816 Base Address:0x40012000)

Name	Type	Address	Contents	Default
ISO78160_BAUDDIVL	R/W	0x0004	ISO78160 baudrate low-byte register	0x00
ISO78160_BAUDDIVH	R/W	0x0008	ISO78160 baudrate high-byte register	0x00
ISO78160_DATA	R/W	0x000C	ISO78160 data register	0x00
ISO78160_INFO	R/C	0x0010	ISO78160 information register	0x00
ISO78160_CFG	R/W	0x0014	ISO78160 control register	0x00
ISO78160_CLK	R/W	0x0018	ISO78160 clock divider control register	0x00
ISO78161_BAUDDIVL	R/W	0x0044	ISO78161 baud rate low-byte register	0x00
ISO78161_BAUDDIVH	R/W	0x0048	ISO78161 baud rate high-byte register	0x00
ISO78161_DATA	R/W	0x004C	ISO78161 data register	0x00
ISO78161_INFO	R/C	0x0050	ISO78161 information register	0x00
ISO78161_CFG	R/W	0x0054	ISO78161 control register	0x00
ISO78161_CLK	R/W	0x0058	ISO78161 clock divider control register	0x00

19.5 Register Definition

19.5.1 ISO7816x_BAUDDIVL Register

Table 19-2 ISO7816x_BAUDDIVL Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	BAUDDIVL	R/W	The low-byte of baudrate divider	0x0

19.5.2 ISO7816x_BAUDDIVH Register

Table 19-3 ISO7816x_BAUDDIVH Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	BAUDDIVH	R/W	The high-byte of baudrate divider. Baudrate counter is from BAUDDIV to 0xFFF, so the baudrate formula: BAUDDIV=0x10000−(APBCLK/ baud rate) For example: When APBCLK=6.5536MHz, baud rate =9600bps, the register value should be: 0x10000-(6553600/9600)=0xFD56。	0x0

19.5.3 ISO7816x_DATA Register

Table 19-4 ISO7816x_DATA Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	DATA	R/W	Read: receive data. When the receiving data is not completed, and there is a new data receiving, OVIF bit will be set 1. Write: transmit data. For the serial port writing, it will trigger one data transmit of ISO7816 bus.	0x0

19.5.4 ISO7816x_INFO Register

Table 19-5 ISO7816x_INFO Register

Bit	Name	Type	Contents	Default
31:10	-	-	Reserved	0
9	DMATXDONE	R/C	DMA transmit completed flag bit. When batch data is sent via DMA, it will be automatically set to 1 when all transmissions are completed. User must wait until the DMA transmission is completed before reading this flag bit. Write 1 to clear this bit.	0x0
8	TXRTYERRIF	R/C	The transmit retry error counter interrupt flag bit. When the number of retries reaches the limit setting in the TXRTYCNT register, this bit will be set to 1. When the bit is read as 1, it is necessary to disable and reinitialize the entire ISO7816 module through the EN bit in the ISO7816x_CFG register. Write 1 to clear this bit.	0x0
7	RXOVIF	R/C	Received data overflows flag bit. When already received data did not read by CPU but already received another new data, the bit will set 1. Write 1 to cleat the bit. Receive overflow flag bit. When the received data is not read by the CPU and another data is received, this bit will be set to 1. Write 1 to clear this bit.	0x0
6	TXDONEIF	R/C	Transmit done interrupt flag bit. This bit will only be set when the received acknowledgement (ACK) is 1 or the number of retries	0x0

			reaches the setting in TXRTYCNT. Write 1 to clear this bit.	
5	RXIF	R/C	Received data interrupt flag. When a byte of data is successfully received and an acknowledge signal (ACK) is sent, this bit will be set to 1. Write 1 to clear this bit.	0x0
4:3	-	-	Reserved	0x0
2	RXERRIF	R/C	Received data checksum error flag bit. When received data checksum and error, the bit will set 1. Write 1 to clear the bit.	0x0
1	CHKSUM	R	Transmitted or received data checksum bit. The bit can be read/write by CPU, but the original information will lost.	0x0
0	RXACK	R	Received ACK during the transmitted done. The bit can be read/write by CPU, but the original information will lost.	0x0

19.5.5 ISO7816x_CFG Register

Table 19-6 ISO7816x_CFG Register

Bit	Name	Type	Contents	Default
31:17	-	-	Reserved	0
16	RXACKSET	R/W	The setting of received ACK length. 0:2 bits 1:1 bit	0x0
15:12	TXRTYCNT	R/W	The times of retry setting register. 0: no retry (Only receive ACK to 0, TXRTYERRIF immediately setted 1; meanwhile, ISO7816 stop transmitting.) 1:retry 1 time 2:retry 2 times … 15:retry 15 times When it reached the retry times but we still received ACK error, TXRTYERRIF bit will set 1; meanwhile, ISO7816 stop transmitting, and it did not ask request for DMA controller. User can use DMATXDONE to	0x0

			confirm whether transmission been stopped or not, and check it whether error happeneded via TXRTYERRIF. When TXRTYERRIF is 1, user must write 1 in the "STOP" bit in DMA_CxCTL register in order to stop DMA. If DMA transmission needs to be reset, please write 0 in "STOP" bit.	
11	LSB	R/W	Data bit transmit/ receive order control register 0:high-bit transmit first (MSB) 1:low-bit transmit first (LSB)	0x0
10	-	R/W	Reserved. We suggest user set 1.	0x0
9	AUTORXACK	R/W	When received the error data, it will automatic respond ACK to 0, and re-transmit the data. 0:Disable automatic re-transmit mode 1:enable automatic re-transmit mode	0x0
8	TXRTYERRIE	R/W	Transmit retry error interrupt enable registerWhen it reached the retry times but we still received ACK error, TXRTYERRIF bit will be set 1.	0x0
7	RXOVIE	R/W	Receive data overflow interrupt enable register	0x0
6	TXDONEIE	R/W	Interrupt enable register for transmit completed.	0x0
5	RXIE	R/W	Receiving interrupt enable register	0x0
4	ACKLEN	R/W	After received error data, transmit ACK low-level length. 0:1 bit 1:2 bits	0x0
3	-	R/W	Reserved	0x0
2	RXERRIE	R/W	Interrupt enable register for receive data error	0x0
1	CHKP	R/W	Parity check control register 0:even check 1:odd check	0x0
0	EN	R/W	ISO7816 enable register 0:disable ISO7816 function 1:enable ISO7816 function	0x0

19.5.6 ISO7816x_CLK Register

Table 19-7 ISO7816x_CLK Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7	CLKEN	R/W	ISO7816 clock output enable 0:disable clock output 1:enable clock output	0x0
6:0	CLKDIV	R/W	ISO7816 clock divider value 0:APBCLK/1 1:APBCLK/2 2:APBCLK/3 … 127:APBCLK/128	0x0

The following table shows ISO7816 data bit format.

Table 19-8 ISO7816 Data Bit Foramt

bit	0	1~8	9	10	11	12	0	…
Transmit Direction	Transmitter→ Receiver			Receiver→ Transmitter		--	Transmitter→ Receiver	
Definition	Start bit	Data	Parity bit	ACK*		Wait	Start bit	…
Value	0	MSB→LSB	P	ACK*		1	0	…
TX	0	MSB→LSB	P	1			0	…
RX	1	1	1	ACK*		1	1	…
Description	10 bits data			3 bits protective time			next packet	

If ACK is 0, RX will be reset from 1 to 0 in the middle of the 10th bit, and the 11^{th}-bit and 12^{th}-bit will be set 1, controlled by ACKLEN in ISO7816x_CFG.

There are 10 bits in total for transmission, including 1 start bit, 8 datas and 1 parity bit. There are 3 bits protective time to the receiver checks the correctness of the receiver and sends a 1-bit or 2-bit response ACK.. Both the transmitter and receiver should remain in the high state at bit 12, waiting for the next data packet.

20. Timer/PWM Controller

20.1 Introduction

There are 8 timers in V85XXP. Four of them are 32-bit timers which is used to timing function. Another four of them are 16-bit timers which possessed PWM comparsion and capture function. Each timer can independent produce a CPU interruption. Each PWM has 3 outputs which possessed the different waveforms. The settings of Timer/PWM controller will be reset after woke-up from sleep or deep-sleep mode. User should reset the settings by manual after it woke-up from these 2 modes.

20.2 Features

--4x 32-bit normal timers;

--4x 16-bit PWM output and capture timers;

--Each PWM timer at most has 3 outputs and 3 intputs;

--There are 8 output modes selectable.

20.3 Functional Block Diagram

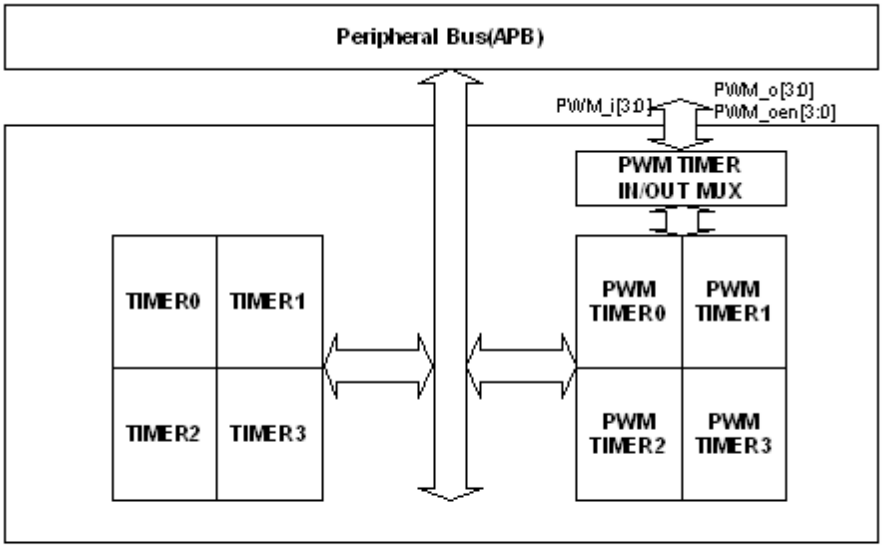


Figure 20-1 Timer Functional Block Diagram

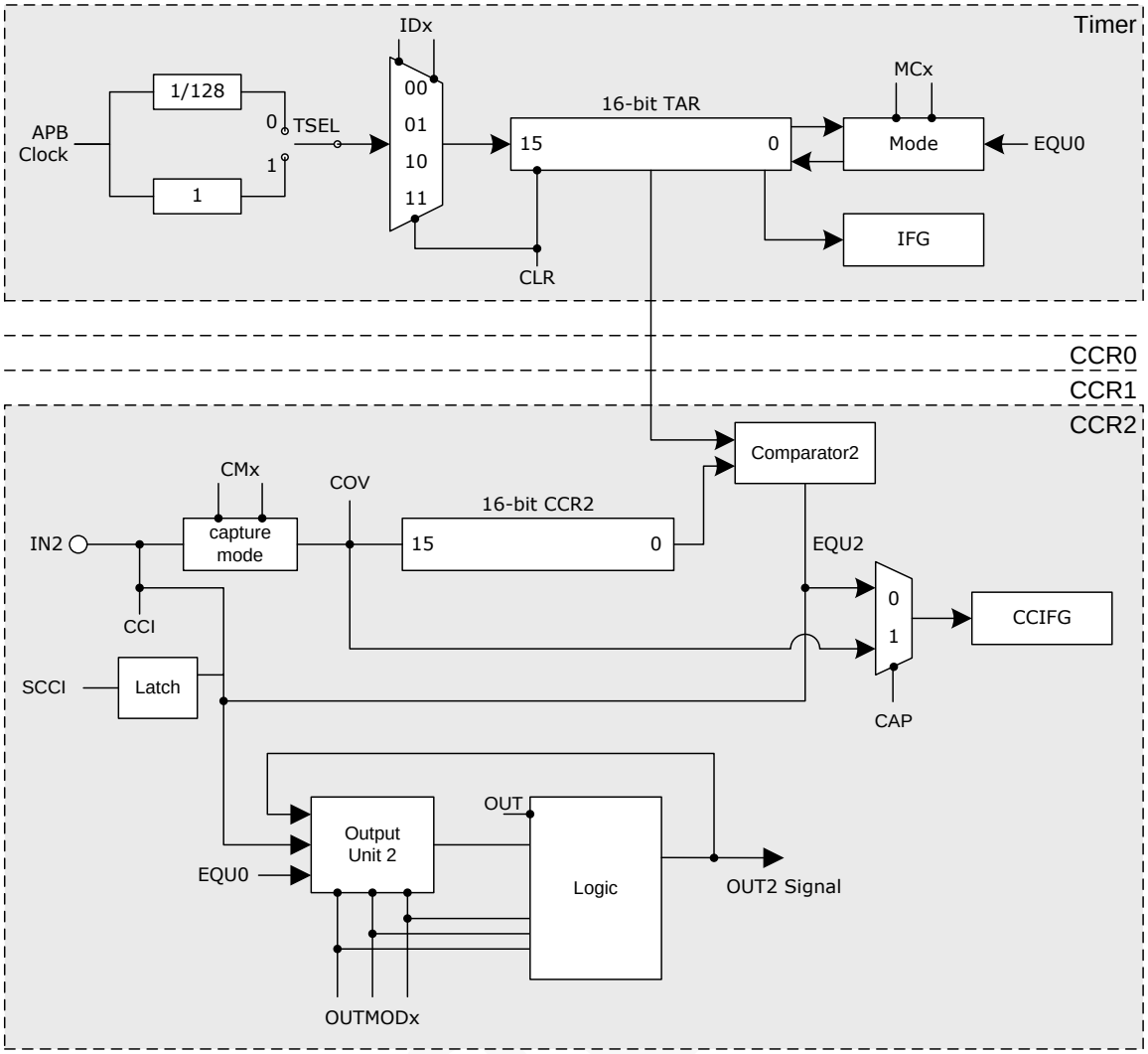


Figure 20-2 PWM Timer Functional Block Diagram

20.4 Register Address

Table 20-1 32-bit TIMER (32-bit TIMER Base Address:0x40012800)

Name	Type	Address	Contents	Default
TMR0_CTRL	R/W	0x0000	Timer0 control register	0x0
TMR0_VALUE	R/W	0x0004	Timer0 real time counting register	0x00000000
TMR0_RELOAD	R/W	0x0008	Timer0 reloads register	0x00000000
TMR0_INTSTS	R/C	0x000C	Timer0 interrupt status register	0x0
TMR1_CTRL	R/W	0x0020	Timer1 control register	0x0
TMR1_VALUE	R/W	0x0024	Timer1 real time counting register	0x00000000
TMR1_RELOAD	R/W	0x0028	Timer1 reloads register	0x00000000
TMR1_INTSTS	R/C	0x002C	Timer1 interrupt status register	0x0

TMR2_CTRL	R/W	0x0040	Timer2 control register	0x0
TMR2_VALUE	R/W	0x0044	Timer2 real time counting register	0x00000000
TMR2_RELOAD	R/W	0x0048	Timer2 reloads register	0x00000000
TMR2_INTSTS	R/C	0x004C	Timer2 interrupt status register	0x0
TMR3_CTRL	R/W	0x0060	Timer3 control register	0x0
TMR3_VALUE	R/W	0x0064	Timer3 real time counting register	0x00000000
TMR3_RELOAD	R/W	0x0068	Timer3 reloads register	0x00000000
TMR3_INTSTS	R/C	0x006C	Timer3 interrupt status register	0x0

Table 20-2 16-bit PWM TIMER (16-bit PWM TIMER Base Address:0x40012900)

Name	Type	Address	Contents	Default
PWM0_CTL	R/W	0x0000	PWM Timer0 control register	0x00
PWM0_TAR	R	0x0004	PWM Timer0 real time counting register	0x0000
PWM0_CCTL0	R/W	0x0008	PWM Timer0 compare/capture control register 0	0x000
PWM0_CCTL1	R/W	0x000C	PWM Timer0 compare/ capture control register 1	0x000
PWM0_CCTL2	R/W	0x0010	PWM Timer0 compare/ capture control register 2	0x000
PWM0_CCR0	R/W	0x0014	PWM Timer0 compare/ capture data register 0	0x0000
PWM0_CCR1	R/W	0x0018	PWM Timer0 compare/ capture data register 1	0x0000
PWM0_CCR2	R/W	0x001C	PWM Timer0 compare/ capture data register 2	0x0000
PWM1_CTL	R/W	0x0020	PWM Timer1 control register	0x00
PWM1_TAR	R	0x0024	PWM Timer1 real time counting register	0x0000
PWM1_CCTL0	R/W	0x0028	PWM Timer1 compare/ capture control register 0	0x000
PWM1_CCTL1	R/W	0x002C	PWM Timer1 compare/ capture control register 1	0x000
PWM1_CCTL2	R/W	0x0030	PWM Timer1 compare/ capture control register 2	0x000

PWM1_CCR0	R/W	0x0034	PWM Timer1 compare/ capture data register 0	0x0000
PWM1_CCR1	R/W	0x0038	PWM Timer1 compare/ capture data register 1	0x0000
PWM1_CCR2	R/W	0x003C	PWM Timer1 compare/ capture data register 2	0x0000
PWM2_CTL	R/W	0x0040	PWM Timer2 control register	0x00
PWM2_TAR	R	0x0044	PWM Timer2 real time counting register	0x0000
PWM2_CCTL0	R/W	0x0048	PWM Timer2 compare/ capture control register 0	0x000
PWM2_CCTL1	R/W	0x004C	PWM Timer2 compare/ capture control register 1	0x000
PWM2_CCTL2	R/W	0x0050	PWM Timer2 compare/ capture control register 2	0x000
PWM2_CCR0	R/W	0x0054	PWM Timer2 compare/ capture data register 0	0x0000
PWM2_CCR1	R/W	0x0058	PWM Timer2 compare/ capture data register 1	0x0000
PWM2_CCR2	R/W	0x005C	PWM Timer2 compare/ capture data register 2	0x0000
PWM3_CTL	R/W	0x0060	PWM Timer3 control register	0x00
PWM3_TAR	R	0x0064	PWM Timer3 real time counting register	0x0000
PWM3_CCTL0	R/W	0x0068	PWM Timer3 compare/ capture control 0	0x000
PWM3_CCTL1	R/W	0x006C	PWM Timer3 compare/ capture control 1	0x000
PWM3_CCTL2	R/W	0x0070	PWM Timer3 compare/ capture control 2	0x000
PWM3_CCR0	R/W	0x0074	PWM Timer3 compare/ capture data register 0	0x0000
PWM3_CCR1	R/W	0x0078	PWM Timer3 compare/ capture data register 1	0x0000
PWM3_CCR2	R/W	0x007C	PWM Timer3 compare/ capture data register 2	0x0000
PWM_O_SEL	R/W	0x00F0	PWM output select register	0xDB51
PWM_I_SEL01	R/W	0x00F4	PWM0 PWM1 input select register	0x00390024

PWM_I_SEL23	R/W	0x00F8	PWM2 PWM3 input select register	0x0013000E

20.5 Register Definition

20.5.1 TMRx_CTRL Register

Table 20-3 TMRx_CTRL Register

Bit	Name	Type	Contents	Default
31:4	-	-	Reserved	0
3	INTEN	R/W	Timerx interrupt enable register	0x0
2	EXTCLK	R/W	Select the external clock signal ext_clk (IOB15)* as the clock source. The rising edge of ext_clk will be used as the enable signal of the internal counter. Every time when a rising edge of external clock ext_clk arrives, the internal counter subtracts 1. In this mode, the frequency of the external clock signal ext_clk should be lower than PCLK/6.	0x0
1	EXTEN	R/W	Select ext_clk (IOB15) pins as the clock enable IO port. When EXTEN is 1 and ext_clk is 1, the internal counter will subtracts 1 as PCLK clock frequency. When EXTEN is 1 and ext_clk is 0, the internal counter will not change. There are 2 simultaneously cycle clock in order to avoid the glitch es on the ext-clk. When EXTCLK and EXTEN enable at the same time, EXTCLK priority is higer than EXTEN.	0x0
0	EN	R/W	Timerx enable control register	0x0

Annotation (*): ext_clk (IOB15) is a pin named TIMEREXT_CLK (IOB15).

20.5.2 TMRx_VALUE Register

Table 20-4 TMRx_VALUE Register

Bit	Name	Type	Contents	Default
31:0	VALUE	R/W	Timerx real time counter register	0x00000000

20.5.3 TMRx_RELOAD Register

Table 20-5 TMRx_RELOAD Register

Bit	Name	Type	Contents	Default

31:0	RELOAD	R/W	Timerx reloads register. Each time timer count down to 0, RELOAD value will be overloaded to TMRx_VALUE timer, and restart count down again; meanwhile, INTSTS bit will ve set 1. The calculation formula RELOAD timer: RELOAD = Period * APBCLK – 1.	0x00000000

20.5.4 TMRx_INTSTS Register

Table 20-6 TMRx_INTSTS Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved	0
0	INTSTS	R/C	Timerx interrupt status register. When timer count down to 0, the bit will set 1. Write 1 to clear the bit.	0x0

20.5.5 PWMx_CTL Register

Table 20-7 PWMx_CTL Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:6	ID	R/W	PWM Timerx input clock divide control. 0:input clock 1/2 division 1:input clock 1/4 division 2:input clock 1/8 division 3:input clock 1/16 division	0x0
5:4	MC	R/W	PWM Timer control. 0:stop counting 1: count up: count up to CCR0, and from 0 to start it. 2: continue counting: count up to 0xFFFF, and from 0 to start it. 3: count up/down: count up to CCR0, and from CCR0 count down to 0.	0x0
3	TSEL	R/W	Clock source selected. 0:APB clock/128	0x0

			1:APB clock	
2	CLR	R/W	TAR clear register. When the bit set 1, TAR will clear 0. After TAR cleared 0, the bit also will be automatic cleared 0.	0x0
1	IE	R/W	PWM Timerx interrupt enable register	0x0
0	IFG	R/C	PWM Timerx interrupt status flag bit. Write 1 to clear the bit. Count up: from CCR0 to 0, the bit set 1. Continue counting: from 0xFFFF to 0, the bit set 1. Count up/ count down: from 0x0001 to 0, the bit set 1.	0x0

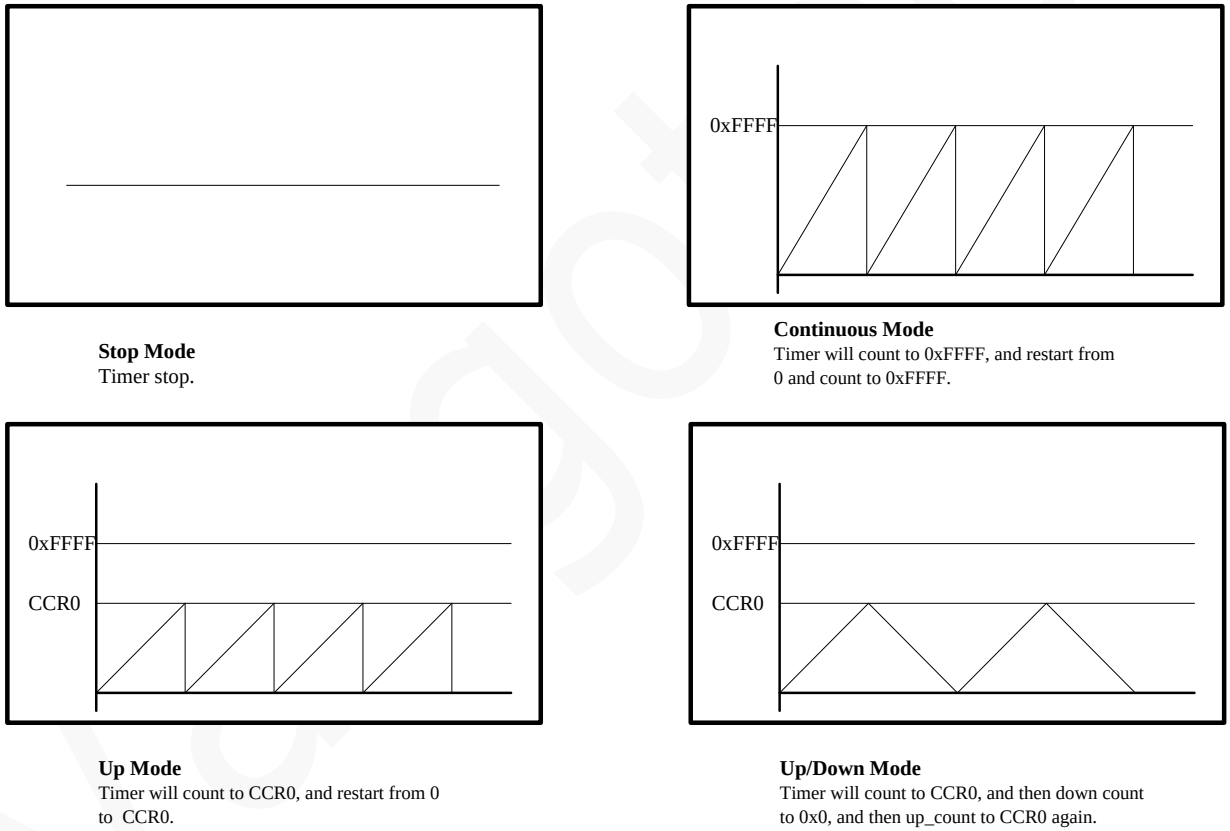


Figure 20-3 PWM Timer Mode

When MC is set to a non-zero value, the timer will start to work. When the PWM Timer working mode is up-counting mode and up/down-counting mode, if PWMx_CCR0 is set to 0, timer x will stop counting. If a non-zero value is written to PWMx_CCR0 again, the timer will restart counting.

In the up-counting mode, the value of CCR0 is changed during the counting period and the new value of CCR0 is greater than the current count value, the timer will count to the new CCR0 and then return to 0. If the new value of CCR0 is less than the current count value, the timer will reset the counter value to 0 after counting one beat and restart counting.

In the up/down counting mode, during the up counting period, if the value of CCR0 is changed during the counting period and the new value of CCR0 is greater than the current count value, the timer will count to the new CCR0 and then count down to 0. If the new CCR0 is less than the current count value, the timer will count down to 0 after counting one beat. During the down counting period, if the value of CCR0 is changed during the counting period, the timer will continuously complete the down counting process.

In continuous mode, user can dynamically set the value of CCR0~CCR2 to control the output frequency. The figure below shows an example of this application.

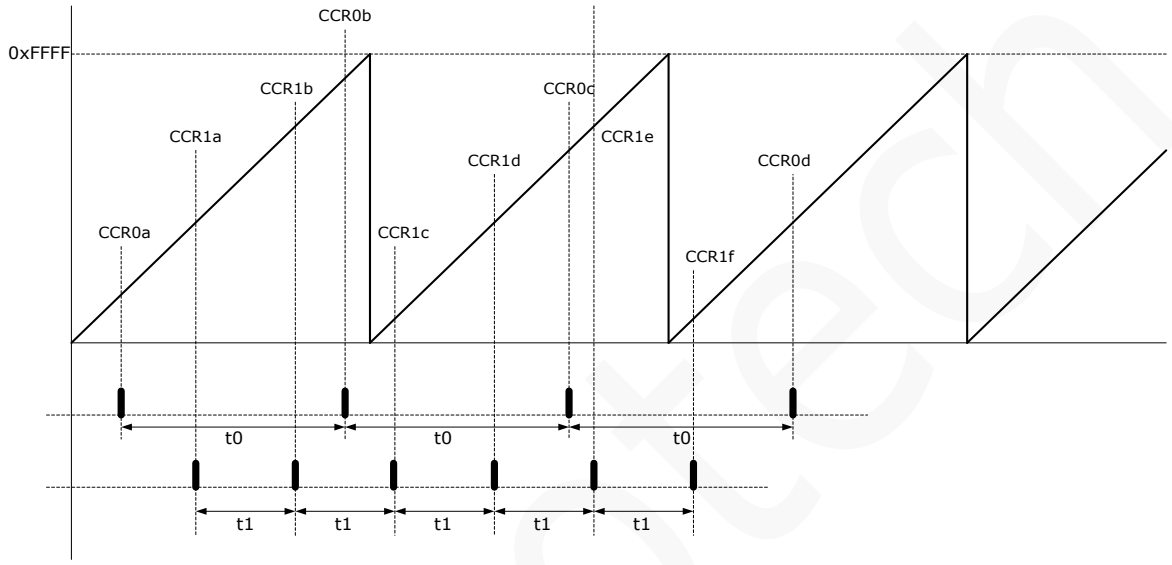


Figure 20-4 Continue Mode

In the figure above, CCR0a and CCR1a are the values of CCR0 and CCR1 at time Ta0 and Ta1, respectively, and CCR0b and CCR1b are the values of CCR0 and CCR1 at time Tb0 and Tb1 (Tb0=Ta0+t0, Tb1=Ta1+t1).

The figure above shows that in the continuous mode, user can set CCIFG (bit 0 of CCTLx) and CCIE (bit 4 of CCTLx), and set CCR0 and CCR1, then an interrupt signal can be generated when TAR=CCR0a or TAR=CCR1a. When TAR=CCR0b or TAR=CCR1b, another interrupt with a different cycle can be generated. T0 and T1 are completely independent, so a PWM timer can set up to 3 completely independent interrupts. In this mode, when the timer counts from 0xFFFF to 0x0, the IFG flag will be set to 1.

20.5.6 PWMx_TAR Register

Table 20-8 PWMx_TAR Register

Bit	Name	Type	Contents	Default
31:0	TAR	R/W	PWM Timer0 real time counting register	0x00000000

20.5.7 PWMx_CCTLx Register

Table 20-9 PWMx_CCTLx Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:14	CM	R/W	Capture edge selected 0:prohibit the capture function 1:rising-edge capture 2:falling-edge capture 3:both-edge capture	0x0
13:11	-	-	Reserved	0
10	SCCI	R	When TAR is equal to CCRx, the electricity level status of current channel input pins.	0x0
9	OUTEN	R/W	OUTx output enable control register 0:OUTx output disable 1:OUTx output enable	0x0
8	CAP	R/W	Capture/compare mode selection 0:Compare mode. It is used to produce PWM output. 1: Capture mode. It is used to measure or count the external signal frequency.	0x0
7:5	OUTMOD	R/W	Output mode selection 0:constant mode, the value of OUTx output OUT bit. 1: set mode. When TAR=CCRx(x=0~2), OUTx will set 1. 2:reverse/reset mode. When TAR=CCRx(x=1~2), OUTx reverse; when TAR=CCR0, OUTx reset is 0. This mode cannot be used in OUT0. 3: set/ reset mode. When TAR=CCRx(x=1~2),OUTx set 1; when TAR=CCR0, OUTx reset to 0. This mode cannot be used in OUT0. 4:Reverse mode. When TAR=CCRx(x=0~2), OUTx will be reversed. 5:Resert mode. When TAR=CCRx(x=0~2), OUTx will reset to 0.	0x0

			6:Reserved/ set mode. When TAR=CCRx(x=1~2), OUTx was reversed; when TAR=CCR0, OUTx will set 1. This mode cannot be used in OUT0. 7:reset / set mode. When TAR=CCRx(x=1~2), OUTx reset is 0; when TAR=CCR0, OUTxwill set 1. This mode cannot be used in OUT0.	
4	CCIE	R/W	Capture /compare interrupt enable register	0x0
3	-	-	Reserved	0
2	OUT	R/W	When OUTMOD set 0, the bit is used to control the output value of OUTx.	0x0
1	COV	R/C	Capture overflows flag bit. When CCIFG set 1 but happended another capture event, the bit will be set 1. Write 1 to clear the bit.	0x0
0	CCIFG	R/C	Under the capture mode, when capture event happened, the bit will set 1, and TAR will be locked in CCRx. Under the comparsion mode, when TAR=CCRx, the bit will be set 1. Write 1 to clear the bit.	0

The following table is PWM output under the counting up mode:

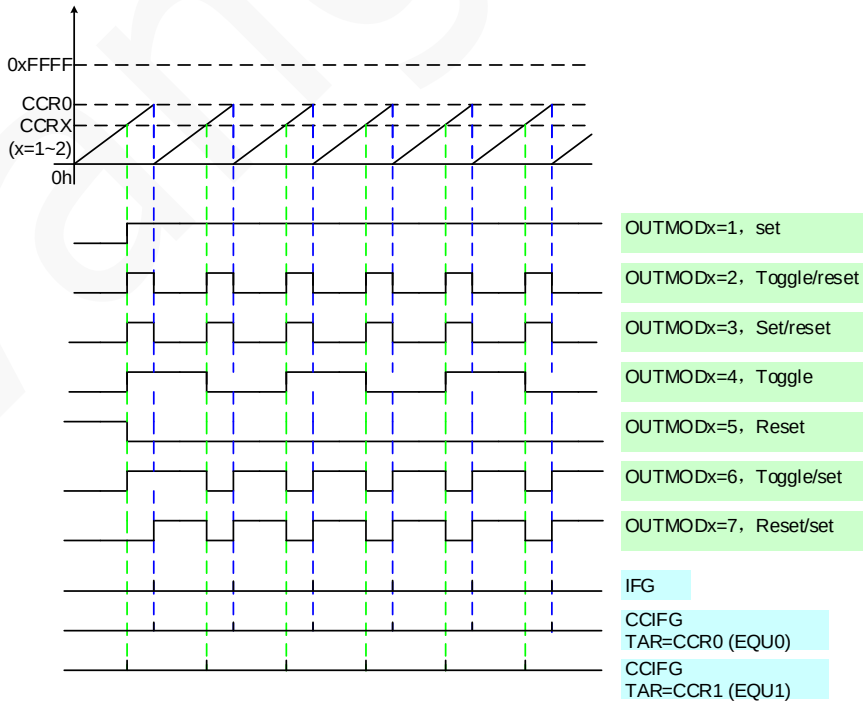


Figure 20-5 PWM Output Under the Count Up Mode

The following table is PWM output under continue counting mode:

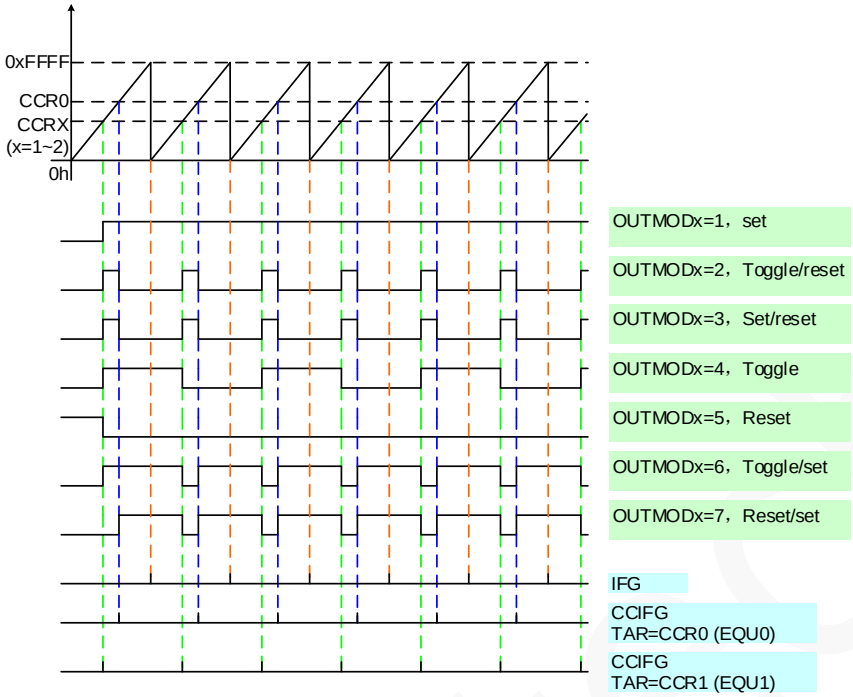


Figure 20-6 PWM Output Under Continue Counting Mode

The following table is PWM output under counting up/ counting down mode:

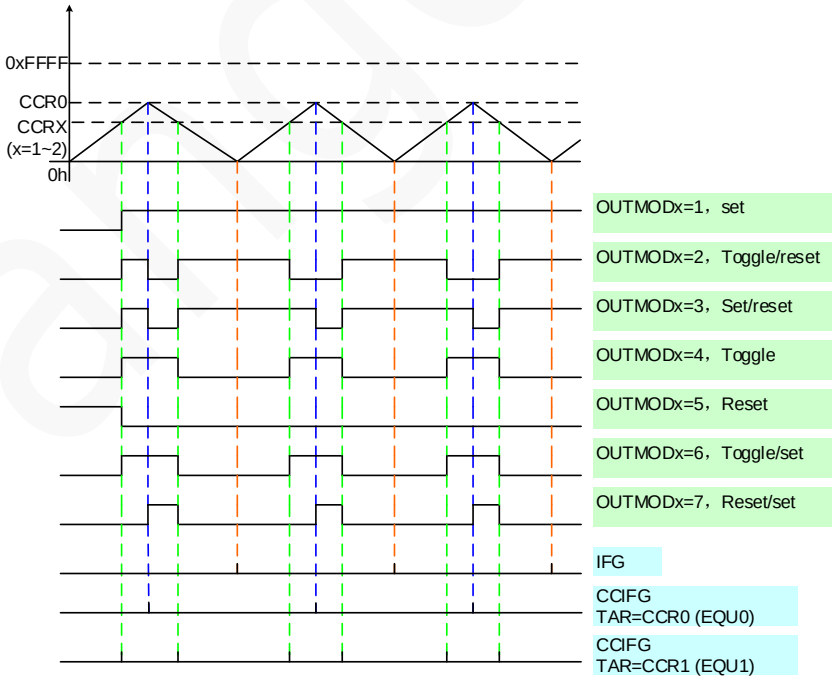


Figure 20-7 PWM Output Under Counting Up/ Counting Down Mode

20.5.8 PWMx_CCRx Register

Table 20-10 PWMx_CCRx Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	CCRx	R/W	Compare / capture data register Under capture mode, the captured TAR will store in the register. Under comparsion mode, the register is used to compare with TAR and generate PWM output.	0x0

20.5.9 PWM_O_SEL Register

Table 20-11 PWM_O_SEL Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:12	SEL3	R/W	External output pin selected register for PWM3. The same definition with SEL0.	0xD
11:8	SEL2	R/W	External output pin selected register for PWM2. The same definition with SEL0.	0xB
7:4	SEL1	R/W	External output pin selected register for PWM1. The same definition with SEL0.	0x5
3:0	SEL0	R/W	External output pin selected register for PWM0. 0x0: OUT0 from PWM0 0x1:OUT1 from PWM0 0x2:OUT2 from PWM0 0x4:OUT0 from PWM1 0x5:OUT1 from PWM1 0x6:OUT2 from PWM1 0x8:OUT0 from PWM2 0x9:OUT1 from PWM2 0xA:OUT2 from PWM2 0xC:OUT0 from PWM3 0xD:OUT1 from PWM3 0xE:OUT2 from PWM3	0x1

			Others: reserved	

20.5.10 PWM_I_SEL01 Register

Table 20-12 PWM_I_SEL01 Register

Bit	Name	Type	Contents	Default
31:22	-	-	Reserved	0
21:20	SEL12	R/W	The external input control of PWM1 channel 2 (IN2). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x3
19:18	SEL11	R/W	The external input control of PWM1 channel 1 (IN1). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x2
17:16	SEL10	R/W	The external output control of PWM1 channel 0 (IN0). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x1
15:6	-	-	Reserved	0
5:4	SEL02	R/W	The external input control of PWM0 channel 2 (IN2) 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x2
3:2	SEL01	R/W	The external input control of PWM0 channel 1 (IN1). 0:from PWM0 pins 1:from PWM1 pins	0x1

			2:from PWM2 pins 3:from PWM3 pins	
1:0	SEL00	R/W	The external input control of PWM0 channel 0 (IN0). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x0

20.5.11 PWM_I_SEL23 Register

Table 20-13 PWM_I_SEL23 Register

Bit	Name	Type	Contents	Default
31:22	-	-	Reserved	0
21:20	SEL32	R/W	The external input control of PWM3 channel 2 (IN2). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x1
19:18	SEL31	R/W	The external input control of PWM3 channel 1 (IN1). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x0
17:16	SEL30	R/W	The external input control of PWM3 channle 0 (IN0). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x3
15:6	-	-	Reserved	0
5:4	SEL22	R/W	The external input control of PWM2 channel 2 (IN2). 0:from PWM0 pins	0x0

			1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	
3:2	SEL21	R/W	The external input control of PWM2 channel 1 (IN1). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x3
1:0	SEL20	R/W	The external input control of PWM2 channel 0 (IN0). 0:from PWM0 pins 1:from PWM1 pins 2:from PWM2 pins 3:from PWM3 pins	0x2

21. LCD Controller

21.1 Introduction

LCD controller is used to to display contents on LCD panels. LCD controller supports 4/6/8 COM mode, at most 76. There are 2 packet buffers with automatic switching function. The settings of LCD controller will be reset after woke-up from deep-sleep mode. User should restore the settings after it woke-up from deep-sleep mode.

21.2 Features

--4/6/8 COM mode;

--Support at most 4 COM×76 SEG, 6 COM×74 SEG or 8 COM×72 SEG;

--Support 1/3 Bias or 1/4 Bias mode;

-- The LCD bias voltage is generated by an independent 3.3 V LDO, which is adjustable in steps of 50mV/LSB between 2.85~3.6V;

--Embedded shunt resistance circuit to generate LCD waveforms voltage;

--LCD scan frequency are generated by RTCCLK;

--Support 2 packet buffers, and support automatic switching function;

--Packet frequency is adjustable.

21.3 Functional Block Diagram

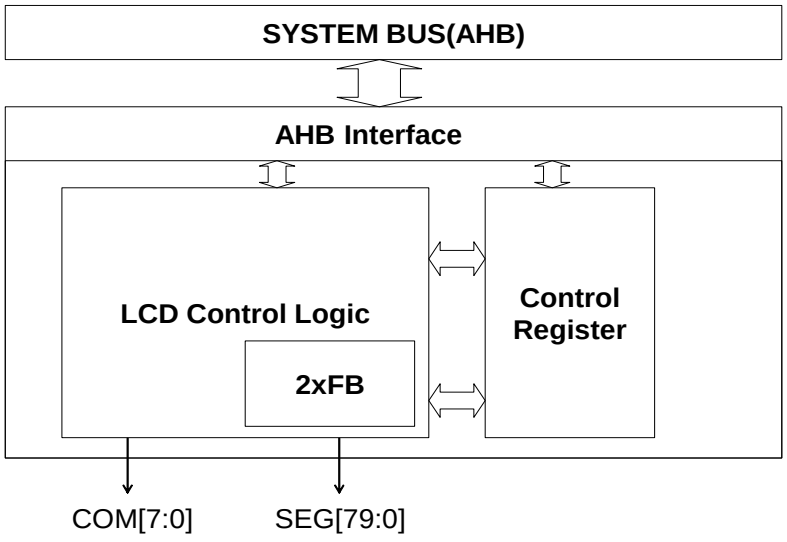


Figure 21-1 LCD Functional Block Diagram

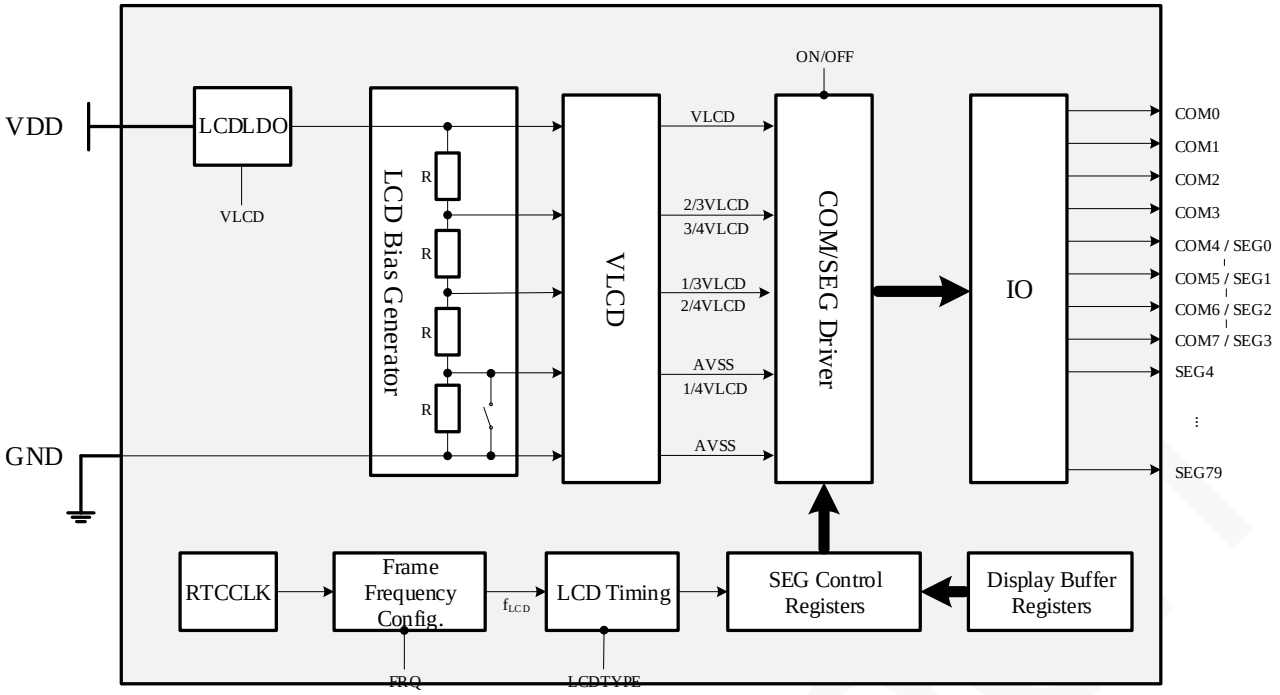


Figure 21-2 LCD Structure Diagram

21.4 LCD Time Sequence

LCD controller is used to display contents on LCD panels. LCD controller supports 4/6/8 COM mode, at most 76. There are 2 packet buffers with automatic switching function. The settings of LCD controller will be reset after woke-up from deep-sleep mode. User should restore the settings after it woke-up from deep-sleep mode.

21.5 LCD Waveforms Voltage

In V85XXP, the bias voltage of LCD driving circuit follows VDD, and passed internal shunt resistance circuit by independent AVCC to generate LCD bias voltage (VLCD) which is used to generate LCD driving waveforms.

21.6 LCD Working Current

User can change the control bit DRV in LCD_CTRL register, and configure each shunt resistance value in bias voltage circuit to change current size in order to adjust the brightness of LCD display. Under the default conditions, each shunt resistance value is 300kΩ.

21.7 LCD Driving Waveforms

There are 4 series resistors in the LCD bias voltage generating circuit, which can be configured as 1/3 Bias mode or 1/4 Bias mode. User can configure the LCDBMOD bit (bit0 of ANA_REG6) to enable or disable a resistor, thereby configure the LCD to be 1/3 bias or 1/4 bias mode.

The following figure is LCD driving waveform (1/4 duty, 1/3 bias):

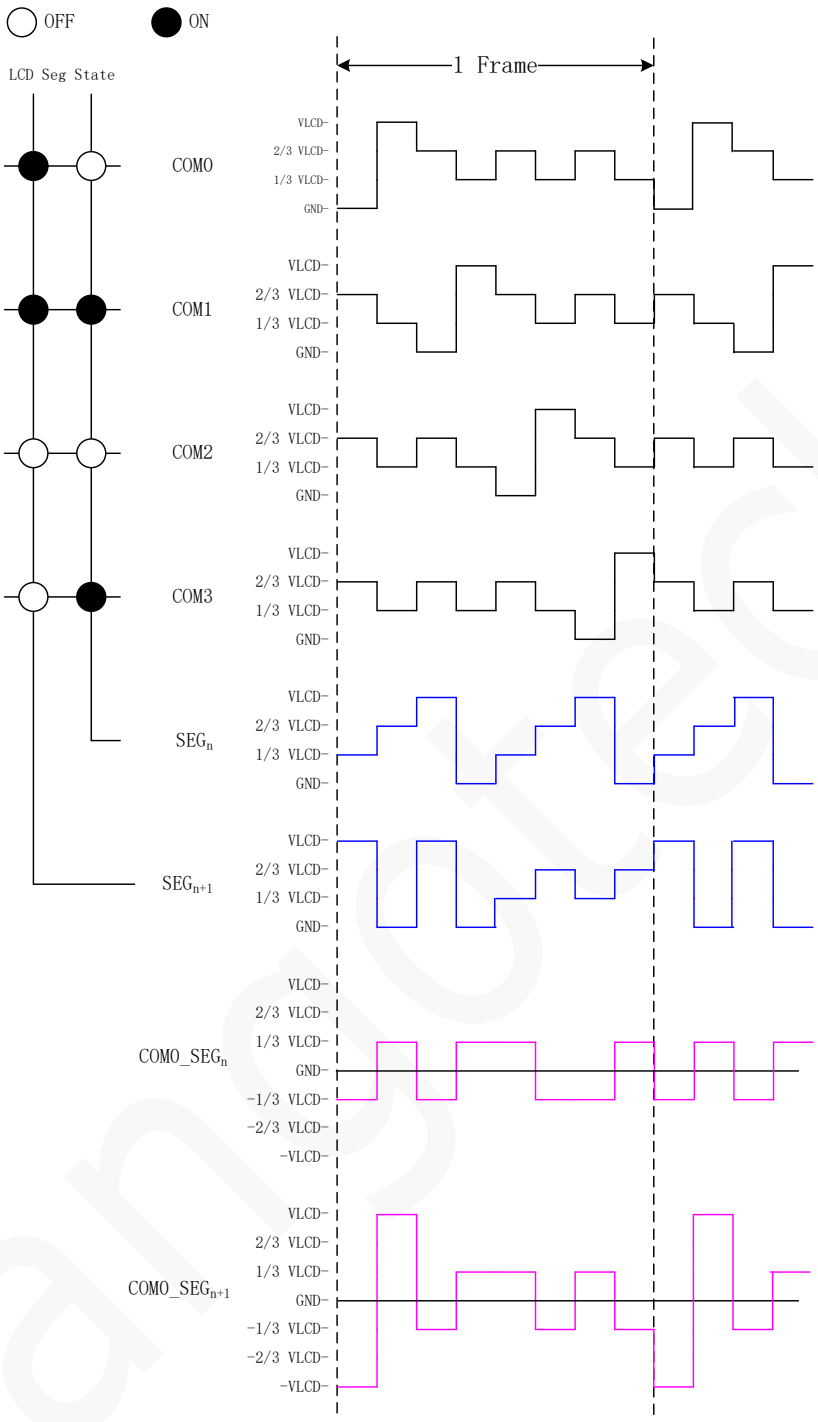


Figure 21-3 LCD Waveforms [1/4 duty, 1/3 bias]

The following figure is LCD driving waveform (1/6 duty, 1/3 bias):

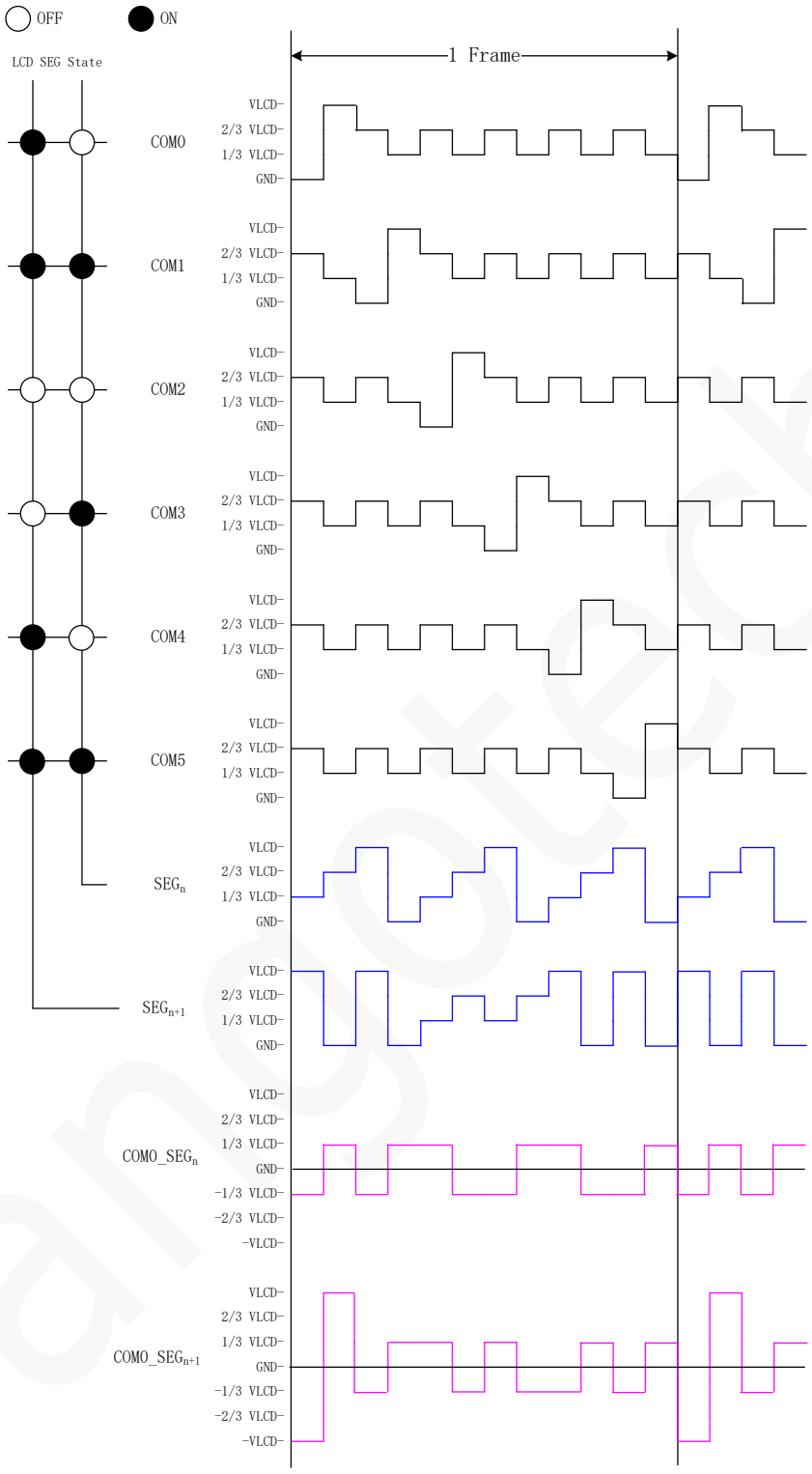


Figure 21-4 LCD Waveforms [1/6 Duty, 1/3 Bias]

The following figure is LCD driving waveform (1/8 duty, 1/3 bias):

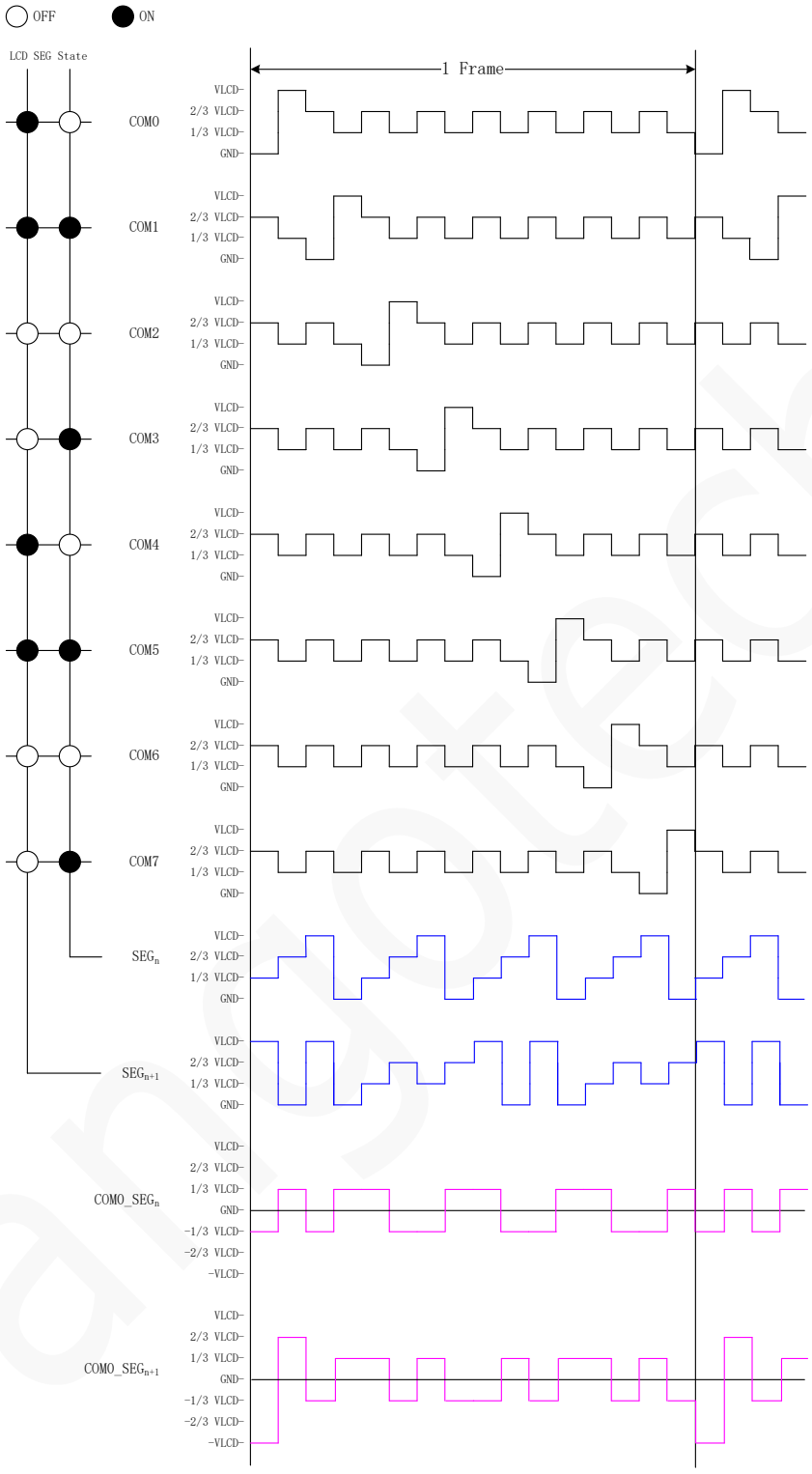


Figure 21-5 LCD Waveforms [1/8 Duty, 1/3 Bias]

The following figure is LCD driving waveform (1/8 duty, 1/4 bias):

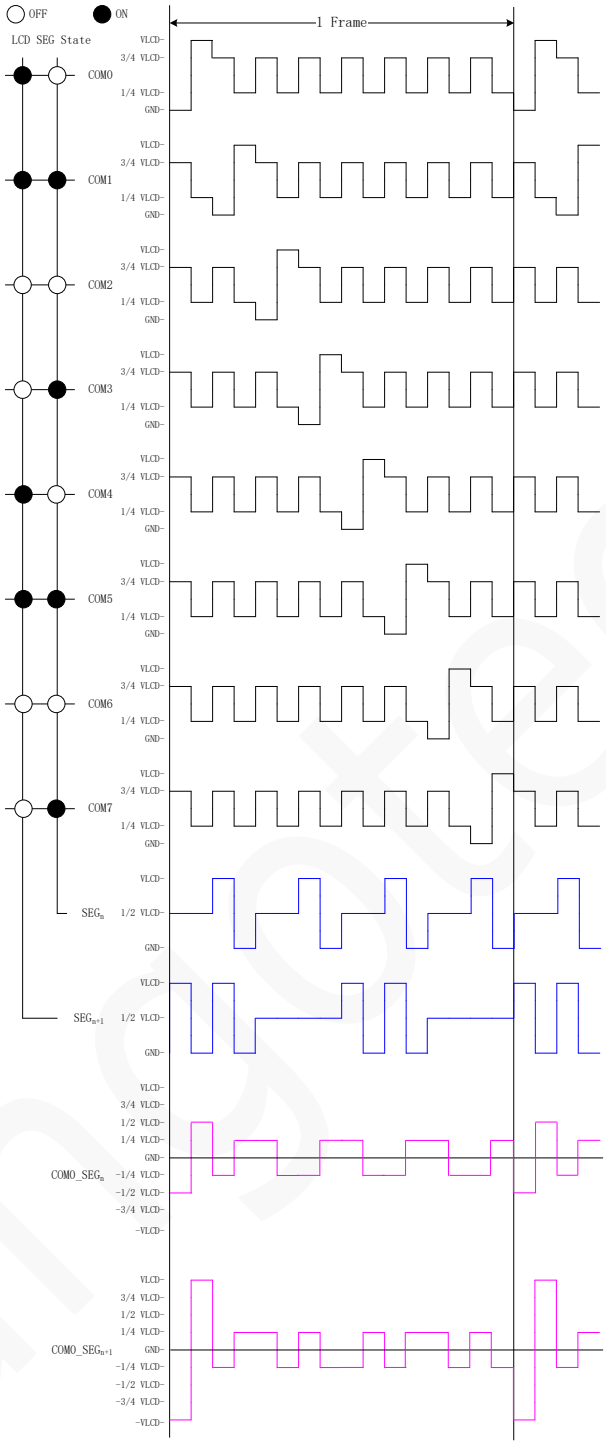


Figure 21-6 LCD Waveforms [1/8 Duty, 1/4 Bias]

21.8 Register Address

Table 21-1 ANA is related to LCD (ANA Base Address:0x40014200)

Name	Type	Address	Contents	Default
ANA_REG6	R/W	0x0018	ANA register 6	0x00

Table 21-2 LCD (LCD Base Address:0x40002000)

Name	Type	Address	Contents	Default

LCD_FB00	R/W	0x0000	LCD packet buffer 0 register	--
LCD_FB01	R/W	0x0004	LCD packet buffer 1 register	--
LCD_FB02	R/W	0x0008	LCD packet buffer 2 register	--
LCD_FB03	R/W	0x000C	LCD packet buffer 3 register	--
LCD_FB04	R/W	0x0010	LCD packet buffer 4 register	--
LCD_FB05	R/W	0x0014	LCD packet buffer 5 register	--
LCD_FB06	R/W	0x0018	LCD packet buffer 6 register	--
LCD_FB07	R/W	0x001C	LCD packet buffer 7 register	--
LCD_FB08	R/W	0x0020	LCD packet buffer 8 register	--
LCD_FB09	R/W	0x0024	LCD packet buffer 9 register	--
LCD_FB0A	R/W	0x0028	LCD packet buffer 10 register	--
LCD_FB0B	R/W	0x002C	LCD packet buffer 11 register	--
LCD_FB0C	R/W	0x0030	LCD packet buffer 12 register	--
LCD_FB0D	R/W	0x0034	LCD packet buffer 13 register	--
LCD_FB0E	R/W	0x0038	LCD packet buffer 14 register	--
LCD_FB0F	R/W	0x003C	LCD packet buffer 15 register	--
LCD_FB10	R/W	0x0040	LCD packet buffer 16 register	--
LCD_FB11	R/W	0x0044	LCD packet buffer 17 register	--
LCD_FB12	R/W	0x0048	LCD packet buffer 18 register	--
LCD_FB13	R/W	0x004C	LCD packet buffer 19 register	--
LCD_FB14	R/W	0x0050	LCD packet buffer 20 register	--
LCD_FB15	R/W	0x0054	LCD packet buffer 21 register	--
LCD_FB16	R/W	0x0058	LCD packet buffer 22 register	--
LCD_FB17	R/W	0x005C	LCD packet buffer 23 register	--
LCD_FB18	R/W	0x0060	LCD packet buffer 24 register	--
LCD_FB19	R/W	0x0064	LCD packet buffer 25 register	--
LCD_FB1A	R/W	0x0068	LCD packet buffer 26 register	--
LCD_FB1B	R/W	0x006C	LCD packet buffer 27 register	--
LCD_FB1C	R/W	0x0070	LCD packet buffer 28 register	--
LCD_FB1D	R/W	0x0074	LCD packet buffer 29 register	--

LCD_FB1E	R/W	0x0078	LCD packet buffer 30 register	--
LCD_FB1F	R/W	0x007C	LCD packet buffer 31 register	--
LCD_FB20	R/W	0x0080	LCD packet buffer 32 register	--
LCD_FB21	R/W	0x0084	LCD packet buffer 33 register	--
LCD_FB22	R/W	0x0088	LCD packet buffer 34 register	--
LCD_FB23	R/W	0x008C	LCD packet buffer 35 register	--
LCD_FB24	R/W	0x0090	LCD packet buffer 36 register	--
LCD_FB25	R/W	0x0094	LCD packet buffer 37 register	--
LCD_FB26	R/W	0x0098	LCD packet buffer 38 register	--
LCD_FB27	R/W	0x009C	LCD packet buffer 39 register	--
LCD_CTRL	R/W	0x0100	LCD control register	0x00
LCD_CTRL2	R/W	0x0104	LCD control register 2	0x0000
LCD_SEGCTRL0	R/W	0x0108	LCDSEG enable control register 0	0x00000000
LCD_SEGCTRL1	R/W	0x010C	LCDSEG enable control register 1	0x00000000
LCD_SEGCTRL2	R/W	0x0110	LCDSEG enable control register 2	0x00000000

21.9 Register Definition

21.9.1 LCD_FBx Register

Table 21-3 LCD_FBx Register

Bit	Name	Type	Contents	Default
31:0	DATAx	R/W	Each bit represents the data in list. The detail information about data list under the different mode, please refer to Table 21-4 These register can read or write the byte, so user can use CPU or DMA to read or write these registers.	--

LCD_FB00~LCD_FB13 is packet buffer A.

LCD_FB14~LCD_FB27 is packet buffer B.

The following table shows packet buffer A. If FBMODE is selected 1, then packet buffer B display the same data with packet buffer B.

Table 21-4 LCD_FBx The Data List of Register

Register	Dat bit

	31:24	23:16	15:8	7:0
LCD_FB00	SEG3 corresponding COM[7:0]	SEG2 corresponding COM[7:0]	SEG1 corresponding COM[7:0]	SEG0 corresponding COM[7:0]
LCD_FB01	SEG7 corresponding COM[7:0]	SEG6 corresponding COM[7:0]	SEG5 corresponding COM[7:0]	SEG4 corresponding COM[7:0]
…..				
LCD_FB13	SEG79 corresponding COM[7:0]	SEG78 correspoinding COM[7:0]	SEG77 corresponding COM[7:0]	SEG76 corresponding COM[7:0]

When choose 4/6 COM mode, the higher bits COM will be abandon. Therefore, data list format should be the same to 8COM mode.

21.9.2 LCD_CTRL Register

Table 21-5 LCD_CTRL Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7	EN	R/W	LCD enable register 0:disable 1:enable User must set 1.	0x0
6	-	-	Reserved	0
5:4	TYPE	R/W	LCD mode control register 0:4 COM mode 1:6 COM mode 2:8 COM mode 3:reserved	0x0
3:2	DRV	R/W	LCD driving resistance control register 0:300k ohm 1:600k ohm 2:150k ohm	0x0

			3:200 kohm	
1:0	FRQ	R/W	LCD frequency scan 0:64Hz 1:128Hz 2:256Hz 3:512Hz Here represents the scan rate of each COM. Therefore, if there are 4 COMs in total, the packet speed = the value divided by 4.	0x0

Note: When switching the COM type, please enable the LCD controller (bit 7 of the LCD_CTRL register)first, and then wait for a delay to ensure the completion of the current frame transmission. The delay is related to the current frame rate (bit 1: 0, bit 7 of the LCD_CTRL register).

For example: the current scan rate of LCD is 64Hz, switch the COM type from 4COM to 6COM, the delay time is calculated as follows:

TDelay=1/(64/4)=62.5ms

21.9.3 LCD_CTRL2 Register

Table 21-6 LCD_CTRL2 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:8	SWPR	R/W	Frame buffer switching cycle. The switching cycle formula as below: 0.5 seconds* (SWPR+1)	0x0
7:6	FBMODE	R/W	The control register for LCD frame buffer switching 0:always display frame buffer A 1:Switch between frame buffer A and frame buffer B 2:Switch between frame buffer A and space 3:reserved	0x0
5	-	-	Reserved	0
4	BKFILL	R/W	Blank period filled value. This register controls the filled value during the blank period.	0x0

3:0	-	-	Reserved	0

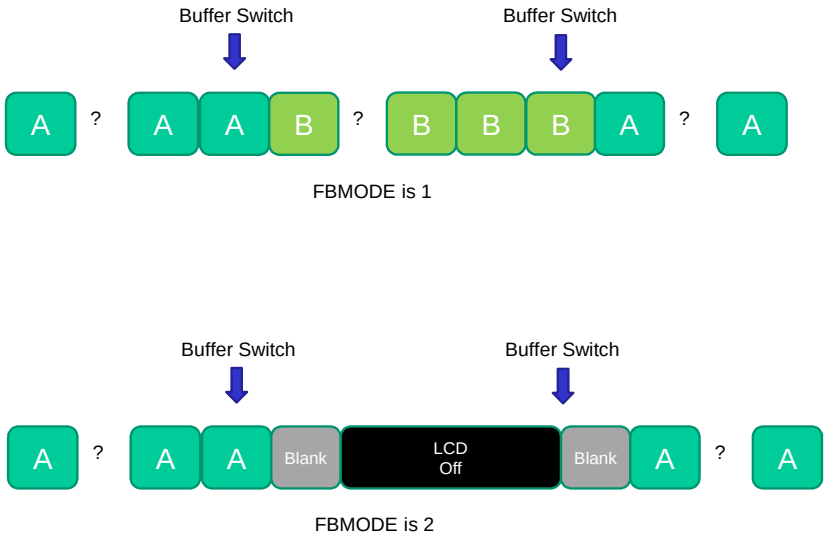


Figure 21-7 Packet Buffer Operation Mode in Different FBMODE

21.9.4 LCD_SEGCTRL0 Register

Table 21-7 LCD_SEGCTRL0 Register

Bit	Name	Type	Contents	Default
31:0	SEGCTRL	R/W	Each bit controls LCD signal enable of SEG0~SEG31. Bit 0:enable control of SEG0 Bit 1:enable control of SEG1 .... Bit 31:enable control of SEG31 0:disable SEG output 1:enable SEG output	0x00000000

21.9.5 LCD_SEGCTRL1 Register

Table 21-8 LCD_SEGCTRL1 Register

Bit	Name	Type	Contents	Default
31:0	SEGCTRL	R/W	Each bit controls LCD signal enable of SEG32~SEG63. Bit 0:enable control of SEG32	0x00000000

			Bit 1:enable control of SEG33 …. Bit 31:enable control of SEG63 0:disable SEG output 1:enable SEG output	

21.9.6 LCD_SEGCTRL2 Register

Table 21-9 LCD_SEGCTRL2 Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	SEGCTRL	R/W	Each bit controls LCD signal enable of SEG64~SEG79 Bit 0:enable control of SEG64 Bit 1:enable control of SEG65 ... Bit 15:enable control of SEG79 0:disable SEG output 1:enable SEG output	0x0000

21.9.7 ANA_REG6 Register

Table 21-10 ANA_REG6 Register

Bit	Name	Function	Notes
0	LCD_BMODE	LCD bias mode selection	0:1/3 Bias 1:1/4 Bias
4:1	VLCD[3:0]	LCD driving voltage	When VLCD=0: Default When VLCD=0~6, the adjustment range =+50mV*VLCD. When VLCD=7~15, the adjustment range =-50mV*(VLCD-6).

For each COM and SEG, in order to ensure the normal operation of the LCD, user should set the corresponding IO to prohibit the input and output before enabling the LCD function of the corresponding pin.

22. SPI Controller

22.1 Introduction

V85XXP intergrated 3 serial peripheral interface (SPI) controllers in oder to communicate with other devices and components. The setting of SPI controller will be reset after woke-up from sleep or deep-sleep mode. User should restore the settings by manual after it woke-up from sleep or deep-sleep mode. SPICLK is supported by SPI Master mode: APBCLK/2/4/8/16/32/64/128. The biggest SPICLK of SPI Slave mode is APBCLK/2.

22.2 Features

--Support master and slave mode;

--Support single byte and continue byte transmission;

--Support overflows error flag bit;

--Support transmit/ receive interrupt request;

--Programmable phase and polarity;

--Selectable data sampling time (the end or central of clock cycle);

--Programmable CLK frequency under Master mode: APBClock/2/4/8/16/32/64/128 ;

--Embedded 8x 8-bit FIFOs on the transmit and receive direction, and programmable for 2 FIFOs interrupt tigger threshold.

22.3 Functional Block Diagram

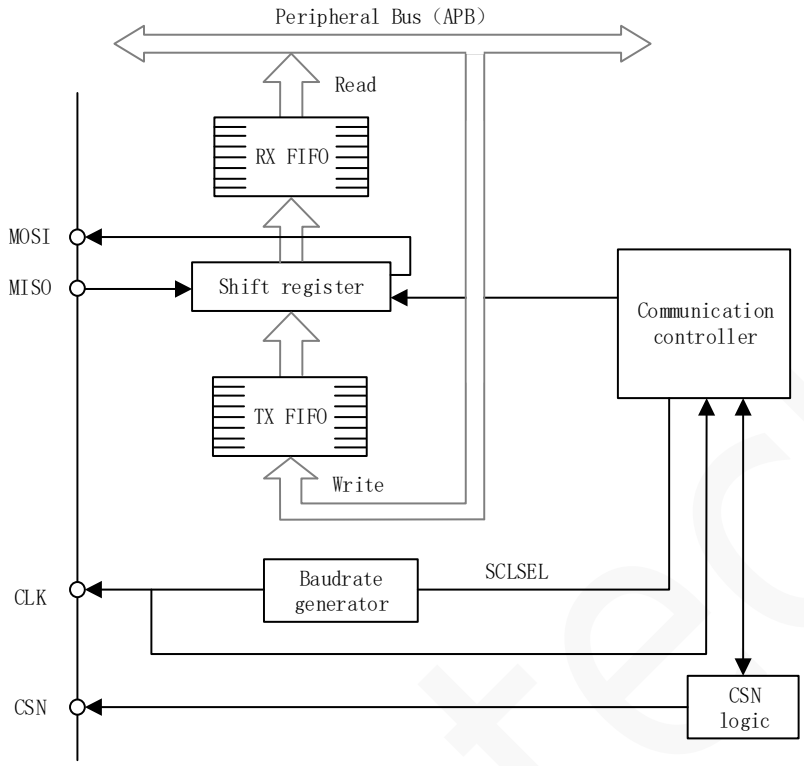


Figure 22-1 SPI Functional Block Diagram

Normally, SPI is connected to external devices through 4 pins.

MOSI: Master device output/slave device input. Generally, this pin is used for data transmission in master mode and data reception in slave mode.

MISO: Master input/slave output. Generally, this pin is used for data reception in master mode and data transmission in slave mode.

CLK: SPI serial clock output pin, the clock is controlled by the master.

CSN: Slave chip select pin. According to the settings of SPI and CSN, this pin can be used to: select a slave to communicate and synchronize data frames.

Note: The maximum SPICLK clock supported by SPI slave mode is APBCLK/2.

22.4 Register Address

Table 22-1 SPI1 (SPI1 Base Address:0x40011000)

Name	Type	Address	Contents	Default
SPI1_CTRL	R/W	0x0000	SPI1 control register	0x0000
SPI1_TXSTS	R/W	0x0004	SPI1 transmit status register	0x8200
SPI1_TXDAT	R/W	0x0008	SPI1 transmit FIFO register	--
SPI1_RXSTS	R/W	0x000C	SPI1 receive status register	0x0000

SPI1_RXDAT	R/W	0x0010	SPI1 receive FIFO register	--
SPI1_MISC	R/W	0x0014	SPI1 Misc control register	0x0003

Table 22-2 SPI2 (SPI2 Base Address:0x40015800)

Name	Type	Address	Contents	Default
SPI2_CTRL	R/W	0x0000	SPI2 control register	0x0000
SPI2_TXSTS	R/W	0x0004	SPI2 transmit status register	0x8200
SPI2_TXDAT	R/W	0x0008	SPI2 transmit FIFO register	--
SPI2_RXSTS	R/W	0x000C	SPI2 receive status - register	0x0000
SPI2_RXDAT	R/W	0x0010	SPI2 receive FIFO register	--
SPI2_MISC	R/W	0x0014	SPI2 Misc control register	0x0003

Table 22-3 SPI3 (SPI3 Base Address:0x40016000)

Name	Type	Address	Contents	Default
SPI3_CTRL	R/W	0x0000	SPI3 control register	0x0000
SPI3_TXSTS	R/W	0x0004	SPI3 transmit status register	0x8200
SPI3_TXDAT	R/W	0x0008	SPI3 transmit FIFO register	--
SPI3_RXSTS	R/W	0x000C	SPI3 receive status register	0x0000
SPI3_RXDAT	R/W	0x0010	SPI3 receive FIFO register	--
SPI3_MISC	R/W	0x0014	SPI3 Misc control register	0x0003

22.5 Register Definition

22.5.1 SPIx_CTRL Register

SPIx_CTRL register is used to control SPIx behaviors.

Table 22-4 SPIx_CTRL Register

Name	Type	Address	Contents	Default
15	EN	R/W	If the bit set 1, SPICLK, SPIMISO, and SPIMOSI pins cannot be the normal GPIOs; therefore, any input or output for them will be invalid. For SPI1 engine, if the bit set 1, IOB[12:10] will be SPI1 interface. For SPI2 engine, if the bit set 1, IOB[3:1] will be SPI2 interface.	0x0

			For SPI3 engine, if the bit set 1, IOB[7:5] will be SPI3 interface. SPICSN pins are controlled by CSGPIO. 0:disable SPI function 1:enable SPI function	
14:13	-	-	Reserved	0
12	LSBF	R/W	SPI LSB control Data bit transmit order control register 0:high-bit transmit first (MSB) 1:low-bit transmit first (LSB)	
11	RST	W	SPI software reset. If the bit set 1, SPI controller and FIFO pointer will return to initial status. 0:invalid 1:reset SPI controller	0x0
10	CSGPIO	R/W	SPICSN pins are controlled by GPIOs or H/W. Master Mode: 0:SPICSN pins are controlled by H/W. 1:SPICSN pins are controlled by software GPIOs. Slave Mode: 0:SPICSN pins are controlled by Master. 1:SPICSN pins are logic 0.	0x0
9	SWAP	R/W	SPI MISO/MOSI pins switching control register 0:not switch MISO/MOSI 1: switch MISO/MOSI	0x0
8	MOD	R/W	SPI mode select register 0:Master mode 1:Slave mode	0x0
7:6	-	-	Reserved	0
5	SCKPHA	R/W	SPI clock phase. Please refer to application note.	0x0
4	SCKPOL	R/W	SPI clock polarity. Please refer to application note.	0x0
3	-	-	Reserved	0

2:0	SCKSEL	R/W	Clock selected in Master mode. 000:APBCLK/2 001:APBCLK/4 010:APBCLK/8 011:APBCLK/16 100:APBCLK/32 101:APBCLK/64 110:APBCLK/128 111:reserved	0x0

22.5.2 SPIx_TXSTS Register

SPIx_TXSTS register controls SPIx transmit to FIFO, and the related interruptions.

Table 22-5 SPIx_TXSTS Register

Name	Type	Address	Contents	Default
31:16	-	-	Reserved	0
15	TXIF	R/C	SPI transmit interrupt flag bit. When the number of data in transmitting FIFO is lower than user setting value, the bit set 1. If SAMART value is 1 in SPI_MISC register, the number of data in transmitting FIFO is higher than user setting value, the bit will be cleared 0; otherwise, we should write 1 in the bit to clear it. Read 0:did not happen Read 1:happened Write 0:invalid Write 1:clear the bit	0x1
14	TXIEN	R/W	SPI transmit interrupt enable. If the bit set 1, and SPI interrupt happended, hardware will transmit a interrupt to CPU. If the bit clear 0, the interrupt will be blocked. 0:disable to transmit interrupt 1:enable to transmit interrupt	0x0

13:10	-	-	Reserved	0
9	TXEMPTY	R	Transmit FIFO empty flag bit. When transmit FIFO is empty, the bit will be set 1 by hardware. When transmit FIFO is not empty, the bit will be cleared by hardware. 0:transmit FIFO is not empty 1:transmit FIFO is empty	0x1
8	TXFUR	R	Slave transmit FIFO empty flag bit during operating. When transmit FIFO is empty, and SPI Master request more data, the bit will be set 1. The bit only set 1 in SPI Slave mode.	0x0
7	-	-	Reserved	0
6:4	TXFLEV	R/W	Transmit FIFO interrupt trigger threshold. The register is used to indicate that when interrupt happened, the number of bytes stored in FIFO. The setting value is smaller, the interrupt trigger will be lesser. So, we can write more datas in a interrupt. 000:the data in FIFO<1, can write 8 data in. 001:the data in FIFO<2, can write 7 data in. 010:the data in FIFO<3, can write 6 data in. 011:the data in FIFO<4, can write 5 data in. 100:the data in FIFO<5, can write 4 data in. 101:the data in FIFO<6, can write 3 data in. 110:the data in FIFO<7, can write 2 data in. 111:the data in FIFO<8, can write 1 data in.	0x0
3	DMATXDONE	R/C	Transmit completed flag bit. When transmitted data batches via DMA, it will automatic set 1 after it completed. User must wait DMA transmitting completed, then can read this flag bit. Write 1 to clear the bit.	0x0
2:0	TXFFLAG	R	The number of transmit data in FIFO. The register is used to indicate the number of data number in FIFO. 0000:There is not any data in FIFO, or there are 8	0x0

			bytes in FIFO. 0001:1 byte in FIFO 0010:2 bytes in FIFO 0011:3 bytes in FIFO 0100:4 bytes in FIFO 0101:5 bytes in FIFO 0110:6 bytes in FIFO 0111:7 bytes in FIFO	

22.5.3 SPIx_TXDAT Register

SPI_TXDAT register is used to write data to FIFO, and move it to external Host or Slave.

Table 22-6 SPIx_TXDAT Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	TXD	W	Write data to transmit FIFO	--

22.5.4 SPIx_RXSTS Register

SPI_RXSTS register is used to control SPI receiving FIFO and the related interruption.

Table 22-7 SPIx_RXSTS Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15	RXIF	R/C	SPI receive interrupt flag bit. When the number of received data is higher than user setting values, the bit will be set 1 by hardware. If SMART set 1 in SPI_MISC register, only if the data in FIFO is lower than interrupt trigger threshold, the bit will be cleared; if SMART value be set 0, we should write 1 in the bit to clear it. Read 0:did not happen Read 1:happened Write 0:invalid Write 1:clear the bit	0x0

14	RXIEN	R/W	SPI receive interrupt enable If the bit set 1, and SPI interrupt happended, hardeare will transmit a interrupt to CPU. If the bit clear 0, the interrupt will be blocked. 0:disable receive interrupt 1:enable receive interrupt	0x0
13:10	-	-	Reserved	0
9	RXFULL	R	FIFO full register When we received FIFO is already full, the bit will be set 1 by hardware. When we received FIFO is not full, the bit will be cleared by hardware. 0:FIFO is not full 1:FIFO is already full	0x0
8	RXFOV	R	FIFO overflows register When FIFO is already full and received more data in SPI data bus, the bit set 1. Write 1 in SPIRXIF bit to clear the bit.	0x0
7	-	-	Reserved	0
6:4	RXFLEV	R/W	The interrupt trigger threshold of the receive FIFO. This register indicates how many bytes of data are in the receive FIFO when an interrupt occurs. The larger the setting value, the fewer interrupt triggers, so more data can be read in one interrupt. 000:data in FIFO>=1, allow 1 data reading 001:data in FIFO>=2, allow 2 data reading 010:data in FIFO>=3, allow 3 data reading 011:data in FIFO>=4, allow 4 data reading 100:data in FIFO>=5, allow 5 data reading 101:data in FIFO>=6, allow 6 data reading 110:data in FIFO>=7, allow 7 data reading 111:data in FIFO>=8, allow 8 data reading	0x0
3	-	-	Reserved	0

2:0	RXFFLAG	R	The number of FIFO data received The register represents the number of FIFO data received. 0000:There is no data in FIFO, or there are 8 bytes in FIFO. 0001:There is a byte in FIFO. 0010:There are 2 bytes in FIFO. 0011:There are 3 bytes in FIFO. 0100:There are 4 bytes in FIFO. 0101:There are 5 bytes in FIFO. 0110:There are 6 bytes in FIFO. 0111:There ae 7 bytes in FIFO.	0x0

22.5.5 SPIx_RXDAT Register

SPI_RXDAT register is used to SPI receiver reads data in receiving FIFO.

Table 22-8 SPIx_RXDAT Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	RXD	R	Read data from SPI receive FIFO.	--

22.5.6 SPIx_MISC Register

SPI_MISC register is used to configure special functions for SPI receive/ transmist function.

Table 22-9 SPIx_MISC Register

Bit	Name	Type	Contents	Default
31:10	-	-	Reserved	0
9	OVER	R/W	SPI FIFO overflows control. The register is used to control when TX/RX FIFO is already full, data will be re-writed or skipped. 0: Further write operations to the full FIFO will be skipped. 1: write in full FIFO, and it will cover the original data in FIFO.	0x0

8	SMART	R/W	SPI FIFO SMART mode register If the bit set 1, user no needs to clear transmit/ receive interrupt flag bit by manual when FIFO status reached the interrupt level. User only needs to write data in FIFO or read data in FIFO, adnt the interrupt flag bit will be cleared 0. When selects DMA mode, we must set 1 to the bit to ensure DMA operation correctly. 0:normal interrupt to clear 0 1:smart interrupt to clear 0	0x0
7:5	-	-	Reserved	0
4	BSY	R	The flag bit for SPI controller is busy. The bit is used to indicate that whether SPI controller is busy. 0:idle 1:busy	0x0
3	RFF	R	Flag bit for SPI receive FIFO is full. The bit indicates that whether SPI received data from FIFO is full. 0:receive FIFO is not full 1:receive FIFO is full	0x0
2	RNE	R	Flag bit for receive FIFO is not empty. The bit shows that whether there is data to receive FIFO. 0:Receive FIFO is empty. 1:Receive FIFO is not empty.	0x0
1	TNF	R	Flag bit for transmit FIFO is not full. The bit shows transmit FIFO whether is not full. 0:Transmit FIFO is full. 1:Transmit FIFO is not full.	0x1
0	TFE	R	Flag bit for transmit FIFO is empty. The bit shows transmit FIFO whether is empty. 0:Transmit FIFO is not empty.	0x1

			1:Transmit FIFO is empty.	

22.6 Application Note

22.6.1 Host Mode

Under Host mode, SPICLK is generated by V85XXP. SCKPHA and SCKPOL two control bits are separated to control CLK phase and polarity of the clock. Write a data in SPI_TXDAT to start the data transmission. As long as there is data in FIFO, the next data will be sent automatically after one byte of data is sent.

When SPI sends data, it moves the data from MSB to LSB or from LSB to MSB according to the LSBF control bit. It takes 8 SPICLK cycles to shift out 8 bits of data. At the same time, data is also shifted in through the output pins of the slave device. When the transmit FIFO level is lower than the interrupt trigger level, the SPITXIF flag bit will be set 1. And, if the SPITXIEN bit is 1, an SPI transmission interrupt will be generated. When the receive FIFO level is higher than the interrupt trigger level, the SPIRXIF flag bit will be set 1. Meanwhile, if the SPIRXIEN bit is 1, an SPI reception interrupt will be generated. SPI data can be read from the SPI_RXDAT register.

The following figure shows different timing schemes under different operation type configurations in SPI master mode. (The polarity control bit is equal to 1 or 0, and the phase control bit is equal to 1 or 0). The slave mode also supports polarity control and phase control.

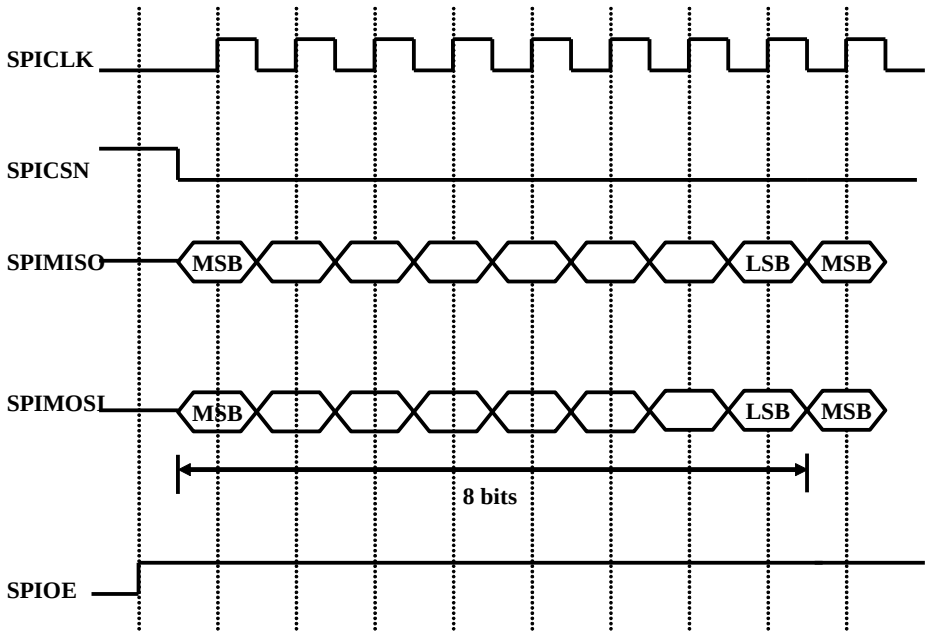


Figure 22-2 Host Mode, SPO=0, SPH=0

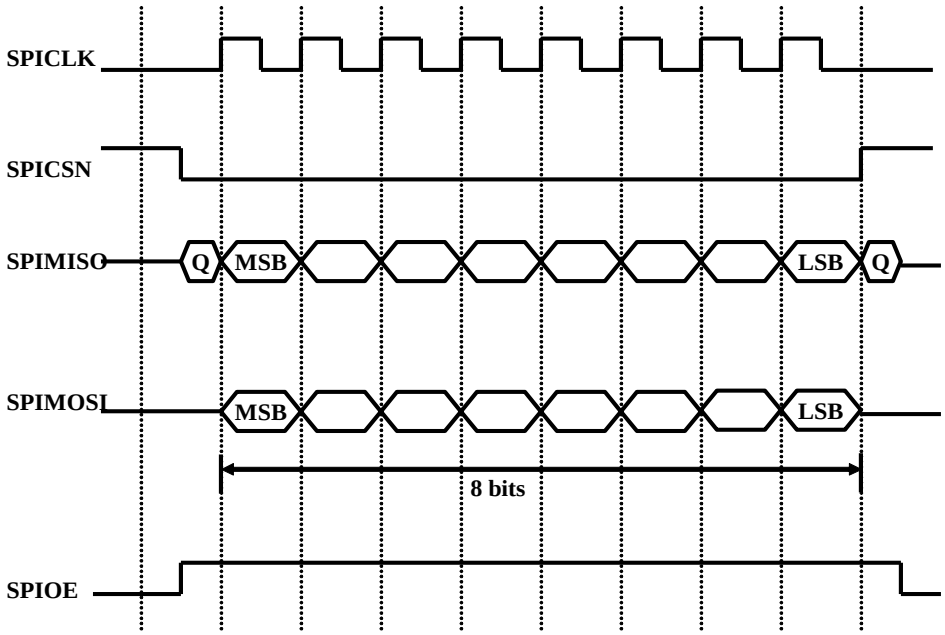


Figure 22-3 Host Mode, SPO=0, SPH=1

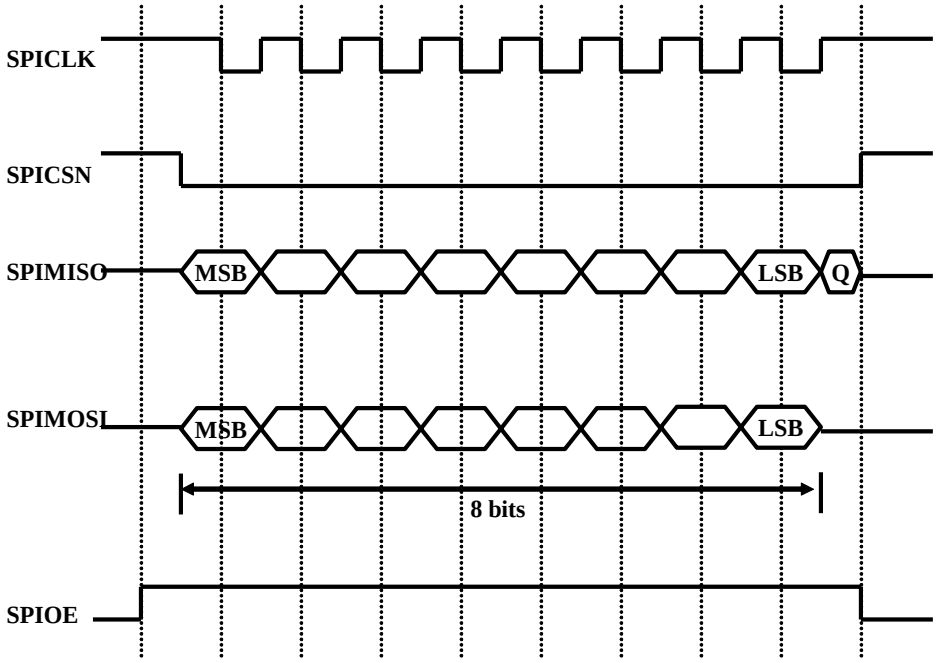


Figure 22-4 Host Mode, SPO=1, SPH=0

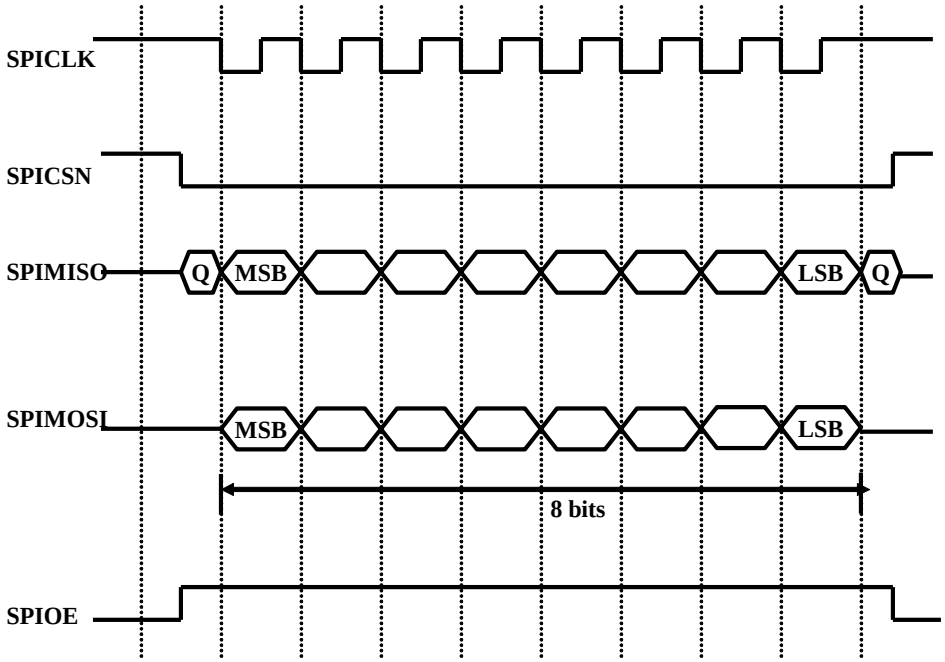


Figure 22-5 Host Mode, SPO=1, SPH=1

22.6.2 Slave Mode

About SPI Slave mode, SPICLK and SPICSN will be generated by external Host. The Slave mode of SPI supports CLK polarity and phase configuration. SPI_TXDAT and SPI_RXDAT registers can be used in data transmission or receiving. The Slave mode of SPI supports the biggest SPICLK is APBCLK/2. When it receiving CLK frequency is faster, we suggest using DMA to transmit data.

22.6.3 Continuous Bytes Transmission

Continuous bytes transmission can be used in Host or Slave mode. When data transmission, only TNF set 1, software can continue transmit data. When receiving data, software needs to check the overflow flag bit to detect whether it lost data due to low rotating rate.

23. I²C Controller

23.1 Introduction

I²C controller provides a interface to fulfill Philips I²C bus requirements, and it supports duplex transmission. I²C is using 2 lines to connect with bus equipments to transmit message: SCL (Serial Clock Line) and SDA(Serial Data Line). I²C supports single-byte transmission. Status register reflects the status of I²C controller and I²C bus. The settings of I²C controller will be reset after it woke-up from sleep or deep-sleep mode. User should restore the settings by manual after it woke-up from sleep or deep-sleep mode. The maximum supporting frequency of I²C: f_{SCL}=1MHz (cycle: 1μs), we can achieve it via setting overflows frequency in TIMER3.

23.2 Features

--Support Host transmission, Host receiving mode;

--Support Slave transmission, Slave receiving mode;

--Bus arbitration failure monitoring;

--Support interrupt signal;

--Programmable response (ACK) generation;

--Programmable the master mode CLK frequency;

--Debounce at input terminal.

23.3 Functional Block Diagram

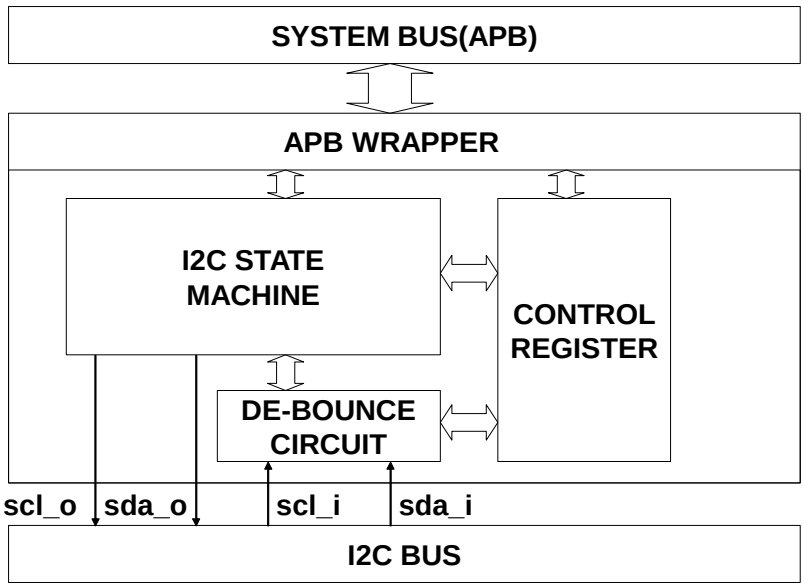


Figure 23-1 I²C Functional Block Diagram

23.4 Register Address

Table 23-1 I²C (I²C Base Address:0x40010800)

Name	Type	Address	Contents	Default
I2C_DATA	R/W	0x0000	I²C data register	0x00
I2C_ADDR	R/W	0x0004	I²C address register	0x00
I2C_CTRL	R/W	0x0008	I²C control/ status register	0x00
I2C_STS	R/W	0x000c	I²C status register	0xF8
I2C_CTRL2	R/W	0x0018	I²C interrupt enable register	0x0

23.5 Register Definition

23.5.1 I2C_DATA Register

Table 23-2 I2C_DATA Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	DATA	R/W	I2C_DATA register including a byte will transmit or received. If the 8-bit register is not in byte shift, CPU can process writing operation for it. There is no shadow register or multiple buffers. So, user only can read I2C_DATA during I^2C interrupt occurs.	0x00

23.5.2 I2C_ADDR Register

Table 23-3 I2C_ADDR Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:1	SLA	R/W	I^2C Slave address (7 bits)	0x00
0	GC	R/W	The response of broadcast calling address If the bit set 1, it will identify the boradcast calling address; otherwise it will ignore the broadcast calling address.	0x0

23.5.3 I2C_CTRL Register

Table 23-4 I2C_CTRL Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7	CR2	R/W	CLK frequency control bit 2	0x0
6	EN	R/W	I^2C enable bit When EN=0, it will set "sdao" and "sclo" output to 1, and chip output is high resistance. Meanwhile, the input signal of "sdai" and "scli" will be ignored. When EN=1, I^2C components will be enabled, and the corresponding IO will automatic be set to I^2C function.	0x0

5	STA	R/W	START flag bit When STA=1, I²C components checks I²C bus status. If bus idle, it will generate a START status.	0x0
4	STO	R/W	STOP flag bit When STO=1 and I²C interface in Host mode, it will transmit a "STOP" status for I²C bus.	0x0
3	SI	R/C	Serial interrupt flag bit When I²C has 25 input status, total is 26 (except F8h), "SI" will be set 1 by hardware. F8h is only no set bit "SI", and it represents there is no available information. "SI" flag bit must be cleared 0 by software. In order to clean "SI" bit, we must write 0 in the bit. Write 1 in the bit, we will not change "SI" value. When interrupt happened, we must set the necessary controller or data in advance.	0x0
2	AA	R/W	Effective response flag bit When AA=1, it will return "response" as the following circumstances: -Already received "own Slave address" -When GC bit set 1 in I²C address register, received a broadcast calling address. When I²C is in Host mode, already received data byte. -When I²C is in Slave mode, already received data byte. When AA='0', it will return " no response" as the following circumstances: -When I²C in Host mode, already received data byte. -When I²C in Slave mode, already received data byte.	0x0
1	CR1	R/W	CLK frequency control bit 1	0x0
0	CR0	R/W	CLK frequency control bit 0	0x0

CR2~CR0 is used to control I²C as SCL clock frequency of Host.

Table 23-5 SCL Frequency Settings

CR2	CR1	CR0	SCL Frequency (KHz)	CLK Divider

			PCLK= 6.5536MHz	PCLK= 13.1072MHz	PCLK= 19.6608MHz	PCLK= 26.2144 MHz	
0	0	0	25.6	51.2	76.8	102.4	256
0	0	1	29.2	58.4	87.6	116.8	224
0	1	0	34.1	68.2	102.3	136.4	192
0	1	1	40.9	81.9	122.9	163.8	160
1	0	0	6.8	13.7	20.5	27.3	960
1	0	1	54.6	109.2	163.8	218.4	120
1	1	0	109.2	218.4	327.7	436.9	60
1	1	1	TIMER3 overflows frequency/8				

23.5.4 I2C_STS Register

Table 23-6 I2C_STS Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:3	STS	R	I^2C status code	0x1F
2:0	-	R	Reserved	0

Table 23-7 I^2C Status in Host Transmit Mode

STS	I^2C Status	Response for Application Software					The Next Step for I^2C
		Read/Write I2C_DATA	I2C_CTRL				
			STA	STO	SI	AA	
0x08	"START" status already been transmitted	Write SLA+W*	X	0	0	X	SLA+W will transmit, ACK will be received.
0x10	Transmit "START" status again	Write SLA+W	X	0	0	X	SLA+W will transmit, ACK will be received.
		Write SLA+R*	X	0	0	X	SLA+R will transmit, I^2C will switch to Host receiving mode.
0x18	SLA+W already been transmitted,	Write data byte	0	0	0	X	Data byte will transmit, ACK will be received.
		No operation	1	0	0	X	"START" status will transmit again.

	ACK already been received.	No operation	0	1	0	X	STOP status will transmit, STO flag bit will be reset.
		No operation	1	1	0	X	After STOP status transmitted, and continue transmit a "START" flag bit, STO flag bit also will be reset.
0x20	SLA+W already been transmitted, ACK did not been received.	Write data byte	0	0	0	X	It will transmit data byte, ACK will be received.
		No operation	1	0	0	X	"START" will be transmitted again.
		No operation	0	1	0	X	STOP status will transmit, STO flag bit will be reset.
		No operation	1	1	0	X	After STOP status transmitted, and continue transmit a "START" status, STO flag bit will be reset.
0x28	I^2C data byte already been transmitted, ACK already been received.	Write data byte	0	0	0	X	Data byte will transmit, ACK will be received.
		No operation	1	0	0	X	"START" will transmit again.
		No operation	0	1	0	X	STOP status will transmit, STO flag bit will be reset.
		No operation	1	1	0	X	After STOP status transmitted, continue transmit a "START" status, STO will be reset.
0x30	I^2C data byte already been transmitted, ACK did not been received.	Write data byte *	0	0	0	X	Data byte will transmit, ACK will be received.
		No operation	1	0	0	X	"START" status will transmit again.
		No operation	0	1	0	X	STOP status will transmit, STO flag bit will reset.
		No operation	1	1	0	X	After STOP status transmitted, continue transmit a START status, and STO flag bit will be reset.

*:SLA+W:Slave address[7:1]+writing operation control bit[0], 0 represents writing.

*:SLA+R:Slave address[7:1]+reading operation control bit [0], 1 represents reading.

Table 23-8 I^2C Status in Host Receive Mode

STS	I^2C Status	Response for Application Software		The Next Step for I^2C
		Read/Write	I2C_CTRL	

		I2C_DATA	STA	STO	SI	AA	
0x08	"START" status already transmitted.	Write SLA+R	X	0	0	X	It will transmit SLA+R, and will receive ACK.
0x10	"START" status transmitted again.	Write SLA+R	X	0	0	X	It will transmit SLA+R, and will receive ACK.
		Write SLA+W	X	0	0	X	It will transmit SLA+W, I^2C will switch to Host transmit mode.
0x40	SLA+R already transmitted, ACK alredy received.	No operation	0	0	0	0	It will receive data byte, no ACK returns.
		No operation	0	0	0	1	It will receive data byte, and will return ACK.
0x48	SLA+R already transmitted, ACK did not received.	No operation	1	0	0	X	"START" status will transmit again.
		No operation	0	1	0	X	STOP status will transmit, STO flag bit will be reset.
		No operation	1	1	0	X	After STOP status transmitted, continue transmit a START status, and STOP flag bit will be reset.
0x50	Already received I^2C data byte, already returns ACK.	Read data byte	0	0	0	0	It will receive data byte, no ACK returns.
		Read data byte	0	0	0	1	It will receive data byte, returns ACK.
0x58	Already transmitted I^2C data byte, and no ACK returns.	Read data byte	1	0	0	X	"START" status will transmit again.
		Read data byte	0	1	0	X	STOP status will transmit, STO flag bit will be reset.
		Read data byte	1	1	0	X	After STOP status transmitted, continue transmit next "START" status, STOP flag bit will be reset.

Table 23-9 I^2C Status in Slave Receive Mode

STS	I^2C Status	Response for Application Software		The Next Step for I^2C
		Read/Write	I2C_CTRL	

		I2C_DATA	STA	STO	SI	AA	
0x60	Received SLA+W, and returns ACK.	No operation	X	0	0	0	It will receive data byte, and no return ACK.
		No operation	X	0	0	1	It will receive data byte, and no return ACK.
0x68	Lost when SLA+R/W as Host Already received ALS+W, already returns ACK.	No operation	X	0	0	0	It will receive data byte, and no return ACK.
		No operation	X	0	0	1	It will receive data byte, and no return ACK.
0x70	Already received broadcast address (00H), already returned ACK.	No operation	X	0	0	0	It will receive data byte, and no return ACK.
		No operation	X	0	0	1	It will receive data byte, and no return ACK.
0x78	Lost when SLA+R/W as Host. Already received broadcast address (00H), already returned ACK.	No operation	X	0	0	0	It will receive data byte, and no return ACK.
		No operation	X	0	0	1	It will receive data byte, and no return ACK.
0x80	Using own SLV adderss to search address before. Already received	Read data byte	X	0	0	0	It will receive data byte, and no returns ACK.
		Read data byte	X	0	0	1	It will receive data byte, and returns ACK.

	DATA, and ACK returns.						
0x88	Read data byte	Read data byte	0	0	0	0	Switch to SLV mode. There is no identidy SLA or broadcast address.
		Read data byte	0	0	0	1	Switch to SLV mode. There is no identidy SLA or broadcast address.
		Read data byte	1	0	0	0	Switch to SLV mode. There is no identidy SLA or broadcast address. START status will transmit will bus idle.
		Read data byte	1	0	0	1	Switch to SLV mode. There is no identidy SLA or broadcast address. START status will transmit when bus is idle.
0x90	Using own broadcast address to search address. Already received DATA, already returned ACK.	Read data byte	X	0	0	0	It will receive data byte, no ACK returns.
		Read data byte	X	0	0	1	It will receive data byte, and ACK returns.
0x98	Using own broadcast address to search address. Already received DATA, no ACK returned.	Read data byte	0	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address.
		Read data byte	0	0	0	1	Switch to SLV mode. Did not identify SLA or broadcast address.
		Read data byte	1	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address. START status will transmit when bus is idle.
		Read data byte	1	0	0	1	Switch to SLV mode. Did not identify SLA or broadcast address. START status will transmit when bus is idle.
0xA0	Already STOP status or	No operation	0	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address.

	START status process again. But it still serarch address by Slave transmission and receiving.	No operation	0	0	0	1	Switch to SLV mode. Identify SLA or broadcast address.
		No operation	1	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address. START status will transmit when bus is idle.
		No operation	1	0	0	1	Switch to SLV mode. Identify SLA or broadcast address. START status will transmit when bus is idle.

Table 23-10 I²C Status in Slave Transmit Mode

STS	I²C status	Response for Application Software					The Next Step for I²C
		Read/Write I2C_DATA	I2C_CTRL				
			STA	STO	SI	AA	
0xA8	Already received SLA+R, already returned ACK.	Write data byte	X	0	0	0	It will transmit last data byte, and receive ACK.
		Write data byte	X	0	0	1	It will transmit data byte, and receive ACK.
0xB0	Lost when SLA_R/W as Host. Already received SLA+R, ACl already returns.	Write data byte	X	0	0	0	It will transmit last data byte, and receive ACK.
		Write data byte	X	0	0	1	It will transmit data byte, and receive ACK.
0xB8	Data byte already transmitted, already received ACK.	Write data byte	X	0	0	0	It will transmit last data byte, and receive ACK.
		Write data byte	X	0	0	1	It will transmit data byte, and receive ACK.
0xC0	Data byte already transmitted,	No operation	0	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address.

	did not receive ACK.	No operation	0	0	0	1	Switch to SLV mode. Identify SLA or broadcast address.
		No operation	1	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast. START status will be transmitted when bus is idle.
		No operation	1	0	0	1	Switch to SLV mode. Identify SLA or broadcast address. START status will be transmitted when bus is idle.
0xC8	Last data byte already transmitted, and already received ACK.	No operation	0	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address.
		No operation	0	0	0	1	Switch to SLV mode. Identify SLA or broadcast address.
		No operation	1	0	0	0	Switch to SLV mode. Did not identify SLA or broadcast address. START status wil be transmitted when bus is idle.
		No operation	1	0	0	1	Switch to SLV mode. Identify SLA or broadcast address. START status will be transmitted when bus is idle.

Table 23-11 I²C Status

STS	I²C Status	Response for Application Software					The Next Step for I²C
		Read/ Write I2C_DATA	I2C_CTRL				
			STA	STO	SI	AA	
0x38	Already received SLA+R, ACK already returned.	Write data byte	X	0	0	0	It will transmit last data byte, and receive ACK.
		Write data byte	X	0	0	1	It will transmit data byte, and receive ACK.
0xF8	Lost when SLA+R/W as Host. Already received	Write data byte	X	0	0	0	It will transmit last data byte, and receive ACK.

	SLA+R, ACK already returned.						
0x00	Data byte already transmitted, ACK already received.	Write data byte	X	0	0	0	It will transmit last data byte, and receive ACK.

23.5.5 I2C_CTRL2 Register

Table 23-12 I2C_CTRL2 Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved	0
0	INTEN	R/W	The interrupt enable control in I^2C controller 0:disable 1:enable	0x0

23.6 Application Note

23.6.1 I²C Bus Agreement:Start/ Stop condition

The start state can transmit a byte serial data via SDA line, and the stop state can stop data transmission. The stop state is the low-level to high-level transition of the SDA line when SCL is high-level. The start and stop state are alwaysgenerated by the master devices. When the start state is generated, the I²C bus is busy. After the stop state processes few minutes, I²C bus will be released again.

When the master device enabled the start state, it should send slave device address to confirm the slave devices. A byte address is composed of 7-bit address and 1-bit transmitting direction (i.e.write or read). If the 8th byte is 0, and it represents the writing operation (send operation); if the 8th-byte is 1, and it represents data reading request (receive opreation).

Master transmits the stop state to end the operation. If master wants to continue transmit data to I²C bus, then it should transmit a start state and a slave address in order to process various formats of read/write operations can be performed.

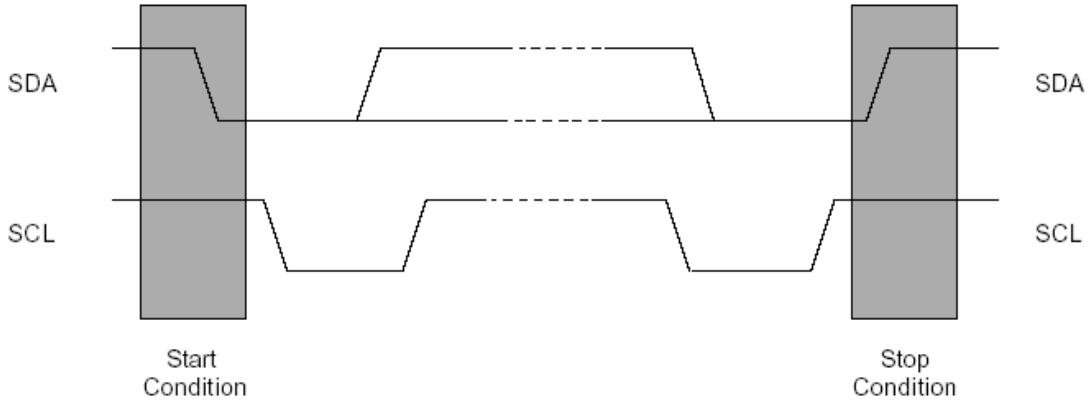


Figure 23-2 Start and Stop Conditions

23.6.2 Data Transmit Format

The length of each byte on the SDA line should be 8 bits. There is no limit to the number of bytes that can be transmitted at a time. The first byte after the start state should be the address field. When the I²C bus is working in master mode, the address field can be sent by the master. Each byte should be followed by an acknowledgment (ACK) bit. The serial data and address are always sent with the MSB first.

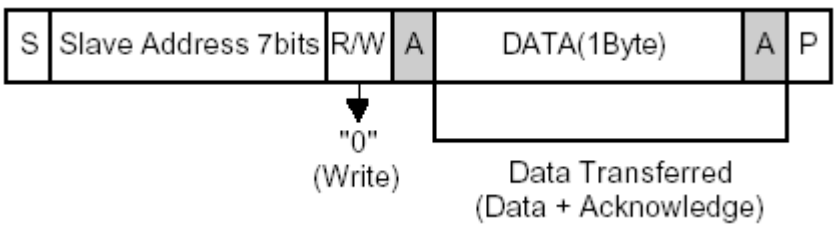


Figure 23-3 7-bit Address Write Mode

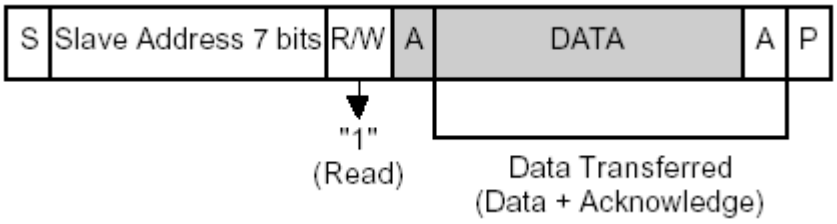


Figure 23-4 7-bit Address Read Mode

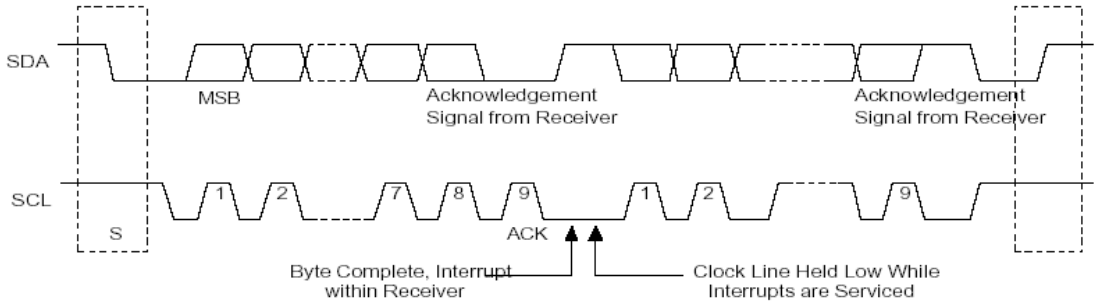


Figure 23-5 Data Transmission

23.6.3 ACK Signal Transmit

To totally complete a byte transmit operation, the receiver should transmit an ACK bit to the transmitter. The ACK pulse should occur in the 9th clock cycle of the SCL line. One byte of data transmit requires eight clock cycles. The master should generate the clock pulse required to send the ACK bit.

When receiving the ACK clock pulse, the transmitter should release the SDA line by setting the SDA line to a high-level. The receiver should also drive the SDA line low during the ACK clock pulse so that SDA is low during the high period of the ninth SCL pulse.

The function of the ACK bit transmit enable or disable can be set by software. However, the ACK pulse on the ninth clock cycle of SCL needs to complete a byte of data transmit operation.

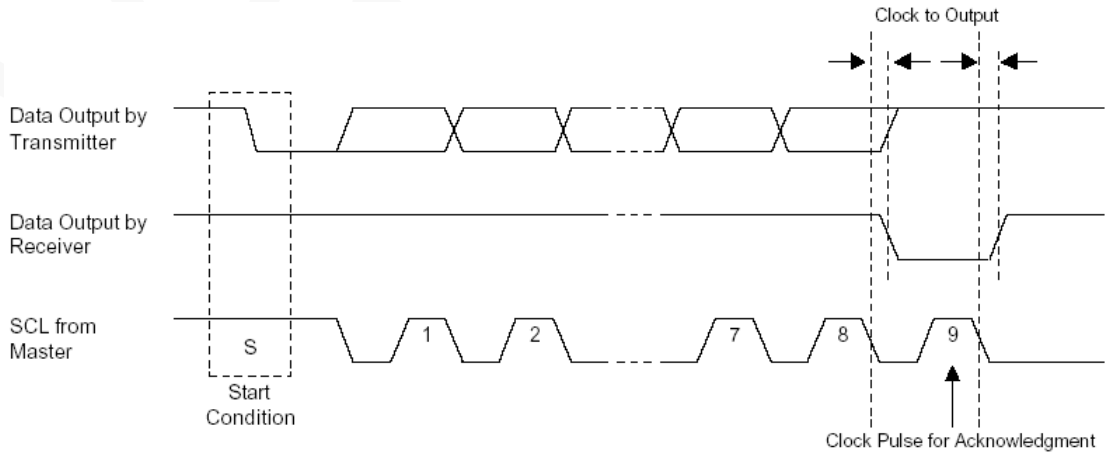


Figure 23-6 The Response Mechanism for I²C Bus

23.6.4 Read/ Write Operation

In transmit mode, after transmit the data, the I^2C bus interface will wait until the pending interrupt is cleared. Before the interrupt is cleared, the SCL line will remain low. After the interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should write the new data to I2C_DATA before clearing the pending interrupt.

In receive mode, after receiving the data, the I^2C bus interface will wait until the pending interrupt is cleared. Before waiting for the interrupt to be cleared, the SCL line will remain low. After the interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clearing the pending interrupt.

Bus Arbitration

Arbitration occurs on the SDA line to prevent competition on the bus between the two masters. If the host whose SDA is high detects that the SDA of another host is low, it will not start data transmission because the current level on the bus does not correspond to itself. The arbitration process will be extended until the SDA line goes high.

However, when SDA line of master is also the low-level, each master should evaluates the controlling right belongs to themselves. In order to evaluation, each master should detect the address. When each master generates a slave address, it should also detect the address in SDA line because SDA low-level priority is higher than SDA line high-level. For example, the first address of a master is low-level, and another master also keeps high-level; under the condition, these 2 masters will detect the low-level in bus because even the first try to keep high in line, the low-level also will be forced to high. When this circumstance happended, the master (as the first address) generated low-level will obtain the controlling right, and the master (as the first address) generated high-level will lose the controlling right. If both 2masters generated low-level in the first address, then they will arbitrate the secondary address. The arbitration will continue the last address.

Suspend State

If the slave receiver does not answer the slave address, it should keep the SDA line high. In this case, the master should generate a stop state and abort the transmission.

If the master receiver wants to suspend the transmission, it should cancel the generation of ACK after receiving the last data byte from the slave to notify the slave of the end of the sending operation. The slave transmitter should release SDA to allow the master to generate a stop state.

23.6.5 Interface Time Sequence

The following figure shows the interface connection of I^2C bus.

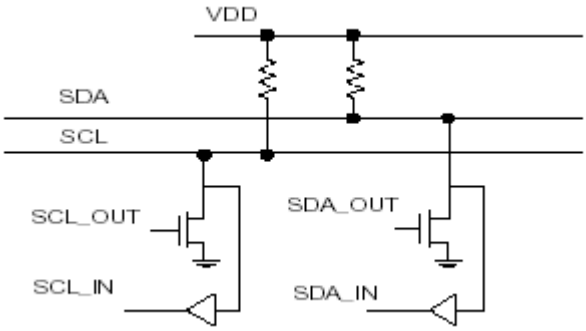


Figure 23-7 I²C Bus Connectoion Side

We can reach the frequency control of different serial clock (SCL) via CR2~CR0 in I2C_CTRL register.

The maximum supports f_{SCL}=1MHz (cycle:1μs).

-The rising time of SCL and SDA: f_{SCL}= 100kHz: 1000ns; f_{SCL}= 400kHz: 300ns

-The falling time of SCL and SDA: f_{SCL}= 100kHz: 300ns; f_{SCL}= 400kHz: 300ns

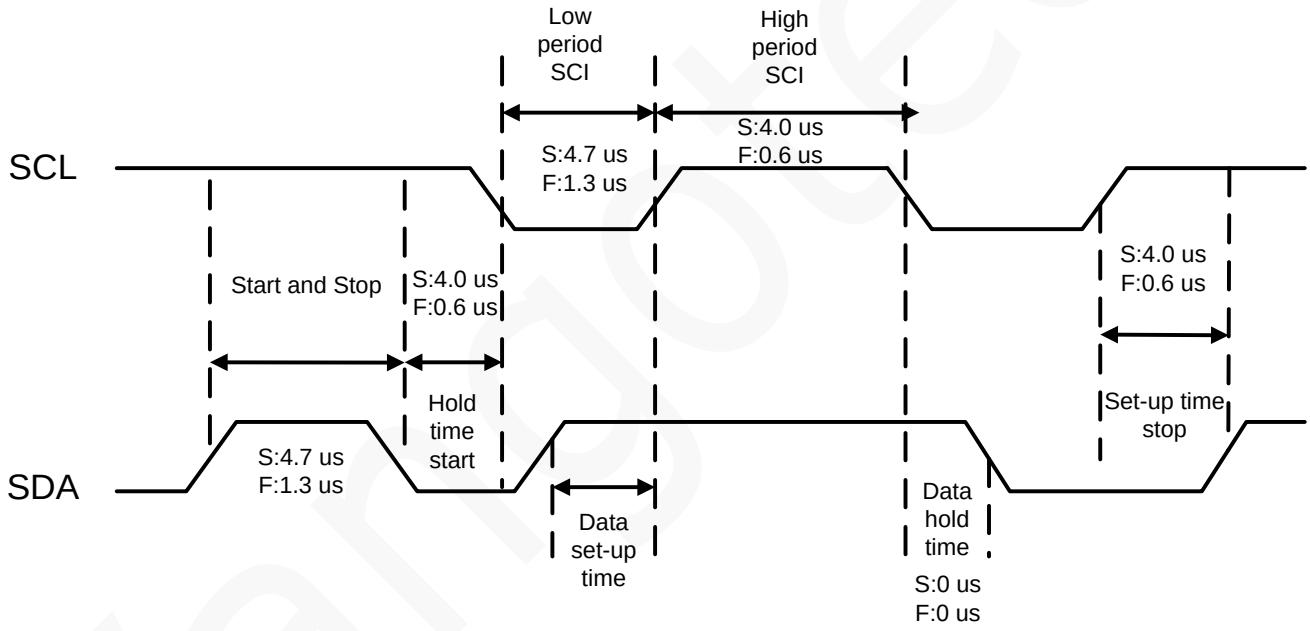


Figure 23-8 SCL and SDA Timing Sequence

Table 23-13 I²C AC Attributes

Time	I2C–master mode(CR<7)		I2C–master mode(CR=7)	
tHD:STA	scl/4	min(15clk)	scl/4	(2bclk)
tLOW	scl/2	min(30clk)	scl/2	(4bclk)
tHIGH	scl/2	min(30clk)	scl/2	(4bclk)
tSU:STA	scl/4	min(15clk)	When scl/4<7clk:scl/2	
			Others:scl/4	
tHD:DAT	6*clk	(6clk)	6*clk	(6clk)

tSU:DAT	1*clk(-forfirstbit)*[1]	(1clk)	1*clk(-forfirstbit)*[1]	(1clk)
	scl/2-6*clk	min(24clk)	scl/2-6*clk	min(1clk)
tSU:STO	scl/4+7*clk	min(22clk)	min(bclk+9)	
tBUF	(¾scl)+9*clk	min(54clk)	min(¾scl)	

*[1] The first bit of the first byte data established time will be shorter, and only a clk. The circumstance only happened when writing data in register, it is closely the rising edge of CSL.

clk:APB clock cycle

bclk:The overflows cycle of timer 3

scl:I²C clock cycle

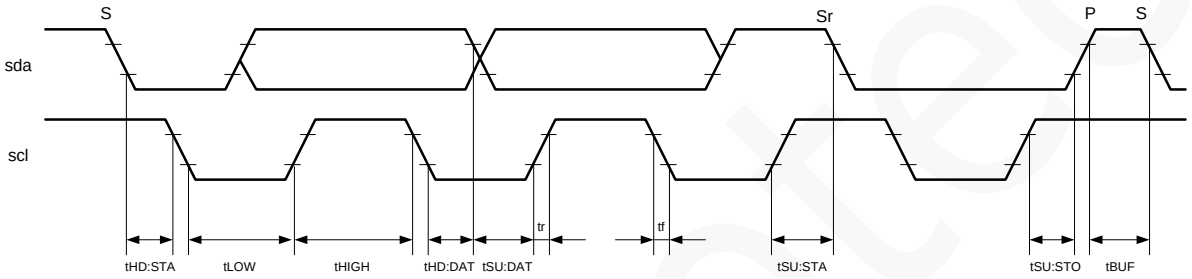


Figure 23-9 AC Timing Sequence of I²C Controller

23.6.6 I²C SDA Solution for Pin Deadlock

During I²C communication process, when the chip reset abnormally (soft-reset, WDT reset, external ESRST pin reset) happended, it may cause I²C bus deadlock status (SDA been deadlocked in low-level status). Solution: before enable I²C, user enhances the time sequence of I²C bus. After reset I²C main equipements, SCL clock line will generate 9 clock pulse in I²C; that is, SDA pin of I²C can reset from deadlock status. If we do not handle the deadlock status currently, it also will not affect I²C using to enhance bus reset.

23.7 Operating Process

23.7.1 Master Transmit Mode

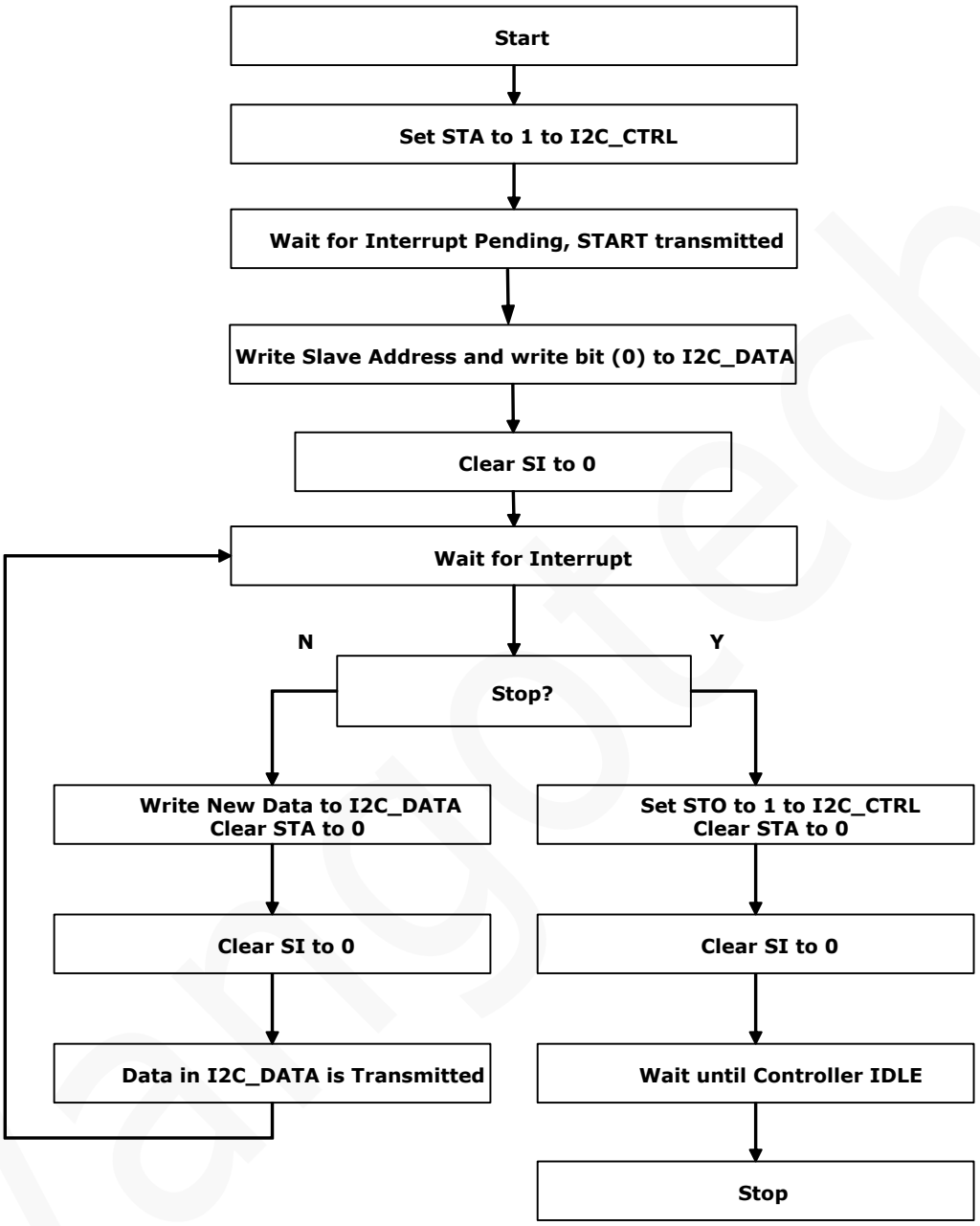


Figure 23-10 The Operating Process of Host Transmit

23.7.2 Master Receive Mode

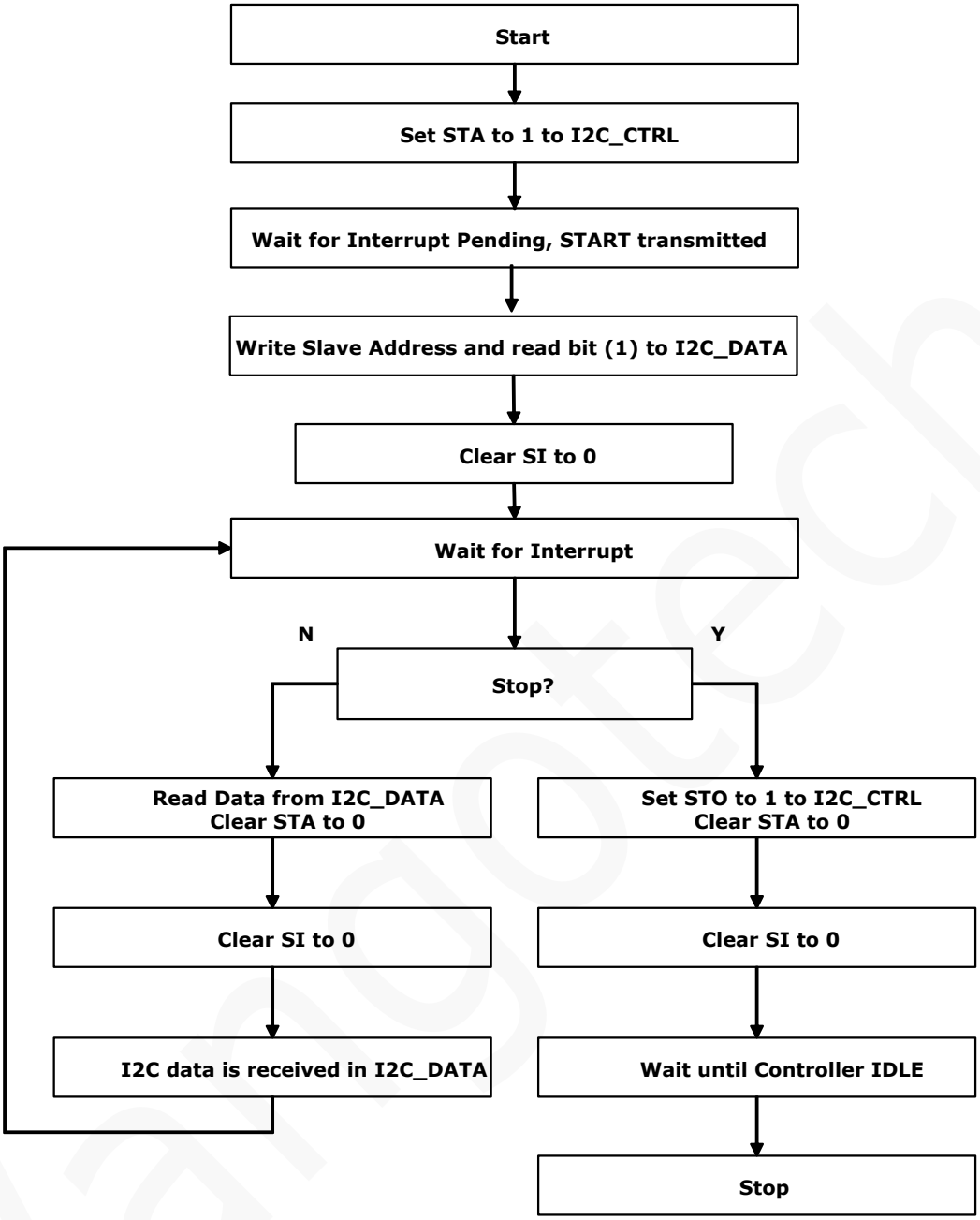


Figure 23-11 The Operating Mode of Host Receive Mode

23.7.3 Slave Transmit Mode

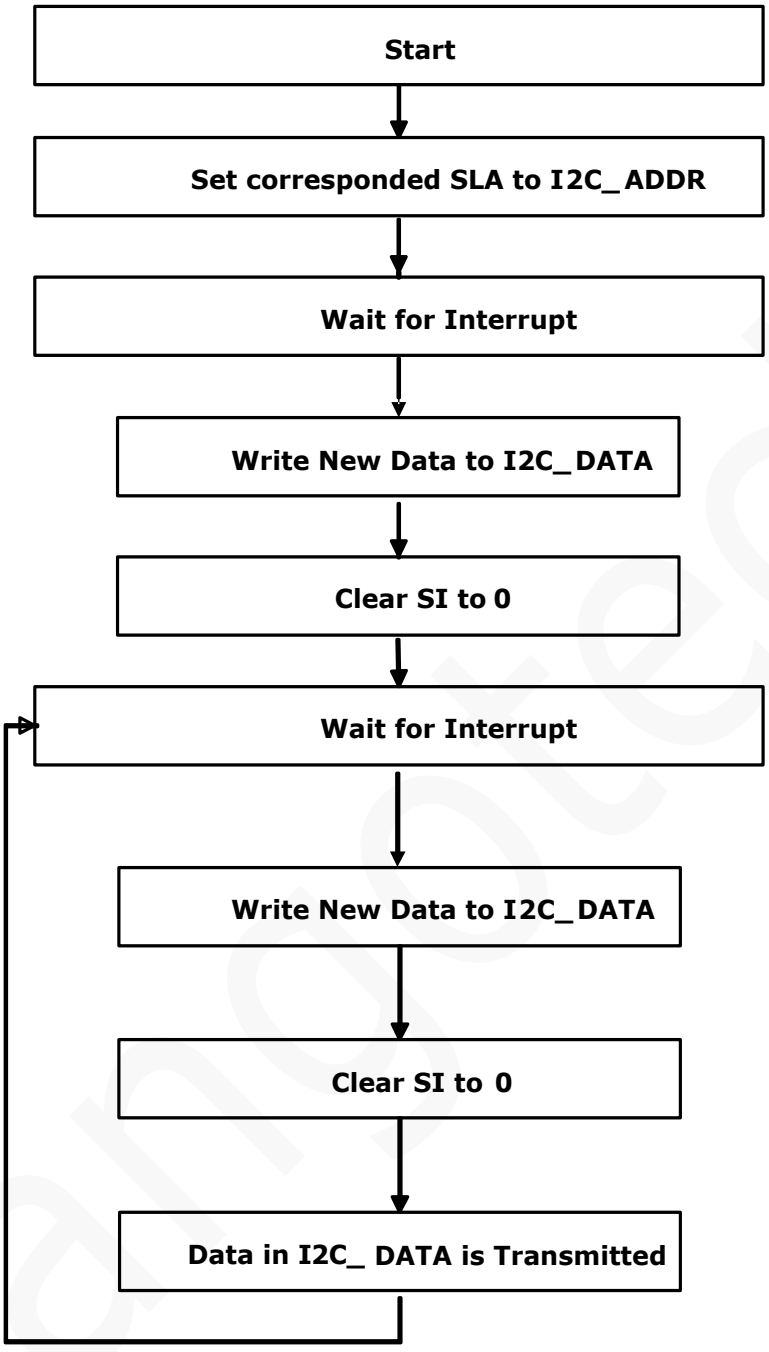


Figure 23-12 The Operating Mode of Slave Transmit Mode

23.7.4 Slave Receive Mode

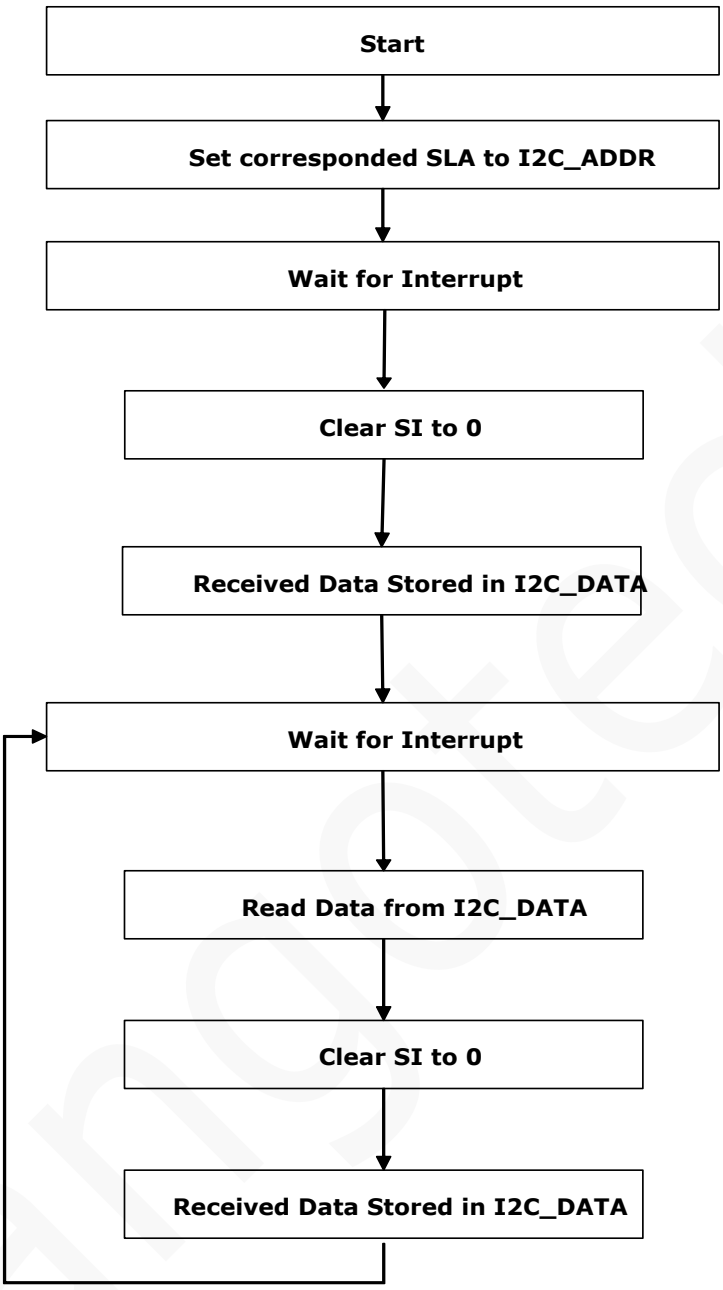


Figure 23-13 The Operating Mode of Slave Receive Mode

24. Interrupt Controller

24.1 Introduction

Any interrupt can wake up system from idle mode. Some of interrupt also can wake up system from sleep mode, and some of interrupt can wake-up system from deep-sleep mode.

24.2 Interrupt Source

Table 24-1 Interrupt Source

Order	Address	Interrupt Serial Number	Contents	Peripherial events enable bit	Peripherial events flag bit	Wake-up Source	
						Deep-sleep	Sleep
NMI	00000008h	-14	NMI				
HardFault	0000000Ch	-13	HardFault				
SVCall	0000002Ch	-5	SVCall				
PendSV	00000038h	-2	PendSV				
SysTick	0000003Ch	-1	SysTick				
PMU	00000040h	0	IOA0~15	PMU_CONTROL.0 and PMU_IOAWKUEN.0~15	PMU_IOAINTSTS.0~15	√	√
			32K crystal invalid	PMU_CONTROL.2	PMU_STS.0	√	√
			6M crystak invalid	PMU_CONTROL.3	PMU_STS.1		
RTC	00000044h	1	ITV and SITV interrupt	RTC_INTEN.0	RTC_INTSTS.0	√	√
			Illegal time format	RTC_INTEN.1	RTC_INTSTS.1	√	√

			Multi-seconds interrupt	RTC_INTEN.2	RTC_INTSTS.2	√	√
			Multi-minutes interruption	RTC_INTEN.3	RTC_INTSTS.3	√	√
			Multi-hours interrupt	RTC_INTEN.4	RTC_INTSTS.4	√	√
			Midnight (00:00) interrupt	RTC_INTEN.5	RTC_INTSTS.5	√	√
			32K counter interrupt	RTC_INTEN.6	RTC_INTSTS.6	√	√
			The illegal writing for CE register	RTC_INTEN.8	RTC_INTSTS.8		
			Alarm interrupt	RTC_INTEN.10	RTC_INTSTS.10	√	√
U32K0~1	00000048h 0000004Ch	2\3	Received data	U32Kx_CTRL1.0	U32Kx_STS.0	√	√
			Received parity check error	U32Kx_CTRL1.1	U32Kx_STS.1	√	√
			Received buffer overflows	U32Kx_CTRL1.2	U32Kx_STS.2	√	√
I2C	00000050h	4	I^2C serial interrupt	I2C_CTRL2.0	I2C_CTRL.3		
SPI1~3	00000054h \000000ACh\000000B0h	5\27\28	SPI transmission	SPIx_TXSTS.14	SPIx_TXSTS.15		
			SPI transmission	SPIx_RXSTS.14	SPIx_RXSTS.15		
UART0~5	00000058h ~0000006Ch	6\7\8\9\10\11	Receive interrupt	UARTx_CTRL.3	UARTx_INTSTS.1		
			Transmit overflows	UARTx_CTRL.4	UARTx_INTSTS.2		
			Receive overflows	UARTx_CTRL.5	UARTx_INTSTS.3		
			Receive parity check error	UARTx_CTRL.7	UARTx_INTSTS.4		

			Transmitted done	UARTx_CTRL.8	UARTx_INTSTS.5		
ISO78160~1	00000070h ~00000074h	12\13	Receive error interrupt	ISO7816x_CFG.2	ISO7816x_INFO.2		
			Receive interrupt	ISO7816x_CFG.5	ISO7816x_INFO.5		
			Transmit interrupt	ISO7816x_CFG.6	ISO7816x_INFO.6		
			Receive overflows	ISO7816x_CFG.7	ISO7816x_INFO.7		
			Re-transmitted error interrupt	ISO7816x_CFG.8	ISO7816x_INFO.8		
Timer0~3	00000078h ~00000084h	14\15\16\17	Timer overflows	TMRx_CTRL.3	TMRx_INTSTS.0		
PWM0~3	00000088h ~000094h	18\19\20\21	PWM timer overflows	PWMx_CTL.1	PWMx_CTL.0		
			Capture/ compare 0	PWMx_CCTL0.4	PWMx_CCTL0.0		
			Capture /compare 1	PWMx_CCTL1.4	PWMx_CCTL1.0		
			Capture /compare 2	PWMx_CCTL2.4	PWMx_CCTL2.0		
DMA	00000098h	22	Channel 0 packet end	DMA_IE.0	DMA_STS.4		
			Channel 1 packet end	DMA_IE.1	DMA_STS.5		
			Channel 2 packet end	DMA_IE.2	DMA_STS.6		
			Channel 3 packet end	DMA_IE.3	DMA_STS.7		
			Channel 0 frame end	DMA_IE.4	DMA_STS.8		

			Channel 1 frame end	DMA_IE.5	DMA_STS.9		
			Channel 2 frame end	DMA_IE.6	DMA_STS.10		
			Channel 3 frame end	DMA_IE.7	DMA_STS.11		
			Channel 0 data abandon	DMA_IE.8	DMA_STS.12		
			Channel 1 data abandon	DMA_IE.9	DMA_STS.13		
			Channel 2 data abandon	DMA_IE.10	DMA_STS.14		
			Channel 3 data abandon	DMA_IE.11	DMA_STS.15		
FLASH	0000009Ch	23	Checksum error	FLASH_CTRL.2	FLASH_INTSTS.0		
ANA	000000A0h	24	ADC switched by manual	ANA_INTEN.0	ANA_INTSTS.0		
			Automatic ADC switched	ANA_INTEN.1	ANA_INTSTS.1		
			The rising and falling edhe of CMP1	ANA_INTEN.2	ANA_INTSTS.2	√	√
			The rising and falling edge of CMP2	ANA_INTEN.3	ANA_INTSTS.3	√	√
			The rising and falling edge of VDDALARM	ANA_INTEN.7	ANA_INTSTS.7	√	√
			The rising and falling of VDCIN	ANA_INTEN.8	ANA_INTSTS.8	√	√
			The rising and falling edge of AVCCLV	ANA_INTEN.10	ANA_INTSTS.10	√	√
			VDCINDROP=0, meanwhile, enter	ANA_INTEN.11	ANA_INTSTS.11	√	√

			the sleep/ deep-sleep mode				
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	√	√
			TADC changes exceeds threshold	ANA_INTEN.13	ANA_INTSTS.13	√	√
			ADC data threshold interruption	ANA_INTEN.14~21	ANA_INTSTS.14~21		

25. MISC Controller

25.1 Introduction

MISC controller is used to control some special function of V85XXP. V85XXP is embedded 2 MISC controllers, one for core field (MISC1 controller), and it will power down under sleep or deep-sleep mode. After woke-up from sleep or deep-sleep mode, the setting of MISC will be reset; and after it woke-up from these 2 modes, user should restore the settings by manual. Another (MISC2 controller) for reserved field, and it will power down under the deep-sleep mode. After woke-up from deep-sleep mode, MISC2 controller will be reset, user should restore the settings by manual after it woke-up from deep-sleep mode.

25.2 Features

--Clock control for each submodule;

--Clock divider of AHBCLK and APBCLK;

--FLASH programmable tick controlling;

-- IR duty cycle control of serial port;

--SRAM parity check interrupt controlling;

25.3 Functional Block Diagram

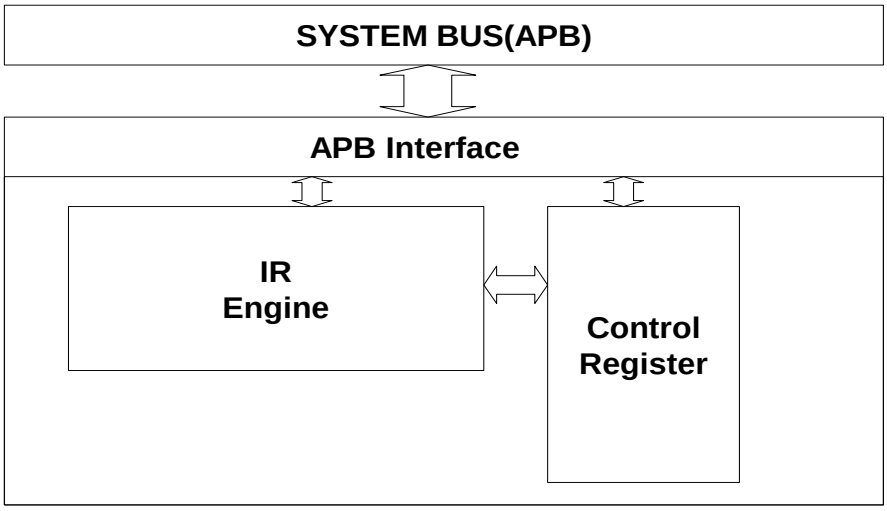


Figure 25-1 MISC Functional Block Diagram

25.4 Register Address

Table 25-1 MISC1 (MISC1 Base Address:0x40013000)

Name	Type	Address	Contents	Default
MISC1_SRAMINT	R/C	0x0000	Interrupt status register for SRAM parity check error	0x00
MISC1_SRAMINIT	R/W	0x0004	SRAM Initialize register	0x01
MISC1_PARERR	R	0x0008	Address register for SRAM parity check error	0x000
MISC1_IREN	R/W	0x000C	IR enable control register	0x00
MISC1_DUTYL	R/W	0x0010	IR modulation wave low-level width control register	0x0000
MISC1_DUTYH	R/W	0x0014	IR modulation wave high-level width control register	0x0000
MISC1_IRQLAT	R/W	0x0018	Cortex-M0 IRQ Delay Control Register	0x000
MISC1_HIADDR	R	0x0020	Records illegal access AHB address	--
MISC1_PIADDR	R	0x0024	Records illegal access AHB address	--

Table 25-2 MISC2 (MISC2 Base Address:0x40013E00)

Name	Type	Address	Contents	Default
MISC2_FLASHWC	R/W	0x0000	FLASH waiting cycle register	0x2100
MISC2_CLKSEL	R/W	0x0004	System select register	0x0
MISC2_CLKDIVH	R/W	0x0008	AHB clock divide control register	0x00
MISC2_CLKDIVP	R/W	0x000C	APB clock divide control register	0x01
MISC2_HCLKEN	R/W	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB clock enable control register	0xFFFFFFFF

25.5 Register Definition

25.5.1 MISC1_SRAMINT Register

Table 25-3 MISC1_SRAMINT Register

Bit	Name	Type	Contents	Default
31:5	-	-	Reserved	0
4	LOCKUP	R/C	The bit represents CM0 locked, write 1 to clear the bit.	0x0

3	PIAC	R/C	The bit represents the invalid address access in APB bus. The invalid APB address is not in 0x40010000～0x4001FFFF field address. If PIACIE is 1, then transmit NMI interrupt to CM0. Write 1 to clear the bit.	0x0
2	HIAC	R/C	The bit represents the invalid address access in APB bus. The invalid address is not FLASH, SRAM or IO, other than address. If HIACIE is 1, then transmit NMI interrupt to CM0. Write 1 to clear the bit.	0x0
1	HIAL	R/C	The bit represents the invalid align access in AHB bus. Meanwhile, the failure address is locked in MISC1_HIADDR. Write 1 to clear the bit.	0
0	PERR	R/C	The bit represents the parity check error duing SRAM reading. If PERRIE is 1, then transmit NMI interrupt to CM0. Write 1 to clear the bit.	0x0

25.5.2 MISC1_SRAMINIT Register

Table 25-4 MISC1_SRAMINIT Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7	LOCKIE	R/W	When CM0 locked happens, enable NMI	0x0
6	PIACIE	R/W	When APB invalid address access happens, enable NMI.	0x0
5	HIACIE	R/W	When AHB invalid address acess happens, enable NMI.	0x0
4:3	-	-	Reserved	0
2	INIT	R/W	SRAM is a initialization register, the register set 1. It will use all zero value of parity check to initialize SRAM. The bit will automatic clear 0. During the initialization time, there is no permit to access any Host in bus (CPU or DMA); otherwise, the access value is a error value.	0x0
1	PERRIE	R/W	When SRAM parity check error, enable NMI.	0x0
0	PEN	R/W	Parity check enable register. When the bit set 1, any writing access to SRAM will write message in parity buffer. During SRAM reading, it will automatic parity check, and generated a parity interrupt during it failed. The function default is opened, so it no needs any special operation in	0x1

			software. However, if CPU or DMA access some field which is not initialization, it may will happened the parity error because there is not existing the parity check in not initialization field. Meanwhile, user can use INIT bit to process SRAM initialization.	

25.5.3 MISC1_PARERR Register

Table 25-5 MISC1_PARERR Register

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved	0
13:0	PEADDR	R	Parity check error address. The register will store the parity check error. When error happened, user can check the error address in SRAM via the register. SRAM error address =0x20000000+4*PEADDR	--

25.5.4 MISC1_IREN Register

Table 25-6 MISC1_IREN Register

Bit	Name	Type	Contents	Default
31:6	-	-	Reserved	0
5:0	IREN	R/W	IR enable control register. Each bit in the register is correspond a UATTTX channel. When IREN[x] set 1, represents UARTTX[x] will be output by IR pulse modulation.	0x0

25.5.5 MISC1_DUTYL Register

Table 25-7 MISC1_DUTYL Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	DUTYL	R/W	Infrared Carrier wave (IR) modulation wave low level width control register . Low pulse width will be (BUTYL+1) *APBCLK cycle.	0x0000

25.5.6 MISC1_DUTYH Register

Table 25-8 MISC1_DUTYH Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	DUTYH	R/W	Infrared(IR) modem wave high-level width control register . High pulse width will be (DUTYH+1)*APBCLK cycle.	0x0000

25.5.7 MISC1_IRQLAT Register

Table 25-9 MISC1_IRQLAT Register

Bit	Name	Type	Contents	Default
31:10	-	-	Reserved	0
9	NOHARDFAULT	R/W	The register is used to disable CPU generating HardFault interruption. 0: When bus error happened, enable HardFault interruption. 1: When bus error happened, disable HardFault interruption. When CM0 detective hardware error happened, it will skip to hardware error interrupt service. After hardware error service completed, program will skip to the normal code and execute the same instruction. Therefore, if hardware error happened again, it will stop in this cycle and never goes out again. The register is used to CPU temporarly disable the hardware error generated.	0x0
8	LOCKRESET	R/W	This register is used to control whether the lockup will issue a system reset 0: Disable CM0 lock reset generation. 1: Enable reset generation locked by CM0.	0x0
7:0	IRQLAT	R/W	The register is used to control Cortex-M0 IRQ response delay. If this bit is set to 0, interrupts are taken as quickly as possible. For no waiting condition to reach no joggle at least set 13 (DEC). For no waiting condition, it will use the higher value to reach no joggle.	0x00

25.5.8 MISC1_HIADDR Register

Table 25-10 MISC1_HIADDR Register

Bit	Name	Type	Contents	Default
31:0	HIADDR	R	AHB bus error address. The register is stored the error address information for acessing AHB bus. When error happened, user can access the error address via the register located AHB bus. The error address= HIADDR	--

25.5.9 MISC1_PIADDR Register

Table 25-11 MISC1_PIADDR Register

Bit	Name	Type	Contents	Default
31:0	PIADDR	R	APB bus error address. The register is stored the error address information for acessing APB bus. When error happened, user can access the error address via the register located APB bus. The error address= 0x40000000 + PIADDR	--

25.5.10 MISC2_FLASHWC Register

Table 25-12 MISC2_FLASHWC Register

Bit	Name	Type	Contents	Default
31:14	-	-	Reserved	0
13:8	CYCLE_1US	R/W	The register is used to FLASH controller and calculate AHBClock 1μs tick. The setting is related to FLASH wake-up time, FLASH erase time, and FLASH programming time. FLASH wake-up time= 1μs tick time*10. Must meet 1μstick>=1μs. 1μstick=(AHB clock cycle)*(CYCLE_1US+1)。 For example, AHB clock frequency is 26.2144M. In order to ensure 1μs tick time, and the smallest wake-up time, CYCLE_1US should set 26. This time, FLASH wake-up time is 27/ 2621440*10, around 10μs. For example, AHB clock frequency is 32.768k. In order to ensure 1μs tick time, and the smallest wake-up time, CYCLE_1US should set 0. This time, FLASH wake-up time is 1/32768*10, around 305μs.	0x21

7:0	-	-	Reserved	0

25.5.11 MISC2_CLKSEL Register

Table 25-13 MISC2_CLKSEL Register

Bit	Name	Type	Contents	Default
31:3	-	-	Reserved	0
2:0	CLKSEL	R/W	The register is used to control AHB clock source. 0:RCH (6.5M RC) 1:XOH (6.5M XTAL) 2:PLLH 3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register) 4:PLLL 5:reserved 6:reserved 7:reserved Before clock selects a clock source, user should enable the corresponding module via PMU_CONTROL register.	0x0

25.5.12 MISC2_CLKDIVH Register

Table 25-14 MISC2_CLKDIVH Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	CLKDIVH	R/W	The register is used to control AHB clock division. 0:clock source divide by 1 1:clock source divide by 2 2:clock source divide by 3 ... 255:clock source divide by 256	0x00

25.5.13 MISC2_CLKDIVP Register

Table 25-15 MISC2_CLKDIVP Register

Bit	Name	Type	Contents	Default
31:8	-	-	Reserved	0
7:0	CLKDIVP	R/W	The register is used to control APB clock division. 0:AHB clock divide by 1 1:AHB clock divide by 2 2:AHB clock divide by 3 ... 255:AHB clock divide by 256	0x01

25.5.14 MISC2_HCLKEN Register

Table 25-16 MISC2_HCLKEN Register

Bit	Name	Type	Contents	Default
31:9	-	-	reserved	0
8:0	HCLKEN	R/W	The register is used to control the clock enable of each AHB module. The corresponding module can be disabled only when its function do not be used. The details about each module, please refer to the following table. 0:disable; 1:enable.	0x1FF

Table 25-17 HCLK Clock Enable

Bit	Module	Attention
0	--	Reserved
1	Arbiter and BusMatrix	Reserved
2	FLASH	Reserved
3	SRAM	Reserved
4	DMA	
5	GPIO	
6	LCD	
7	--	
8	CRYPT	

25.5.15 MISC2_PCLKEN Register

Table 25-18 MISC2_PCLKEN Register

Bit	Name	Type	Contents	Default
31:0	PCLKEN	R/W	The register is used to control the clock enable of each APB module. The corresponding module can be disabled only when its function do not be used. The detail about each module, please refer to the following table. 0:disable 1:enable	0xFFFFFFFF

Table 25-19 PCLK Clock Enable

Bit	Module	Attention
0	AHB2APB Bridge	Reserved
1	DMA	
2	I2C	
3	SPI1	
4	UART0	
5	UART1	
6	UART2	
7	UART3	
8	UART4	
9	UART5	
10	ISO78160	
11	ISO78161	
12	TIMER	
13	MISC1	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K0	

19	U32K1	
20	Reserved	
21	SPI2	
22	SPI3	
31:23	Reserved	

26. CRYPT Controller

26.1 Introduction

The CRYPT controller is used to accelerate ECC. The main features of the CRYPT controller is to realize VLI variable-length integer multiplication, addition (with carry), subtraction (with borrow) and shift. It is 4 times higher than the processing power realized by pure software. Any encryption algorithm that uses VLI can use this hardware to accelerate processing and increase processing speed. The CRYPT controller can directly access SRAM without affecting the access of the M0 processor core.

26.2 Features

--Support variable length integers from 32-bit to 512-bit;

--VLI multiplication;

--VLI ADC;

--VLI SBB;

--VLI logical shift right;

--Directly acess internal SRAM.

26.3 Functional Block Diagram

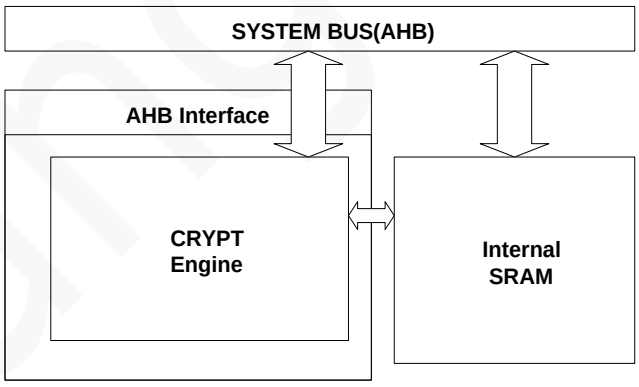


Figure 26-1 CRYPT Functional Block Diagram

26.4 Register Address

Table 26-1 CRYPT (CRYPT Base Address:0x40006000)

Name	Type	Address	Contents	Default
CRYPT_CTRL	R/W	0x0000	CRYPT control register	0x0000
CRYPT_PTRA	R/W	0x0004	CRYPT pointer A	0x0000
CRYPT_PTRB	R/W	0x0008	CRYPT pointer B	0x0000

CRYPT_PTRO	R/W	0x000C	CRYPT pointer O	0x0000
CRYPT_CARRY	R	0x0010	CRYPT carry register	0x0

26.5 Register Definiton

26.5.1 CRYPT_CTRL Register

Table 26-2 CRYPT_CTRL Register

Bit	Name	Type	Contents	Default
31:16	–	–	Reserved	0
15	NOSTOP	R/W	The bit is used to when CRYPT is busy, whether permit CPU reading or writing CRYPT register. 0:When CRYPT is busy, prohibit CPU accessing CRYPT register. 1:When CRYPT is busy, permit CPU accessing CRYPT register. The bit only works in CPU acessing CRYPT register. If it do not acess CRYPT register, the bit is not affected.	0x0
14:12	–	–	Reserved	0
11:8	LENGTH	R/W	The bit is used to control currently the length of operation data (VLI). The length of setting can work simultaneously with ACT set 1. However, if ACT was already 1, we cannot change the bit. 0:32 bits 1:64 bits 2:96 bits …… 15:512 bits	0x0
7	–	–	Reserved	0
6:4	MODE	R/W	The bit is used to control CRYPT operation. The bit setting can work simultanesouly with ACT set 1. However, if ACT was already 1, we cannot change the bit. 0:multiplication, *PTRO=*PTRAx*PTRB 1:add, *PTRO=*PTRA+*PTRB	0x0

			2:subtraction, *PTRO=*PTRA-*PTRB 3:logical shift right, *PTRO=(*PTRA>>1) 4~7:reserved	
3:1	–	–	Reserved	0
0	ACT	R/W	Write 1 in the bit, it will enable the specified calculation of MODE register. After calculation completed, the bit will be cleared 0. And it is valid to write 0 in the bit.	0x0

26.5.2 CRYPT_PTRA Register

Table 26-3 CRYPT_PTRA Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	PTRA	R/W	Pointer A of CRYPT. The valud of PTRA is a SRAM address. The data in the address is used to CRYPT calculation. Due to CRYPT only can control the access of 32 bits, so PTRA[1:0] should always be 0.	0x0000

26.5.3 CRYPT_PTRB Register

Table 26-4 CRYPT_PTRB Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	PTRB	R/W	The pointer B of CRYPT. The value of PTRB is a SRAM address. The data in address is used to CRYPT calculation. Due to CRYPT only can control the access of 32 bits, so PTRB[1:0] shoud always be 0.	0x0000

26.5.4 CRYPT_PTRO Register

Table 26-5 CRYPT_PTRO Register

Bit	Name	Type	Contents	Default
31:16	-	-	Reserved	0
15:0	PTRO	R/W	The pointer O of CRYPT. The value of PTRO is a SRAM address. The data in address is used to store CRYPT	0x0000

			calculation result. Due to CRYPT only can control the access of 32 bits, so PTRO[1:0] shoud always be 0.	

26.5.5 CRYPT_CARRY Register

Table 26-6 CRYPT_CARRY Register

Bit	Name	Type	Contents	Default
31:1	-	-	Reserved	0
0	CARRY	R	The bit represents carry after addition, or borrow after subtraction. After user completed the calculation (ACT will be cleared 0), it will directly read the value of register.	0x0

26.6 Precuations

26.6.1 Data Format

VLI is a positive integer between 32 to 512 bits. So, all operation is unsigned number calculation. The following table shows SRAM number orders.

Address	Data
PTR+0	VLI[31:0]
PTR+4	VLI[63:32]
PTR+8	VLI[95:64]
PTR+12	VLI[127:96]
……	……
PTR+60	VLI[511:480]

Under the different length register, only VLI defined data length can be a intput data. The following table shows the valid VLI numbers in different length settings.

LENGTH	Data
0	VLI[31:0]
1	VLI[63:0]
2	VLI[95:0]
3	VLI[127:0]
……	……
15	VLI[511:0]

26.6.2 Calculation Details

For each calculation, they will show the various of behaviors, such as the handling time cycle, output data width etc… The following table shows the calculation details in each mode.

	MULT	ADD	SUB	RSHIFT1
Operation	*PTRO= *PTRA x *PTRB	*PTRO= *PTRA + *PTRB	*PTRO= *PTRA - *PTRB	*PTRO= (*PTRA>>1)
Outputlength	2*input length	Input length	Input length	Input length
CARRYbit	X	0:output without carry 1:output with carry	0:*PTRA>*PTRB 1:*PTRA<*PTRB	X
LENGTH	**Calculation Cycle**			
0	8	6	6	6
1	17	8	8	8
2	32	12	12	10
3	53	14	14	12
4	80	18	18	14
5	113	20	20	16
6	152	24	24	18
7	197	26	26	20
8	248	30	30	22
9	305	32	32	24
10	368	36	36	26
11	437	38	38	28
12	512	42	42	30
13	593	44	44	32
14	680	48	48	34
15	773	50	50	36

Under the default situation, any access for CPU to CRYPT register will idle until the calculation completed. During the calculation, any changes is not allowed. Therefore, when there is priority events happened, it will be blocked until CPU is released by CRYPT events. Set NOSTOP to 1 to avoid this situation happening, but we need to ensure CRYPT configuration no changes during CRYPT calculation.

Because CRYPT only supports the data operation of SRAM, so when one of operation did not in SRAM, user should move data to SRAM before calculation.

27. Debug Features

V85XXP uses the Cortex-M0 core, which contains the hardware debug module.

27.1 Features

The Cortex-M0 processor supports a number of useful debug features:

--Halting, resuming, and single stepping of program execution;

--Access to processor core registers and special registers;

--Hardware breakpoints (up to four comparators);

--Software breakpoints (BKPT instruction);

--UP to 2 Data monitoring points;

--Dynamic memory access;

--Supports serial wire debug (SWD) protocol;

27.2 SWD Pins

Table 27-1 The Special Function of SWD Pins

Mode	Pin 1	Pin 2
Debug Mode Low-level for MODE pin	SWCLK	SWDIO
Normal Mode High-level for MODE pin	LCDSEG54/IOA0	LCDSEG53/IOA1

28. Cortex-M0 Instruction

ARM Cortec-M0 processor is mainly fulfilled the design for ultra-low power MCU and mixed signal devices. It used 3th-level pipeline of VonNeumann architecture. Through simple, stronger ISA, and fully optimized design (including a single cycle multiplication to handle highly hardware), ARM Cortex-M0 Processor can achieve extremely high energy efficiency. ARM Cortex-M0 Processor used ARMv6-M architecture which is based on 16 bits Thumb ISA and Thumb-2 skils.

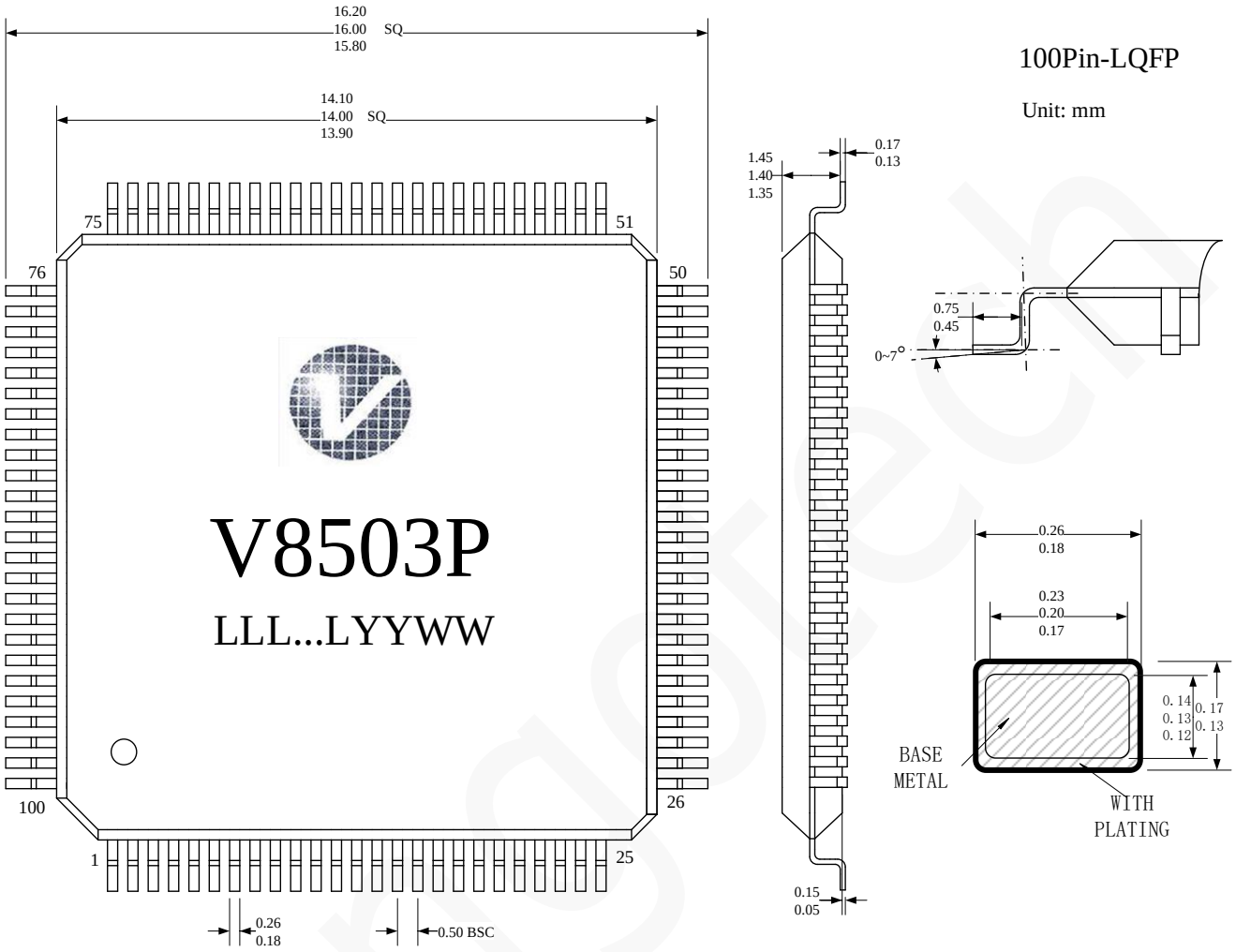
28.1 CMSIS Functions

Table 28-1 CMSIS Functions

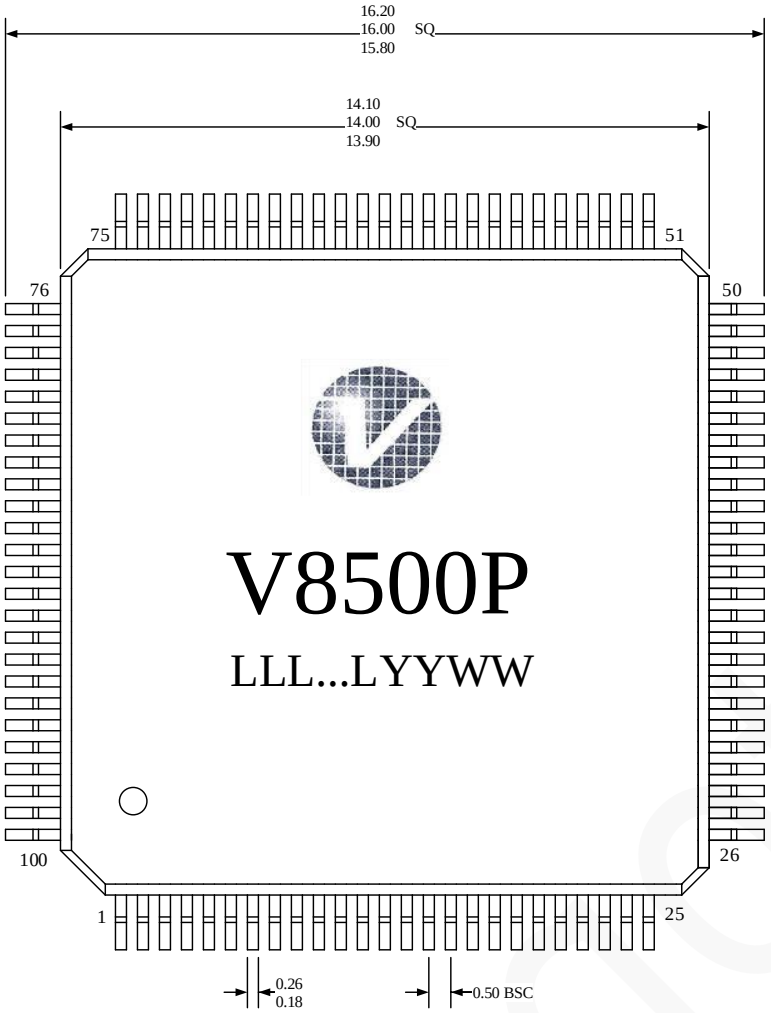
Function	Description
void NVIC_EnableIRQ(IRQn_Type IRQn);	Enable IRQn interrupt. The function is not applicable the abnormal system situation.
void NVIC_DisableIRQ(IRQn_Type IRQn);	Disable IRQn interrupt. The function is not applicable to the abnormal system situation.
void VIC_SetPendingIRQ(IRQn_Type IRQn);	Set IRQn interrupt idle situation. The function is not applicable to the abnormal system situation.
void NVIC_ClearPendingIRQ(IRQn_Type IRQn);	Clear IRQn interrupt idle situation. The function is not applicable to the abnormal system situation.
uint32_t NVIC_GetPendingIRQ(IRQn_Type IRQn);	Obtain IRQn interrupt idle situation
void NVIC_SetPriority(IRQn_Type IRQn,uint32_t priority);	Set IRQn interrupt priority
uint32_t NVIC_GetPriority(IRQn_TypeIRQn);	Obtain IRQn interrupt priority
void __enable_irq(void);	Enable all interrupt
void __disable_irq(void);	Disable all interrupt (except hardfault and NMI)
uint32_t SysTick_Config(uint32_t ticks);	Initialization and enable SysTick counter and its interrupt
void NVIC_SystemReset(void);	M0 core soft reset
SCB->SCR |= SCB_SCR_SLEEPDEEP_Msk; void __WFI(void);	Wait to interrupt (enter sleep mode)
SCB->SCR &= (uint32_t)~((uint32_t)SCB_SCR_SLEEPDEEP_Msk); void __WFI(void);	Wait to interrupt (enter IDLE mode)

29. Package Dimensions

29.1 V8503P Package Dimension

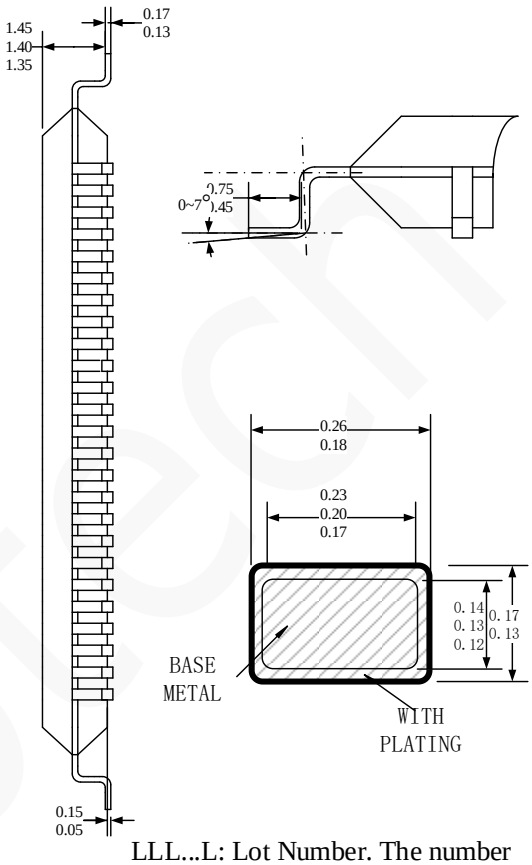


29.2 V8500P Package Dimension



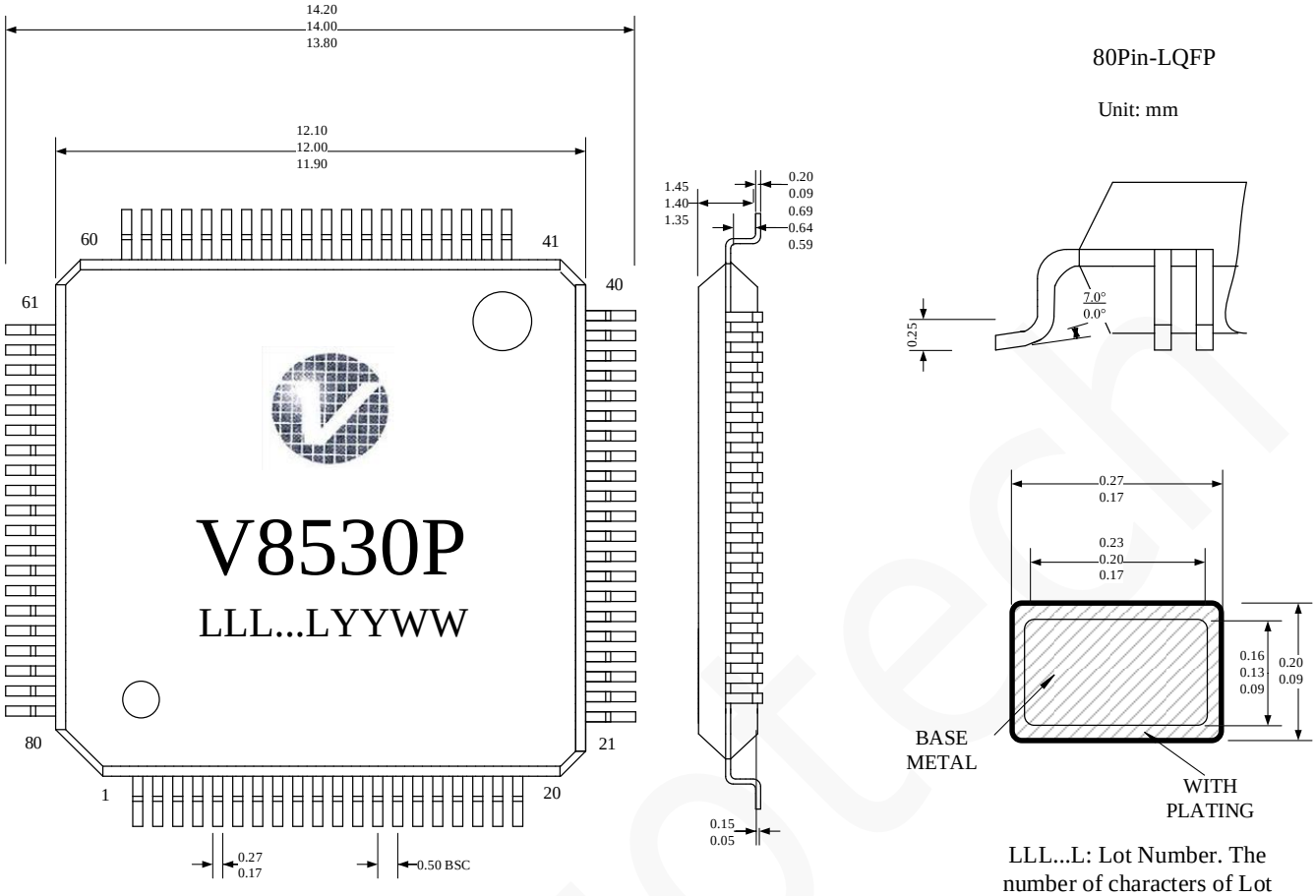
100Pin-LQFP

Unit: mm



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

29.3 V8530P/V8531P Package Dimension

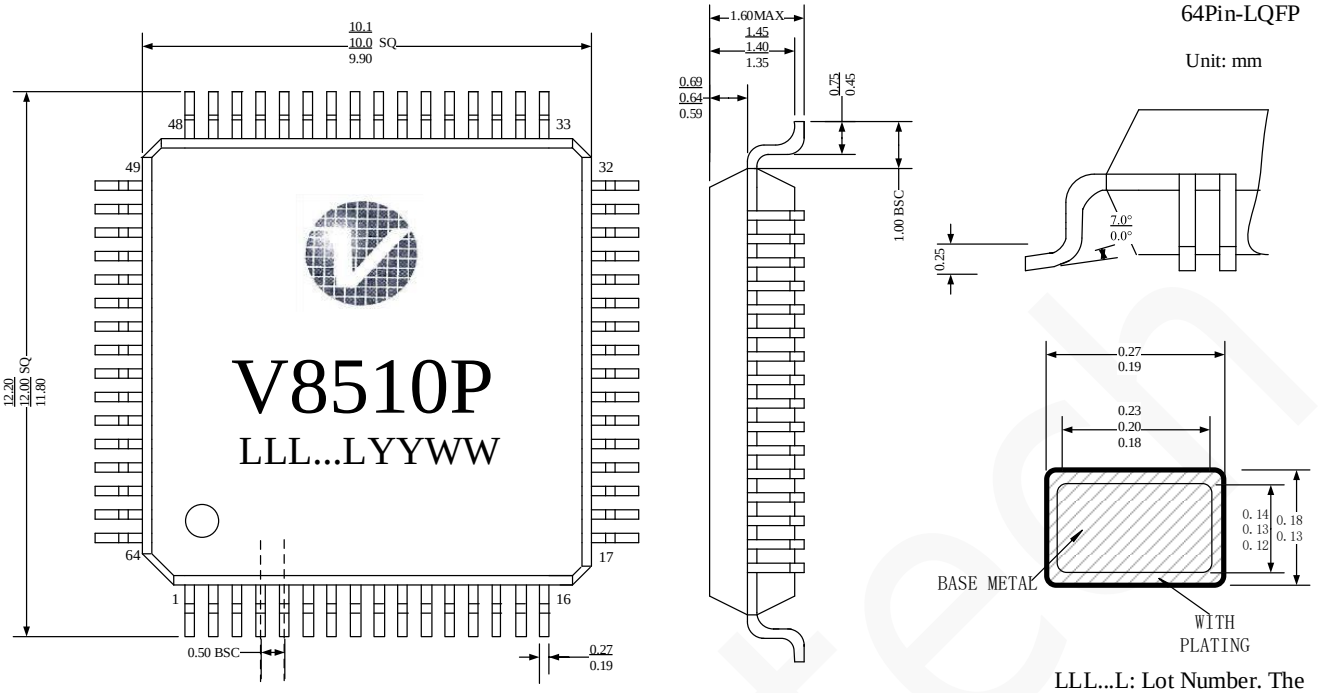


80Pin-LQFP

Unit: mm

LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

29.4 V8510P Package Dimension



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week